2M x 36/2M x 40 DRAM Modules

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

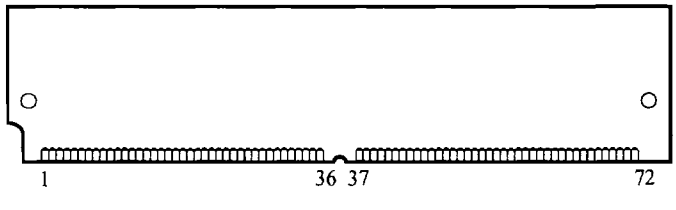
- Optimized for use in ECC applications
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode, Read-Modify-Write cycles
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Au and Sn/Pb versions available

Description

The ECC-Optimized SIMMs, IBM11D2370BA and IBM11D2400BA are 8MB industry standard 72 pin 4-byte single inline memory modules (SIMMs). The Modules are organized as 2M x 36/40 high speed memory arrays, and are configured as 2 1M x 36/40 banks - each independently selectable via unique $\overline{RAS}$ inputs. The 2M x 36 assembly is intended for use in 8 byte applications, typically having 64 data and 8 check bits (64/72 code). The 2M x 40 assembly is applicable to 4 byte applications with 32 data and 7 or 8 check bits (32/39 code), or 8 byte applications with extended error correction capabilities. The modules are manufactured with 18 or 20 1M x 4 devices, each in a 350 mil package, and are compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-pin SIMMs provide a high-performance, flexible 4-byte interface in a 4.25" long footprint. Related products include other density offerings and parity SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS1}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS1}$	Column Address Strobe
$\overline{WE}$	Read/write Input
$\overline{OE}$	Output Enable
A0 - A9	Address Inputs
DQ0-35 or DQ0-39	Data Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
$\overline{ECC}$, PD1 - PD4	Presence Detects

Pinout

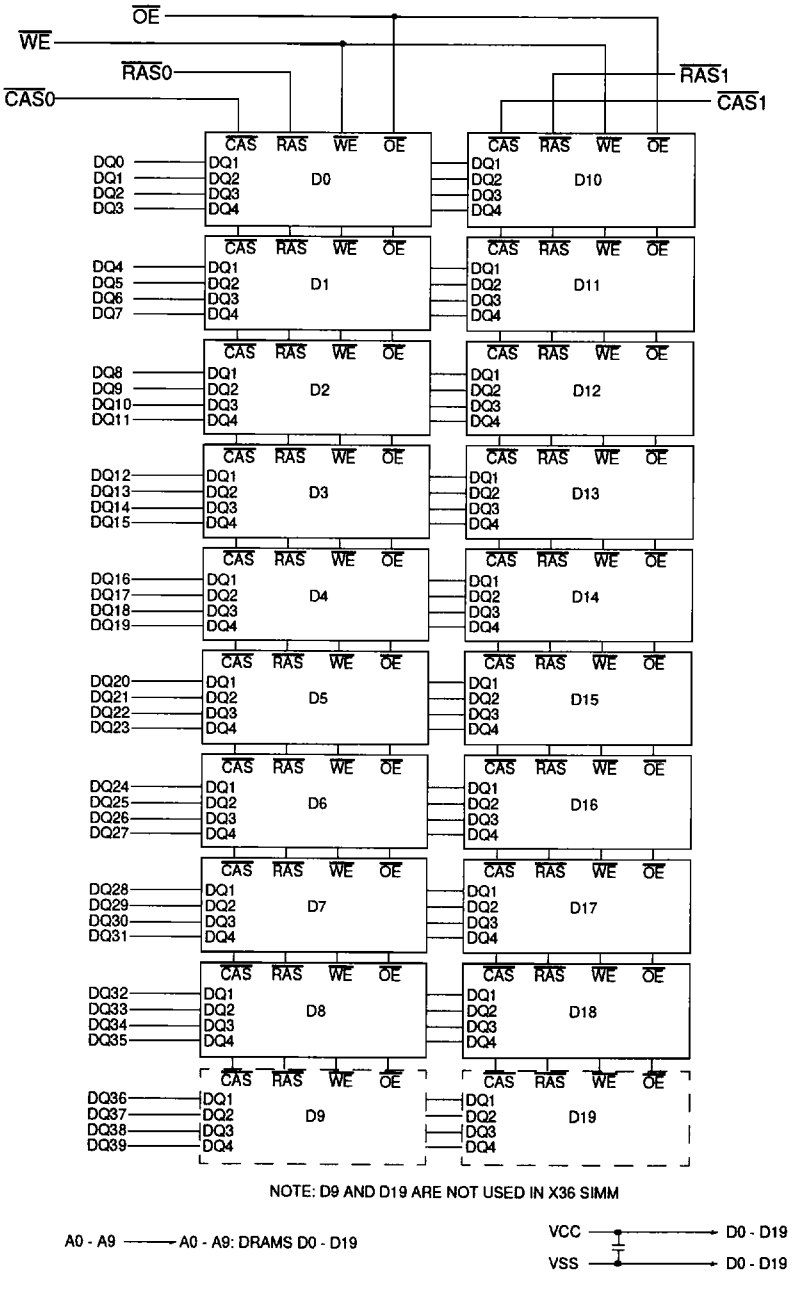
Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name	Pin #	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ19	49	DQ22	61	DQ33
2	DQ0	14	A2	26	DQ14	38	DQ20	50	DQ23	62	DQ34
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ24	63	DQ35
4	DQ2	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ36
5	DQ3	17	A5	29	DQ16	41	NC	53	DQ26	65	DQ37
6	DQ4	18	A6	30	V_{CC}	42	NC	54	DQ27	66	DQ38
7	DQ5	19	$\overline{OE}$	31	A8	43	$\overline{CAS1}$	55	DQ28	67	PD1
8	DQ6	20	DQ8	32	A9	44	$\overline{RAS0}$	56	DQ29	68	PD2
9	DQ7	21	DQ9	33	NC	45	$\overline{RAS1}$	57	DQ30	69	PD3
10	V_{CC}	22	DQ10	34	NC	46	DQ21	58	DQ31	70	PD4
11	NC	23	DQ11	35	DQ17	47	$\overline{WE}$	59	V_{CC}	71	DQ39
12	A0	24	DQ12	36	DQ18	48	$\overline{ECC}$	60	DQ32	72	V_{SS}

1. DQ36 - DQ39 are NC for x36 SIMM.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D2370BA-60	2M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2370BA-70	2M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2370BA-60	2M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E2370BA-70	2M x 36	70ns	Au	4.25" x 1" x .360"	
IBM11D2400BA-60	2M x 40	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D2400BA-70	2M x 40	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E2400BA-60	2M x 40	60ns	Au	4.25" x 1" x .360"	
IBM11E2400BA-70	2M x 40	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	All DQ Bits
Standby	H	X	X	X	X	X	High Impedance
Read	L	L	H	L	Row	Col	Valid Data Out
Early-Write	L	L	L	X	Row	Col	Valid Data In
Late-Write / RMW	L	L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Fast Page Mode-Read 1st cycle	L	H→L	H	L	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	L	N/A	Col	Valid Data Out
Fast Page Mode-Write 1st cycle	L	H→L	L	X	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	X	N/A	Col	Valid Data In
Fast Page Mode Read-Modify-Write: 1st cycle	L	H→L	H→L	L→H	Row	Col	Valid Data Out, Valid Data In
Subsequent Cycles	L	H→L	H→L	L→H	N/A	Col	Valid Data Out, Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	X	High Impedance

Presence Detect

Pin	-60	-70
$\overline{ECC}$ (ECC Optimized SIMM)	V_{SS}	V_{SS}
PD1	NC	NC
PD2	NC	NC
PD3	NC	V_{SS}
PD4	NC	NC

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +6.5	V	1
V_{IN}	Input Voltage	-0.7 to V_{CC} + 0.7	V	1
V_{OUT}	Output Voltage	-0.7 to V_{CC} + 0.7	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	13.2	W	1, 2
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}	V	1
V_{IL}	Input Low Voltage	0.0	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	x36 Max	x40 Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	100	104	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$)	66	70	pF	
C_{I3}	Input Capacitance ($\overline{WE}$)	112	116	pF	
C_{I4}	Input Capacitance ($\overline{OE}$)	112	116	pF	
$C_{I/O}$	Output Capacitance (All DQ bits)	25	25	pF	

2M x 36 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1098	mA	1, 2, 3
		-70	—	990		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	36	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1098	mA	1, 3, 4
		-70	—	990		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	693	mA	1, 2, 3
		-70	—	648		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	36	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1098	mA	1, 3, 4
		-70	—	990		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-180	+180	µA	
		$\overline{RAS}$, $\overline{CAS}$	-90	+90		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank..

2M x 40 DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1220	mA	1, 2, 3
		-70	—	1100		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})		—	40	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH}: t_{RC} = t_{RC} min)	-60	—	1220	mA	1, 3, 4
		-70	—	1100		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	770	mA	1, 2, 3
		-70	—	720		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	40	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1220	mA	1, 3, 4
		-70	—	1100		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{OE}$, $\overline{WE}$, ADDRESS	-200	+200	µA	
		$\overline{RAS}$, $\overline{CAS}$	-100	+100		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-20	+20	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}
4. Refresh current is specified for 1 bank..

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	10	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10	—	10	—	ns	
t_{ODD}	$\overline{OE}$ to D_{IN} Delay Time	—	—	—	—	ns	3
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	—	—	—	—	ns	3
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	45	—	50	—	—	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	10	—	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings, $\overline{CAS}$ or $\overline{WE}$.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	—	20	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OES}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$	—	—	—	—	ns	4
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{OHO}	Output Data Hold Time from $\overline{OE}$	0	—	0	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	10	0	15	ns	5
t_{ROH}	$\overline{RAS}$ Hold to Output Enable	10	—	10	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	10	—	15	—	ns	
t_{OEZ}	Output Buffer Turn-off Delay from $\overline{OE}$		10		15	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.
3. Either t_{RCH} or t_{RRH} must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	2, 3

1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. Measured with the specified current load and 100pF.
3. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}, t_{OEA}.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RWC}	Read-Modify-Write Cycle Time	160	—	180	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90	—	95	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45	—	45	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	55	—	60	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	10	—	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPW} are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.) and $t_{CPW} \geq t_{CPW}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell: If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	90	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	—	—	—	—	ns	1

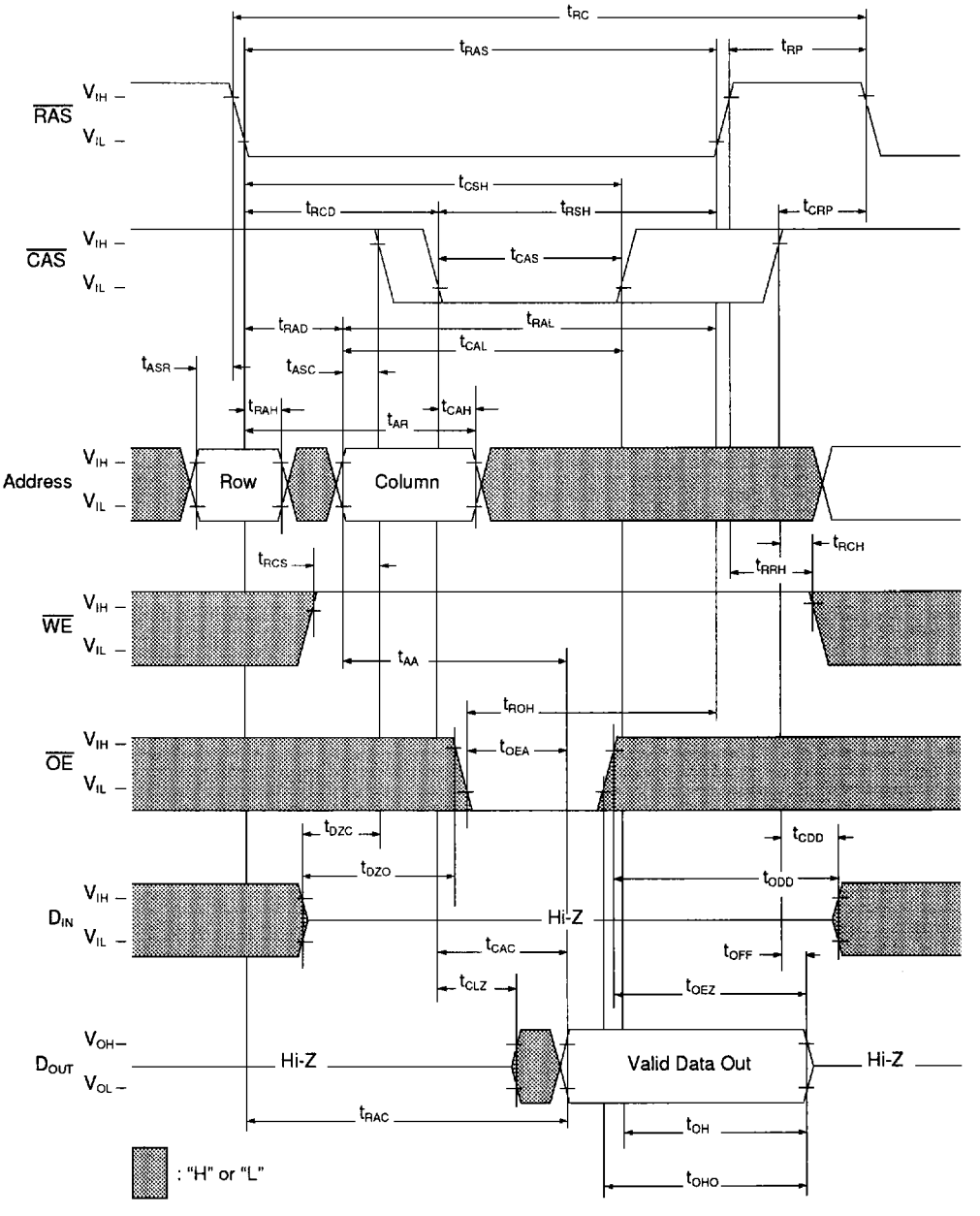
1. This timing parameter is not applicable to this product, but applies to a related product in this family.

Refresh Cycle

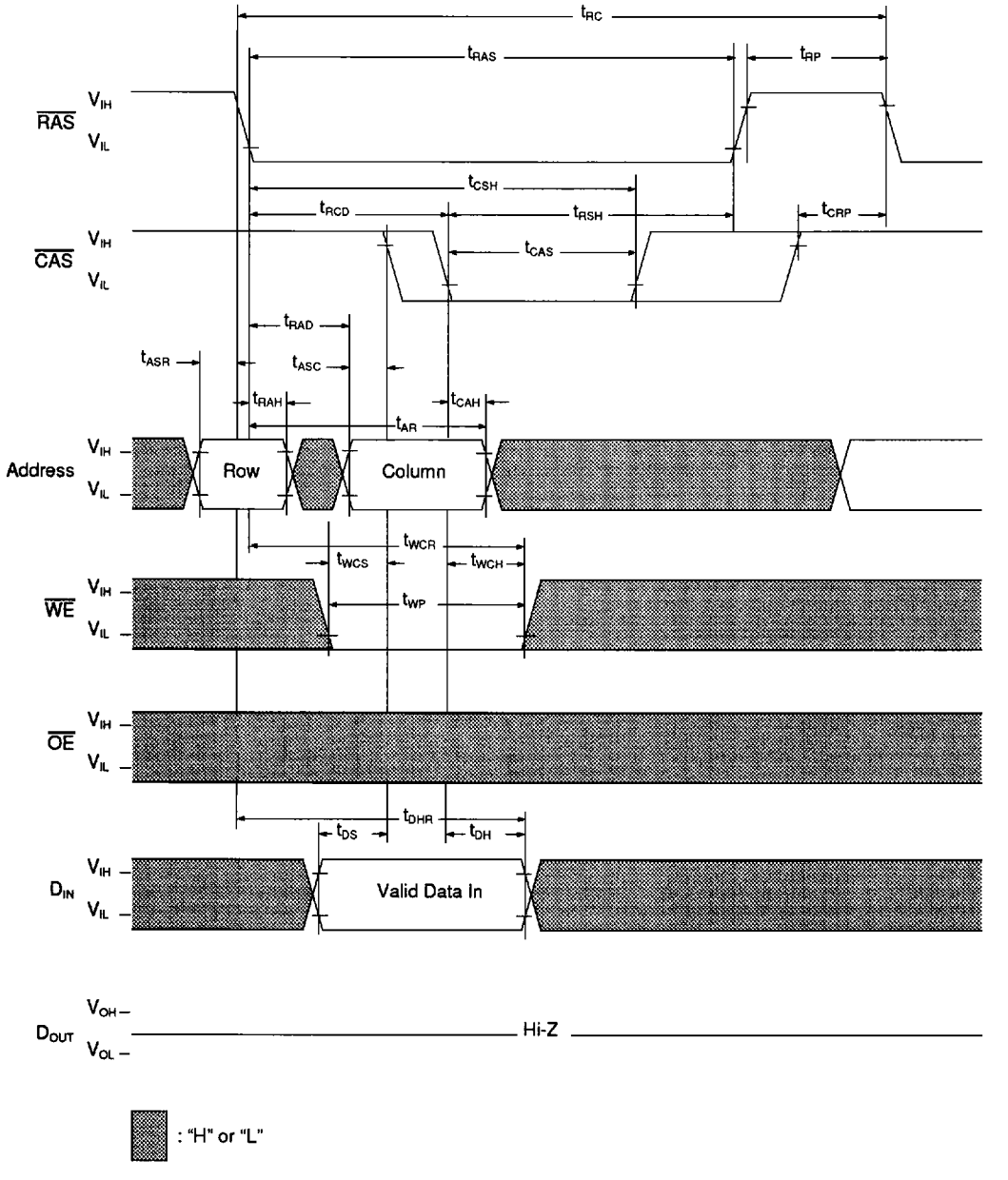
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	15	—	15	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	5	—	5	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	0	—	0	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 Refreshes are required every 16ms.

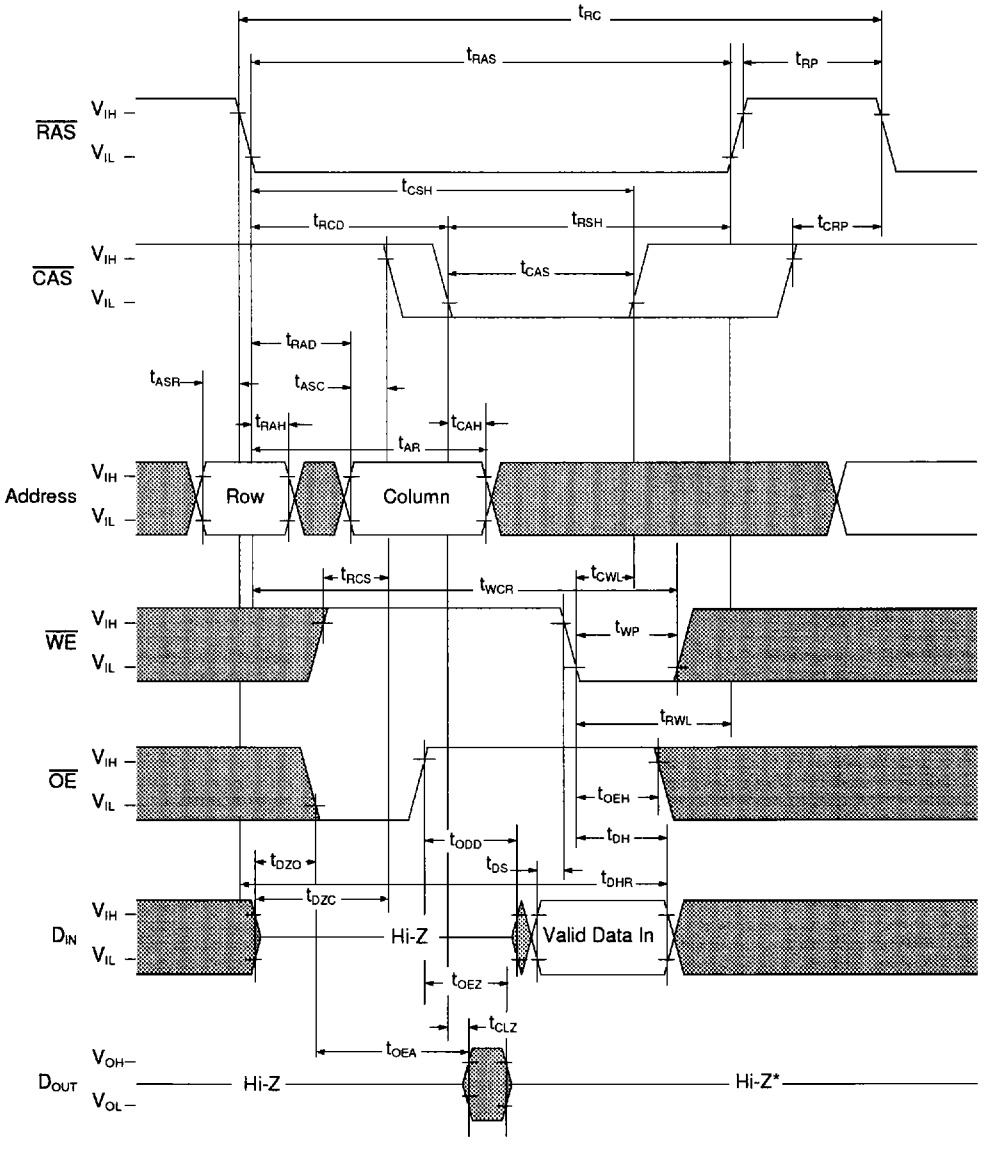
Read Cycle


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tRAH
tAR
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tROH
OE
tOEA
tDZC
tDZO
tCDD
tODD
DIN
Hi-Z
tCAC
tOFF
tCLZ
tOEZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
tOHO
: "H" or "L"

Write Cycle (Early Write)

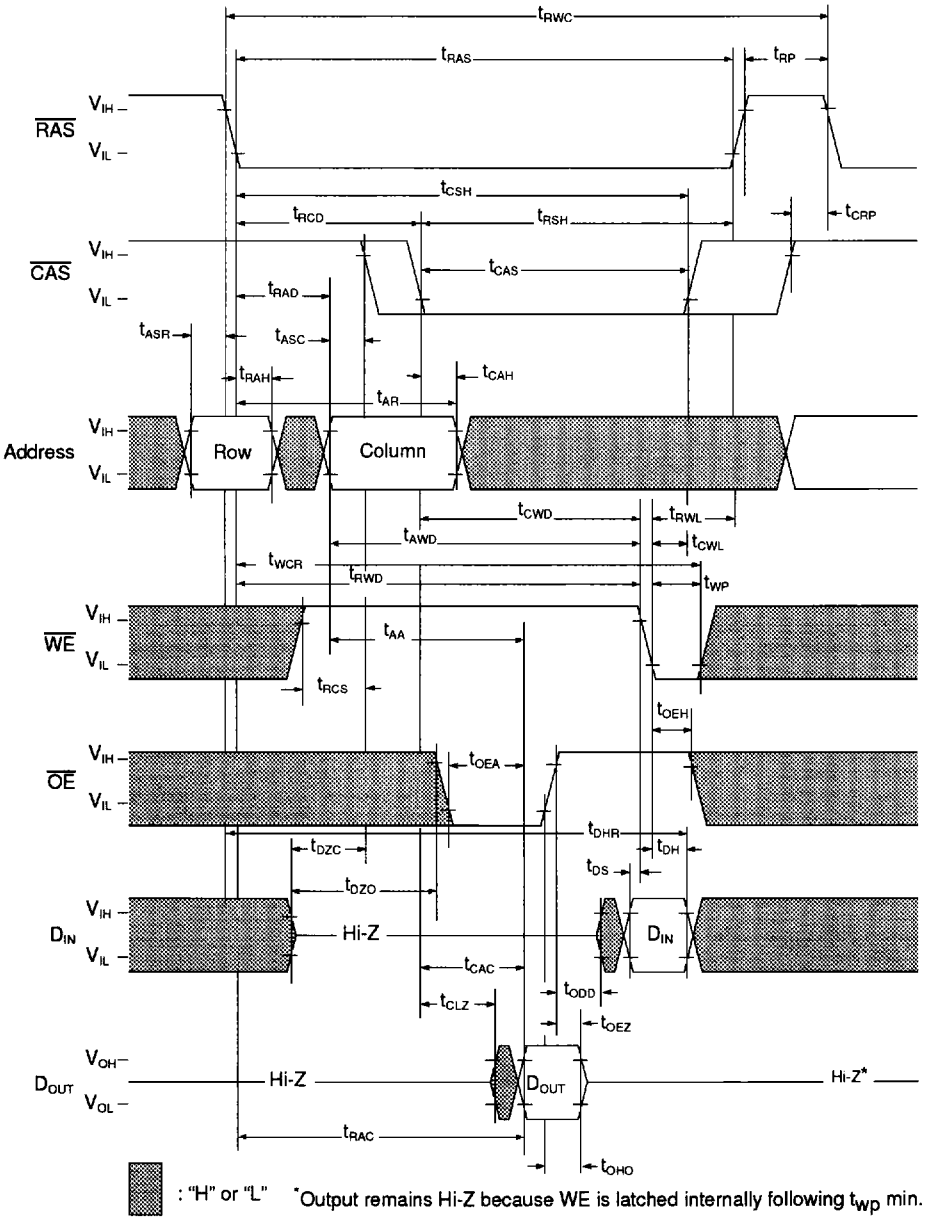


Write Cycle (Late Write)

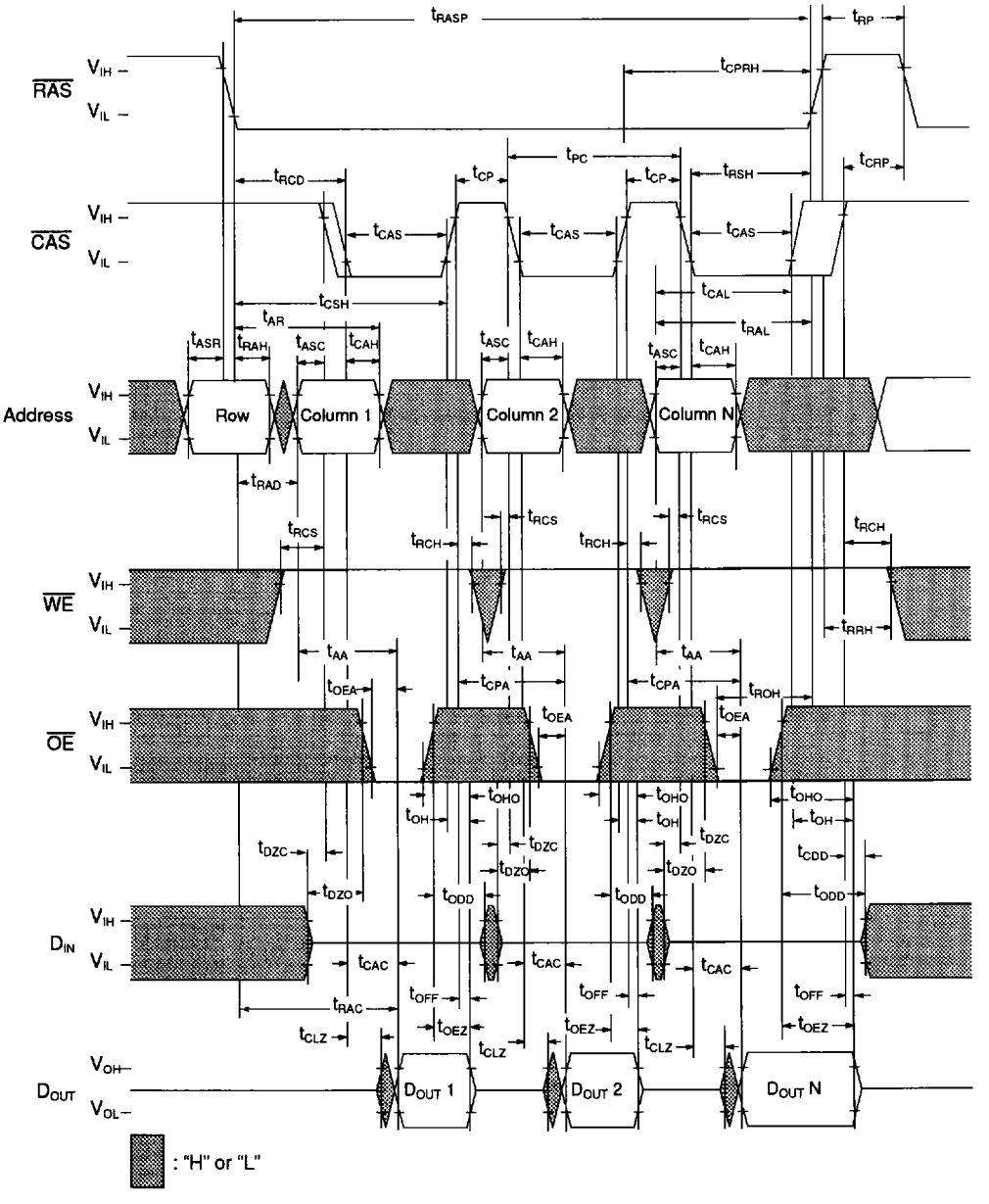


: "H" or "L" *Output remains Hi-Z because $\overline{WE}$ is latched internally following t_{WP} min.

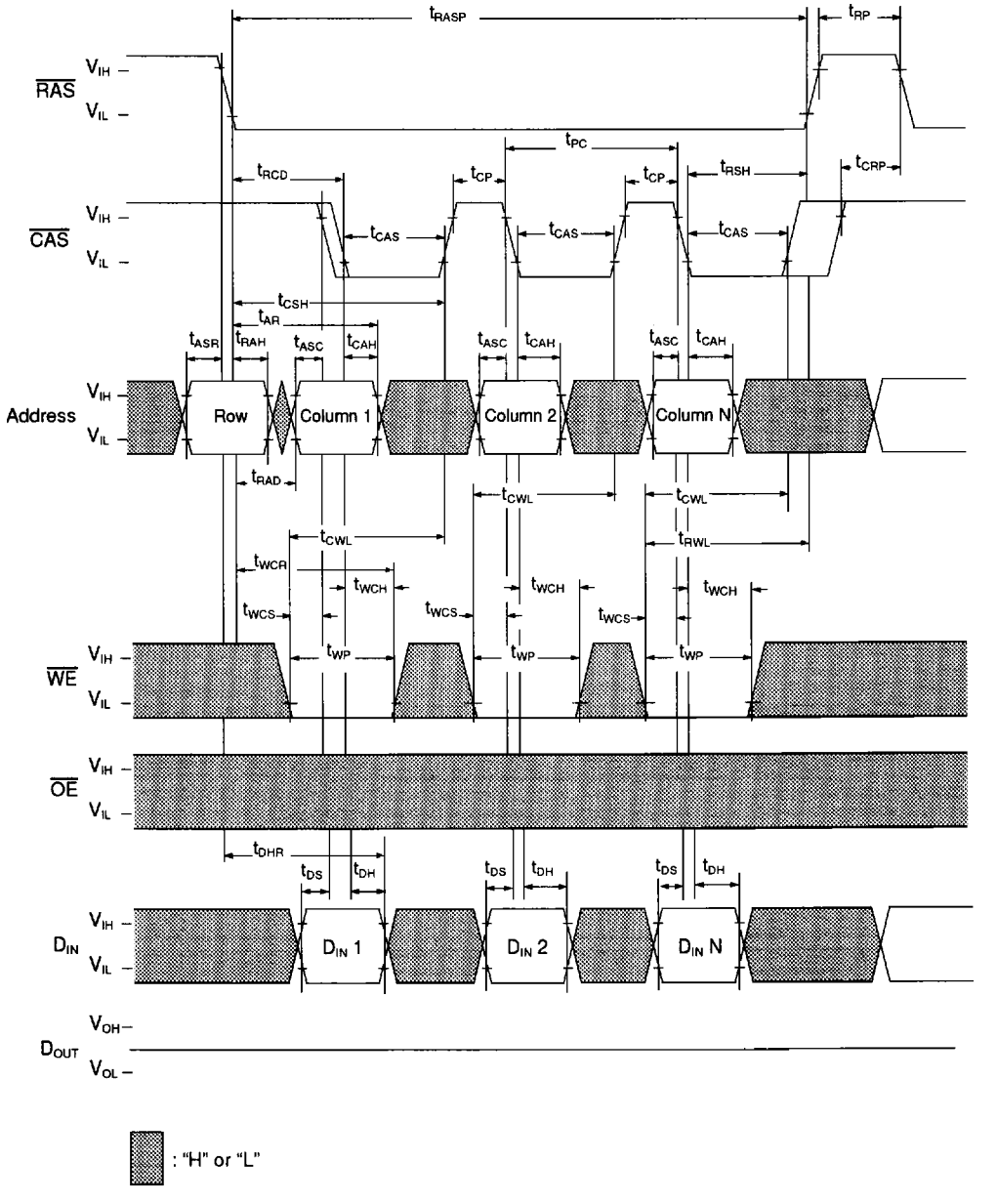
Read-Modify-Write Cycle



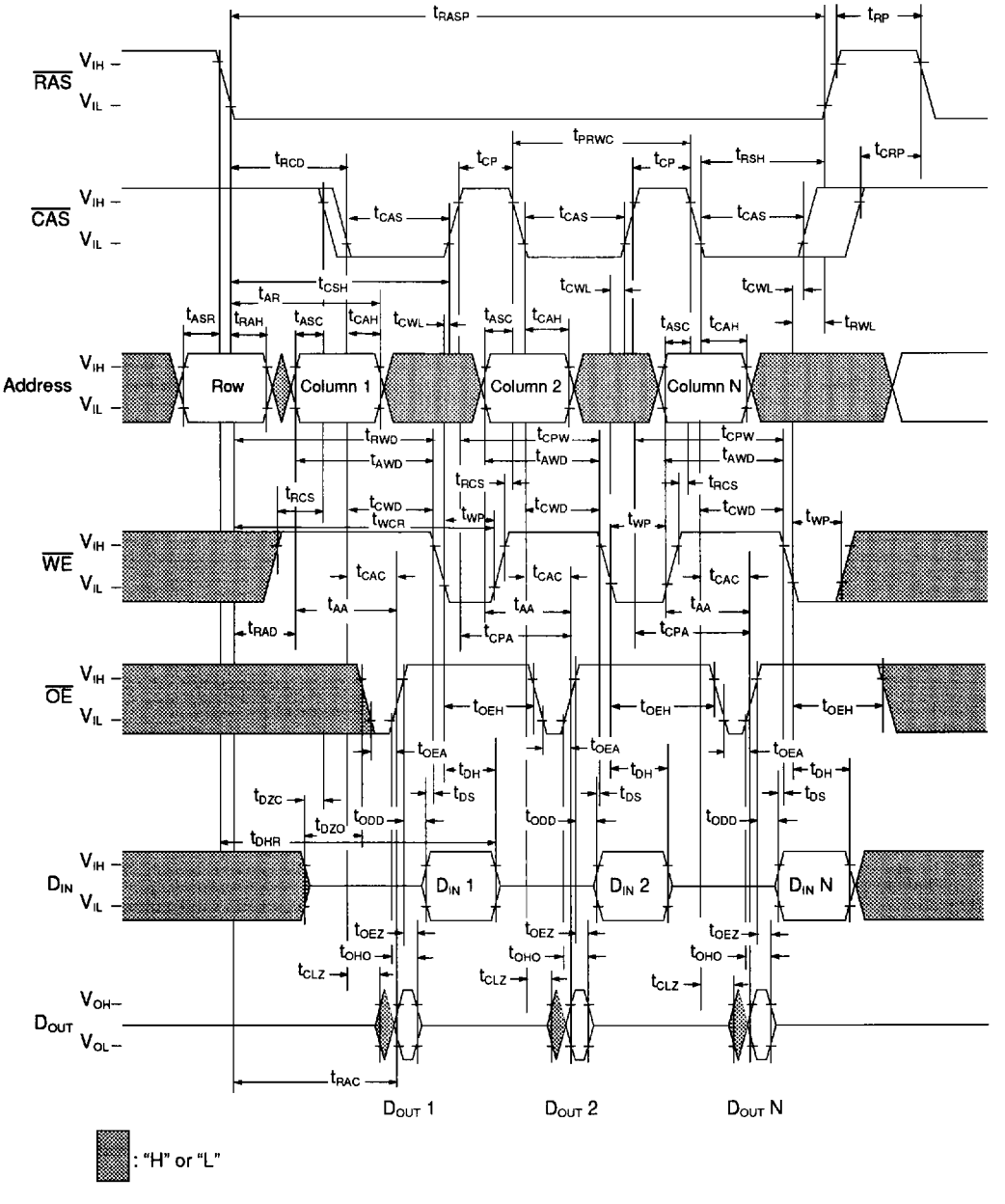
Fast Page Mode Read Cycle



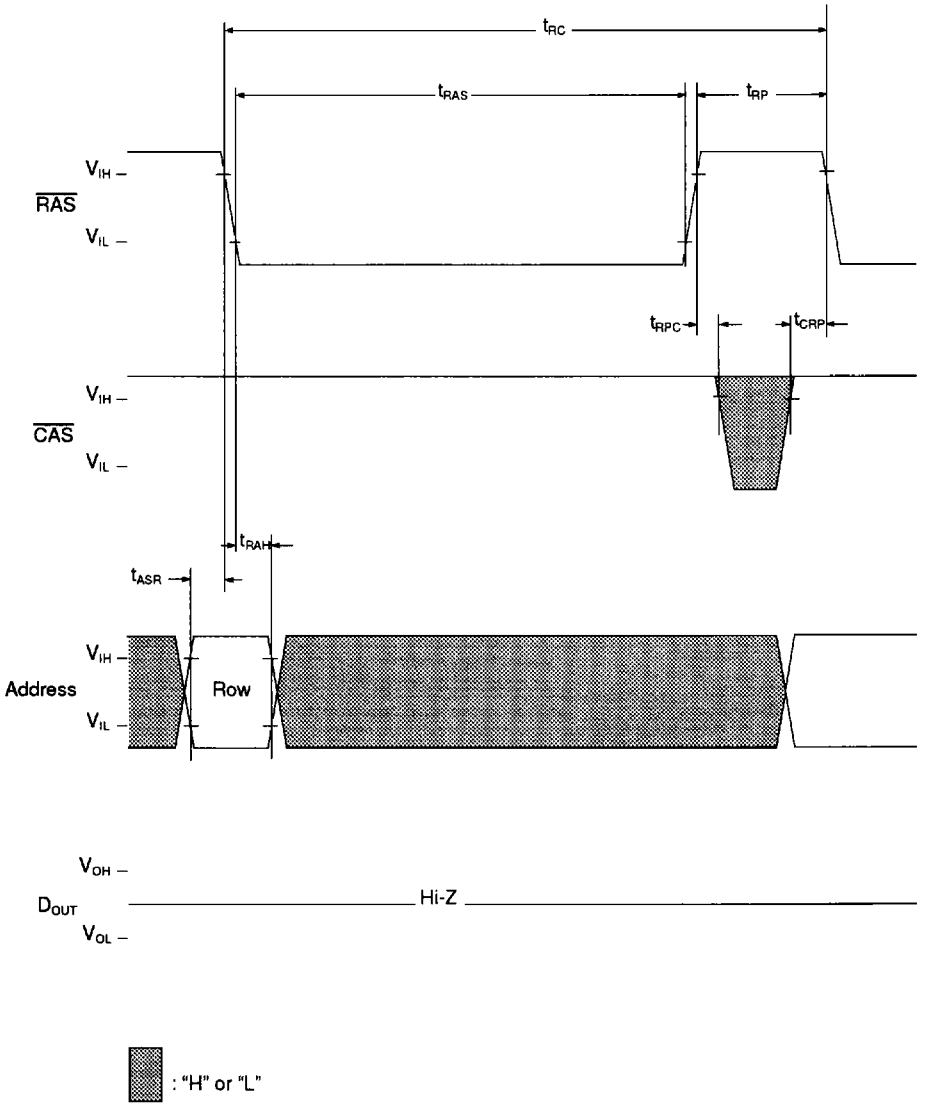
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle

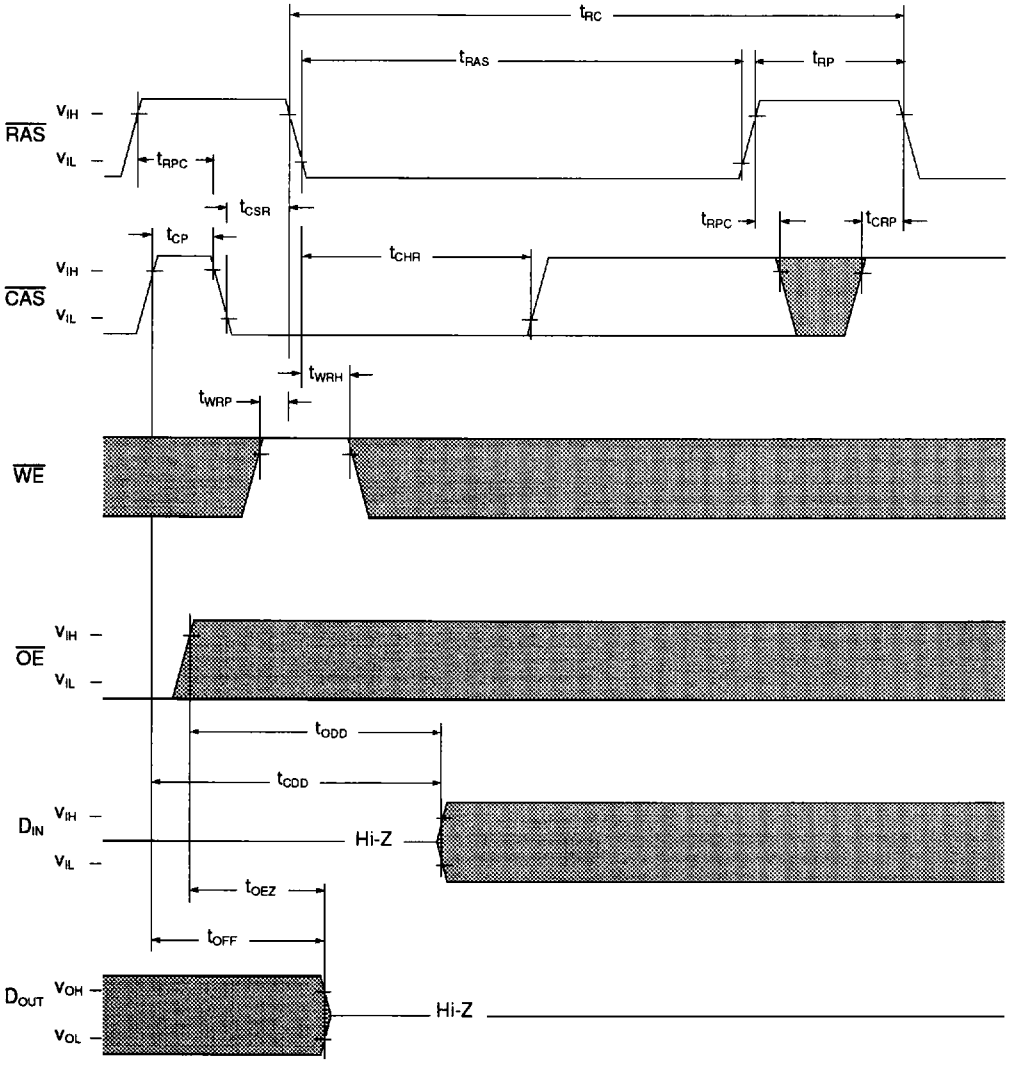


$\overline{RAS}$ Only Refresh Cycle



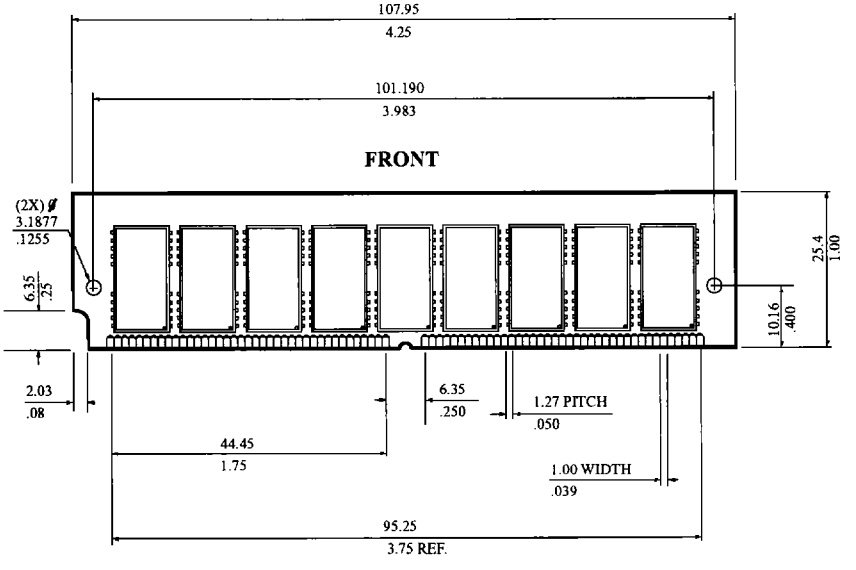
Note: $\overline{WE}$, $\overline{OE}$, D_{IN} are "H" or "L"

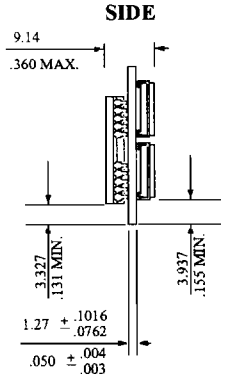
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing (IBM11D2400BA)





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES