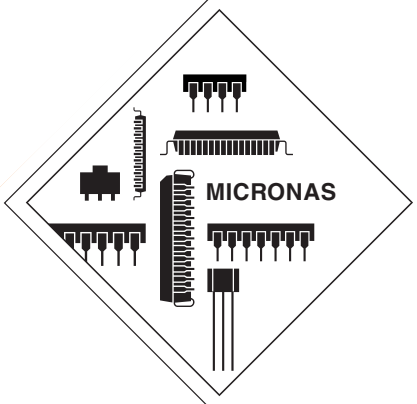

ADVANCE INFORMATION

DDP 3310B
Display and Deflection Processor

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MICRONAS

Contents

Contents, continued

Display and Deflection Processor

1. Introduction

The DDP 3310B is a single-chip digital Display and Deflection Processor designed for high-quality back-end applications in 100/120-Hz TV sets with 4:3- or 16:9 picture tubes. The IC can be combined with members of the DIGIT 3000 IC family (VPC 32xx, TPU 3040), or it can be used with third-party products. The IC contains the entire digital video component and deflection processing and all analog interface components.

1.1. Main Features

Video processing

- linear horizontal scaling (0.25 … 4)
- non-linear horizontal scaling “panoramavision”
- dynamic peaking
- soft limiter (gamma correction)
- color transient improvement
- programmable RGB matrix
- picture frame generator
- two analog RGB/Fast-Blank inputs

Deflection processing

- scan velocity modulation output
- high-performance H/V deflection
- EHT compensation for vertical / East/West
- soft start/stop of H-Drive
- vertical angle and bow
- differential vertical output
- vertical zoom via deflection
- horizontal and vertical protection circuit
- adjustable horizontal frequency for VGA/SVGA display

Miscellaneous

- selectable 4:1:1/4:2:2 YC_rC_b input
- selectable 27/32-MHz line-locked clock input
- crystal oscillator for horizontal protection
- automatic picture tube adjustment (cutoff, white-drive)
- single 5-V power supply
- hardware for simple 50/60-Hz to 100/120-Hz conversion (display frequency doubling)
- two I^2C-controlled PWM outputs
- beam current limiter

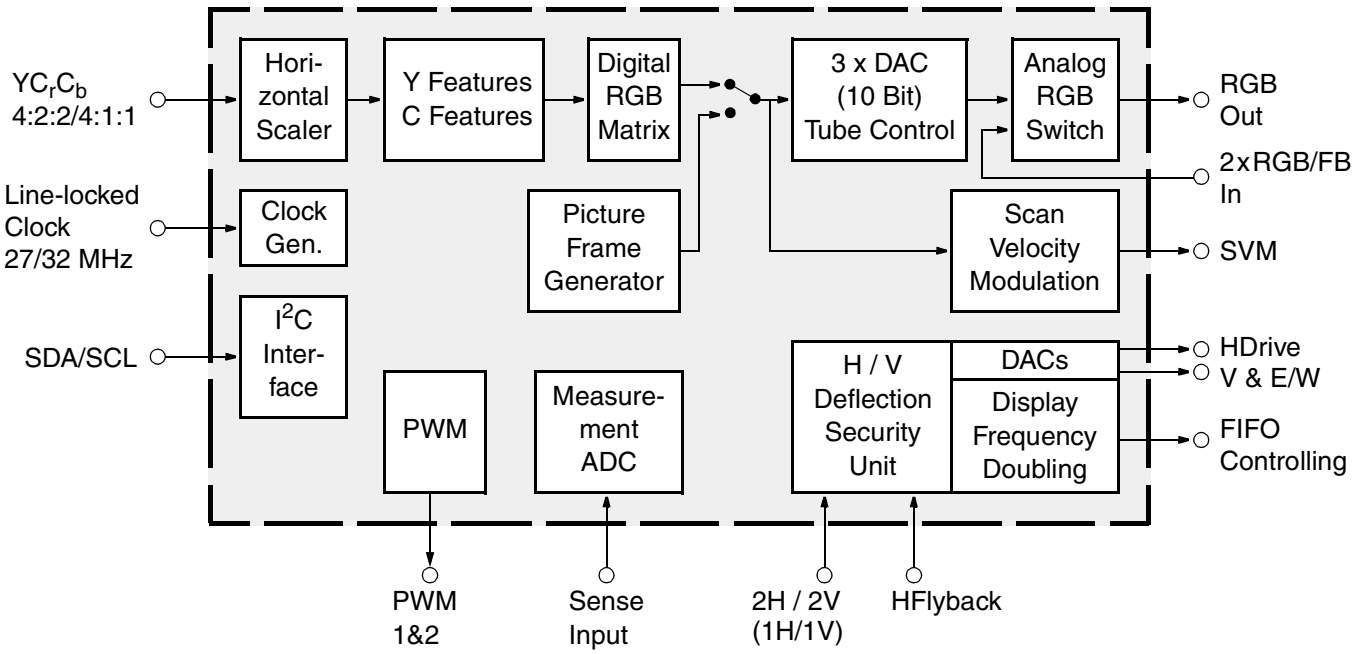


Fig. 1–1: Block diagram of the DDP 3310B

1.2. System Architecture

The DDP 3310B is a mixed-signal IC containing the entire digital video component processing such as chroma transient improvement (CTI), adaptive luma peaking, and a non-linear 'Panorama' aspect ratio conversion. All deflection related signals can be adapted to different scan rates. The analog section contains all analog interface components and an ADC, to compensate long term changes of the picture tube parameters and extreme high-tension effects. Fig. 1–1 shows the block diagram of the single-chip Display and Deflection Processor.

1.3. System Application

Fig. 1–2 depicts several DDP applications. Since the DDP functions as a video back-end, it must be complemented with additional functionality to form a complete TV set.

The VPC 32xx family processes all worldwide analog video signals (including the European PALplus) and allows non-linear Panorama aspect ratio conversion. Thus, 4:3 and 16:9 systems can easily be configured by software. The aspect ratio scaling is also used as a sample rate converter to provide a line-locked digital component output bus (YC_rC_b) compliant to ITU-R-601. All video processing and line-locked clock/data generation is derived from a single 20.25-MHz crystal. An optional adaptive 2H/4H comb filter (VPC 32xx) performs Y/C separation for PAL and NTSC and all of their substandards.

The VPC 32xxD and the CIP 3250A provide a high-quality analog RGB interface with character insertion capability. This allows appropriate processing of external sources such as MPEG 2 set-top boxes in transparent (4:2:2) quality. Furthermore, it translates RGB/Fast-Blank signals to the common digital video bus and makes those signals available for 100-Hz processing. In some European countries (Italy), this feature is mandatory.

The IP indicates memory-based image processing, such as scan rate conversion, vertical processing (Zoom), or PAL+ reconstruction.

Examples:

– Europe: 15 kHz/50 Hz → 32 kHz/100 Hz interlaced

– US: 15 kHz/60 Hz → 31 kHz/120 Hz non-interlaced

Note: The DDP 3310B and the VPC 32xx families support memory-based applications through line-locked clocks, syncs, and data. The CIP 3250A may run either with the native DIGIT3000 clock but also with a line-locked clock system.

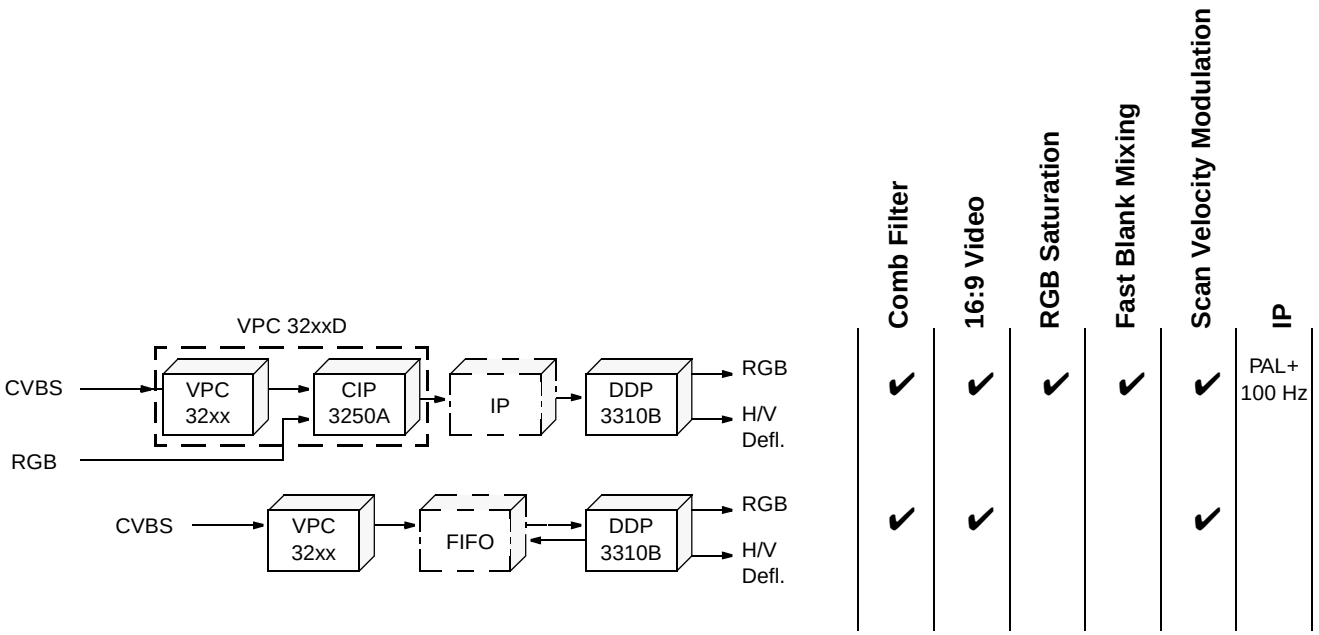


Fig. 1–2: DDP 3310B applications

2. Functional Description

2.1. Display Part

The display part converts the digital YC_rC_b to analog RGB (see Fig. 2–7) and provides contrast and saturation adjustment. In case of YC_rC_b 4:1:1 an interpolation filter is used, which converts the digital input signal to YC_rC_b 4:2:2 standard. The 4:2:2 YC_rC_b signal is processed by the horizontal scaler. In the luminance processing path, a variety of features, such as dynamic peaking and soft limiting, are provided. In the chrominance path, the C_rC_b signals are converted to 4:4:4 format and filtered by a color transient improvement circuit. The YC_rC_b signal is converted by a programmable matrix to RGB color space.

2.1.1. Input Interface

The data inputs Y0…Y7 and C0…C7 are clocked with the external clock LLC2. The clock frequency is selectable for 27 or 32 MHz. A clock generator converts the different external line-locked clock rates to a common internal sample rate of appr. 40.5 MHz in order to provide a fix bandwidth for all digital filters. The horizontal scaler is used for conversion of scan rate and non-linear aspect ratio. The horizontal sync puls at the HS pin should be an active video signal, which is not vertically blanked.

The input interface signals are

– external clock (LLC2)

– luma / chroma inputs (Y0…Y7 / C0…C7)

– horizontal sync (HS) / vertical sync (VS, VS2)

2.1.2. Horizontal Scaler

The scaler block allows linear or non-linear horizontal scaling of the digital input video signal in the range of 0.25 to 4. Non-linear scaling, also called “panorama vision”, provides a geometrical distortion of the input picture. It is used to fit a picture with 4:3 format on a 16:9 screen by stretching the picture geometry at the borders. The inverse effect can be produced by the scaler, also. The scaler consists of a programmable decimation and interpolation filter and a 1/2H FIFO memory.

A summary of scaler modes is given in Table 2–1.

Table 2–1: Scaler modes

Mode	Scale Factor	Description
Panorama 4:3 →16:9	non-linear compr.	4:3 source displayed on a16:9 tube, borders distorted
Waterglass 16:9 →4:3	non-linear zoom	Letterbox source (PAL+) displayed on a 4:3 tube, vertical overscan, borders distorted, no cropping
27→40.5 MHz	1.5 linear	sample rate conversion from external to internal pixel clock
32 →40 MHz	1.25 linear	sample rate conversion from external to internal pixel clock

2.1.3. Luma Processing

The blacklevel of the input signal is assumed to be 16 (ITU-R standard). The luminance signal is multiplied by a factor between 0 and 2 subdivided into 64 steps.

With a contrast adjustment of 32 (gain=1) the signal can be shifted by ±100 % of its maximal amplitude with the digital brightness value. This is for adjustment of the headrooms for under- and overshoot. After the brightness addition, the negative going signals are limited to zero. It is desirable to keep a small positive offset with the signal to prevent undershoots produced by the peaking from being cut.

2.1.4. Dynamic Peaking

Especially with decoded composite signals and notch filter luminance separation as input signals, it is necessary to improve the luminance frequency characteristics. With transparent high-bandwidth signals, it is sometimes desirable to soften the image.

In the DDP 3310B, the luma frequency response is improved by “dynamic” peaking. It adapts to the amplitude and the frequency of the input signal. Small AC amplitudes are sharpened while large AC amplitudes remain nearly unmodified.

The dynamic range can be adjusted from –14 to +14 dB for small high-frequency signals. There is separate adjustment for signal overshoot and for signal undershoot. For large signals, the dynamic range is limited by a non-linear function that does not create any visible alias components. The peaking can be switched over to “softening” by inverting the peaking term by software.

The center frequency of the peaking filter is selectable from 2.5 MHz to 3.2 MHz. For S-VHS and for notch filter color decoding, the total system frequency responses for both PAL and NTSC are shown in Fig. 2–1 and Fig. 2–2. (All frequencies refer to a 50/60-Hz video signal).

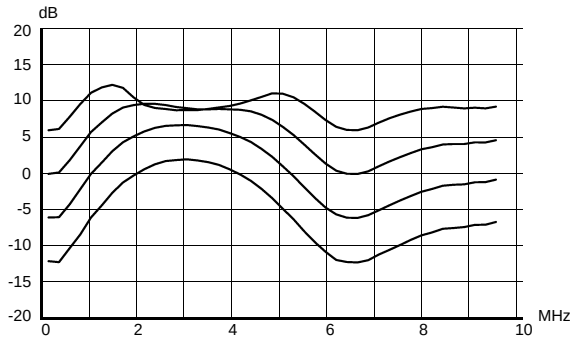


Fig. 2–1: Dynamic peaking frequency response

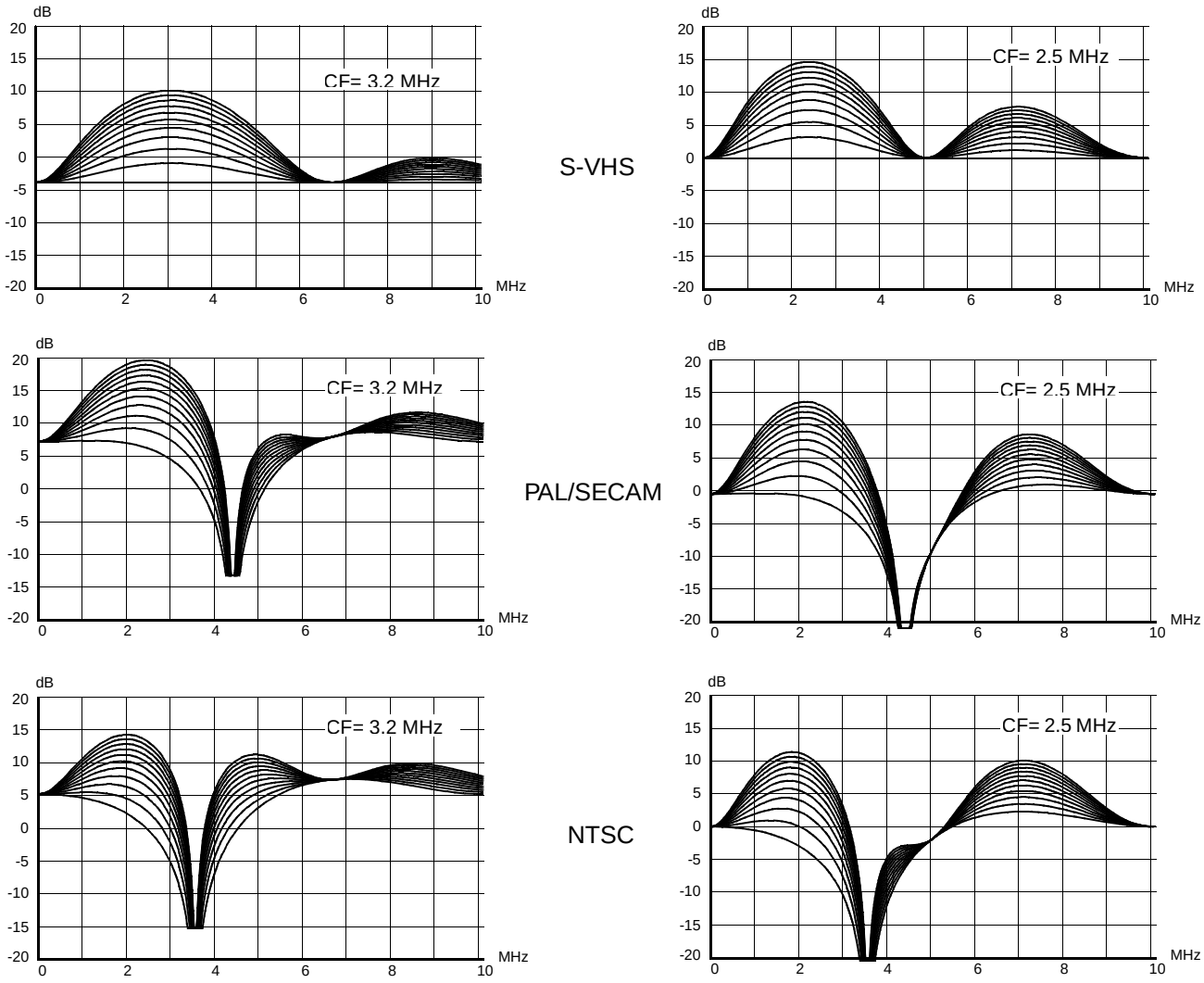


Fig. 2–2: Total frequency response for peaking filter and S-VHS, PAL, NTSC

2.1.5. Soft Limiter

The dynamic range of the processed luma signal must be limited to prevent the CRT from overload. An appropriate headroom for contrast, peaking, and brightness can be adjusted by the TV manufacturer according to the CRT characteristics. All signals above this limit will be “soft”-clipped. A characteristic diagram of the soft limiter is shown in Fig. 2–3. The total limiter consists of three parts:

Part A includes adjustable tilt point and gain. The gain before the tilt value is 1. Above the tilt value, a part (0…15/16) of the input signal is subtracted from the input signal itself. Therefore, the gain is adjustable from 16/16 to 1/16, when the slope value varies from 0 to 15. The tilt value can be adjusted from 0 to 511. Part B has the same characteristics as part A. The subtracting part is also relative to the input signal, so the total differential gain will become negative if the sum of slope A and slope B is greater than 16 and the input signal is above the both tilt values (see characteristics).

Finally, the output signal of the soft limiter will be clipped by a hard limiter adjustable from 256 to 511.

2.1.6. Chroma Input

The chroma input signal can either be YC_rC_b in 4:1:1 or in 4:2:2 format. For the digital signal processing, the time-multiplexed chroma samples will be demultiplexed and synchronized with the signal at the HS pin. The input formatter accepts either two’s complement or binary offset code. Also, the delay can be adjusted within a range of ±2 input clocks relative to the luma signal; this doesn’t affect the chroma multiplex.

Table 2–2: 4:1:1 Chroma format

Pin Name	Pixel Number			
	1	2	3	4
C7	C_{b1}^{7}	C_{b1}^{5}	C_{b1}^{3}	C_{b1}^{1}
C6	C_{b1}^{6}	C_{b1}^{4}	C_{b1}^{2}	C_{b1}^{0}
C5	C_{r1}^{7}	C_{r1}^{5}	C_{r1}^{3}	C_{r1}^{1}
C4	C_{r1}^{6}	C_{r1}^{4}	C_{r1}^{2}	C_{r1}^{0}
Note: C_x^y; x = pixel number, y = bit number				

Table 2–3: 4:2:2 Chroma format

Pin Name	Pixel Number			
	1	2	3	4
C7	C_{b1}^{7}	C_{r1}^{7}	C_{b3}^{7}	C_{r3}^{7}
C6	C_{b1}^{6}	C_{r1}^{6}	C_{b3}^{6}	C_{r3}^{6}
C5	C_{b1}^{5}	C_{r1}^{5}	C_{b3}^{5}	C_{r3}^{5}
C4	C_{b1}^{4}	C_{r1}^{4}	C_{b3}^{4}	C_{r3}^{4}
C3	C_{b1}^{3}	C_{r1}^{3}	C_{b3}^{3}	C_{r3}^{3}
C2	C_{b1}^{2}	C_{r1}^{2}	C_{b3}^{2}	C_{r3}^{2}
C1	C_{b1}^{1}	C_{r1}^{1}	C_{b3}^{1}	C_{r3}^{1}
C0	C_{b1}^{0}	C_{r1}^{0}	C_{b3}^{0}	C_{r3}^{0}
Note: C_x^y; x = pixel number, y = bit number				

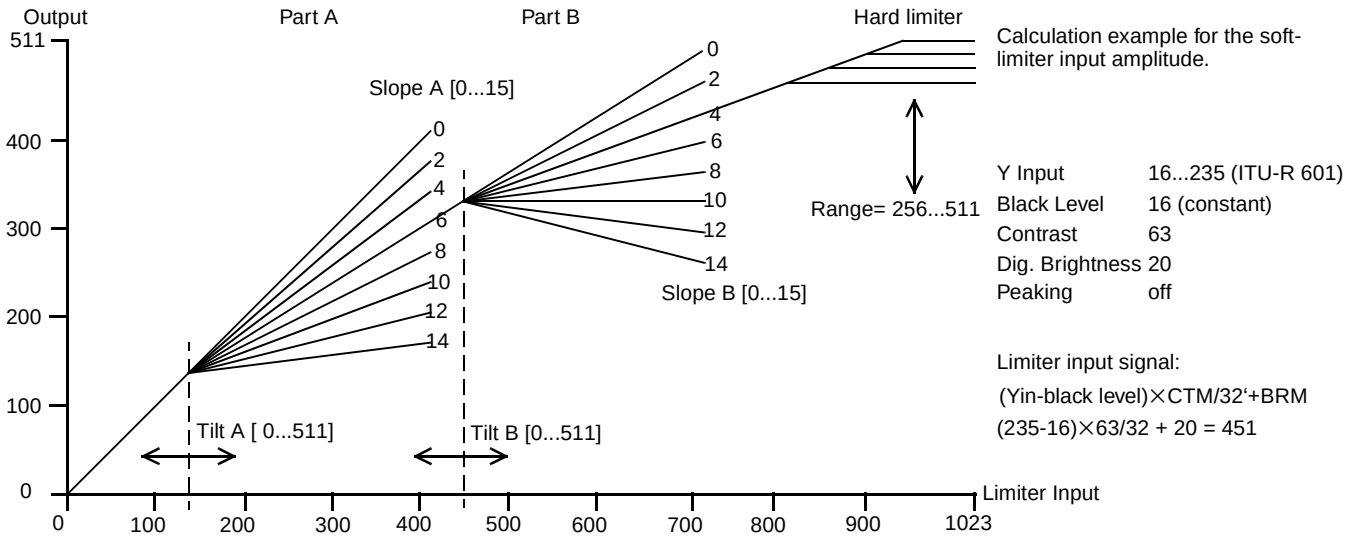


Fig. 2–3: Characteristics of soft limiter A and B and hard limiter

2.1.7. Chroma Interpolation

In case of YC_rC_b 4:1:1 input format, an interpolation filter is used which converts the digital input signal to 4:2:2 format. This filter runs with the incoming pixel clock frequency.

The signal is passed to the scaler in YC_rC_b 4:2:2 format in order to convert the incoming pixel clock frequency (27/32 MHz) to the internal frequency (40.5/40 MHz). A linear phase interpolator is used to convert the chroma sampling rate from 4:2:2 to 4:4:4.

The frequency response of the interpolator is shown in Fig. 2–4. All further processing is carried out at the full sampling rate.

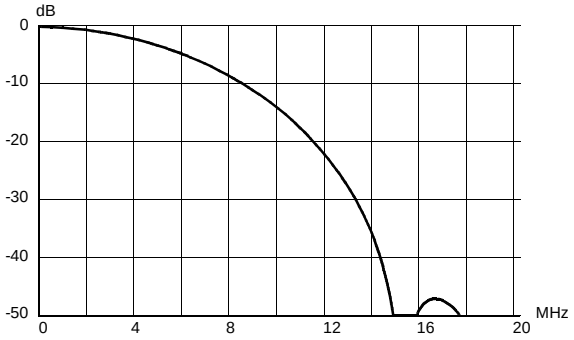
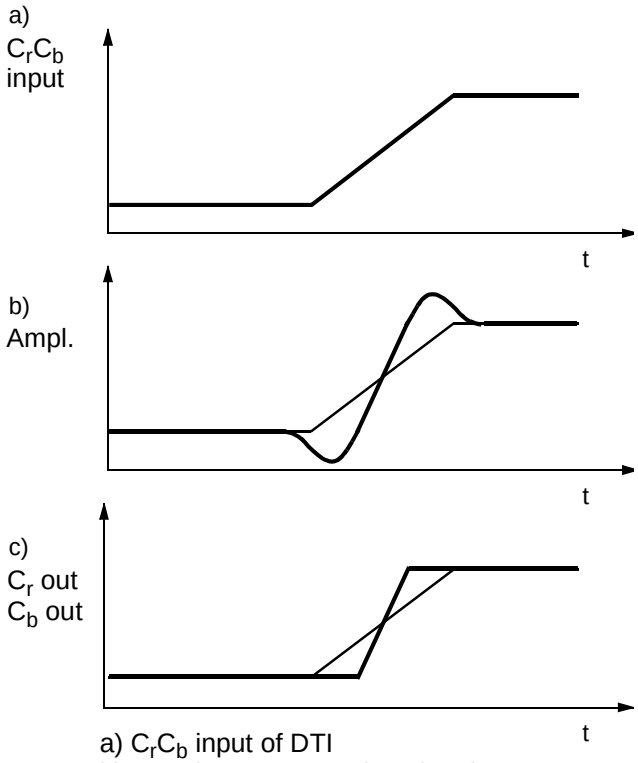


Fig. 2–4: Frequency response of the chroma 4:2:2 to 4:4:4 interpolation filter

2.1.8. Chroma Transient Improvement

The intention of this block is to enhance the chroma resolution. A correction signal is calculated by differentiation of the color difference signals. The differentiation can be selected according to the signal bandwidth, e.g. for PAL/NTSC/SECAM or digital component signals, respectively. The amplitude of the correction signal is adjustable. Small noise amplitudes in the correction signal are suppressed by an adjustable coring circuit. To eliminate “wrong colors”, which are caused by over and undershoots at the chroma transition, the sharpened chroma signals are limited to a proper value automatically.



a) C_rC_b input of DTI
b) C_rC_b input + correction signal
c) sharpened and limited C_rC_b

Fig. 2–5: Digital color transient improvement

2.1.9. Inverse Matrix and Digital RGB Processing

Six multipliers in parallel perform the matrix multiplication to transform the C_r and C_b signals to R–Y, B–Y, and G–Y. The initialization values for the matrix are computed from the standard ITU-R (CCIR) matrix:

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1{,}402 \\ 1 & -0{,}345 & -0{,}713 \\ 1 & 1{,}773 & 0 \end{bmatrix} \times \begin{bmatrix} Y \\ Cb \\ Cr \end{bmatrix}$$

The multipliers are also used to adjust color saturation and picture contrast. Since the multiplier allows ±4 as the biggest coefficient, it is possible that the product of CTM×SATM×MxxM will be clipped, which causes wrong colors. SATLIM limits the product of contrast times saturation to allow a maximum oversaturation. The matrix computes:

After adding the post-processed luma, the digital RGB signals are limited to 10 bits. Three multipliers are used to digitally adjust the white-drive and to implement an average beam current limiter. See also Section 2.2.4. “CRT Measurement and Control”.

$$\begin{bmatrix} R \\ G \\ B \end{bmatrix} = MIN\left[\left(\frac{CTM}{32} \times \frac{SATM}{32}\right), \frac{SATLIM}{32}\right] \times \frac{1}{64} \times \begin{bmatrix} MR1M & MR2M \\ MG1M & MG2M \\ MB1M & MB2M \end{bmatrix} \times \begin{bmatrix} Cb \\ Cr \end{bmatrix} + \left(\frac{CTM}{32} \times Y\right)$$

2.1.10. Picture Frame Generator

When the picture does not fill the total screen (height or width too small) it is surrounded with black areas. These areas (and more) can be colored with the picture frame generator. Another possibility is the insertion of a vertical and a horizontal stripe into the picture. This is done by switching over the RGB signal from the matrix to the signal from the frame color register.

The width of each area (left, right, upper, lower) can be adjusted separately. The generator starts on the right, respectively lower side of the screen and stops on the left, respectively upper side of the screen. This means, it runs during horizontal, respectively vertical flyback.The color of the complete border can be stored in a programmable frame color register. The format is 3×4 bit RGB. The contrast can be adjusted separately. If the start value for the generator is larger than the stop value, the picture frame is inserted at the borders. If the start value is smaller than the stop value a vertical or horizontal stripe is inserted.

2.1.11. Scan Velocity Modulation

Picture tubes equipped with an appropriate yoke can use the Scan Velocity Modulation signal to vary the speed of the electron gun during the entire video scan line depending on its content. Transitions from dark to bright will first speed up and then slow down the scan; vice-versa for the opposite transition (see Fig. 2–6).

The digital RGB input signal for the SVM is converted to Y in a simple matrix. Then the Y signal is differentiated by a filter of the transfer function $1-Z^{-N}$, where N is programmable from 1 to 6. With a coring some noise can be suppressed. This is followed by a gain adjustment and an adjustable limiter. The analog output signal is generated by an 8-bit D/A converter. The signal delay can be adjusted by ±3.5 clocks in half-clock steps in respect to the analog RGB output signals. This is useful to adjust the different group delays of analog RGB amplifiers to the one for the SVM yoke current.

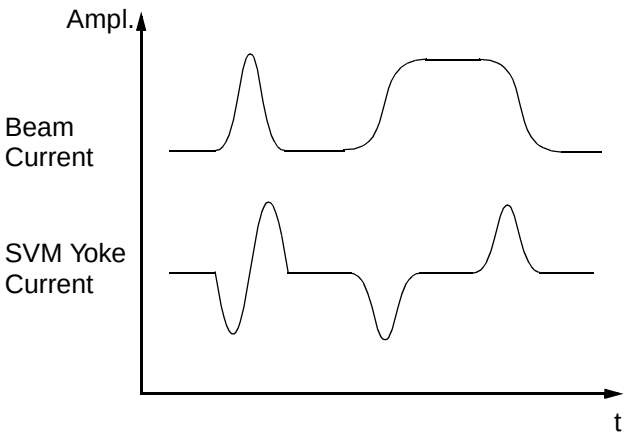


Fig. 2–6: SVM signal wave form

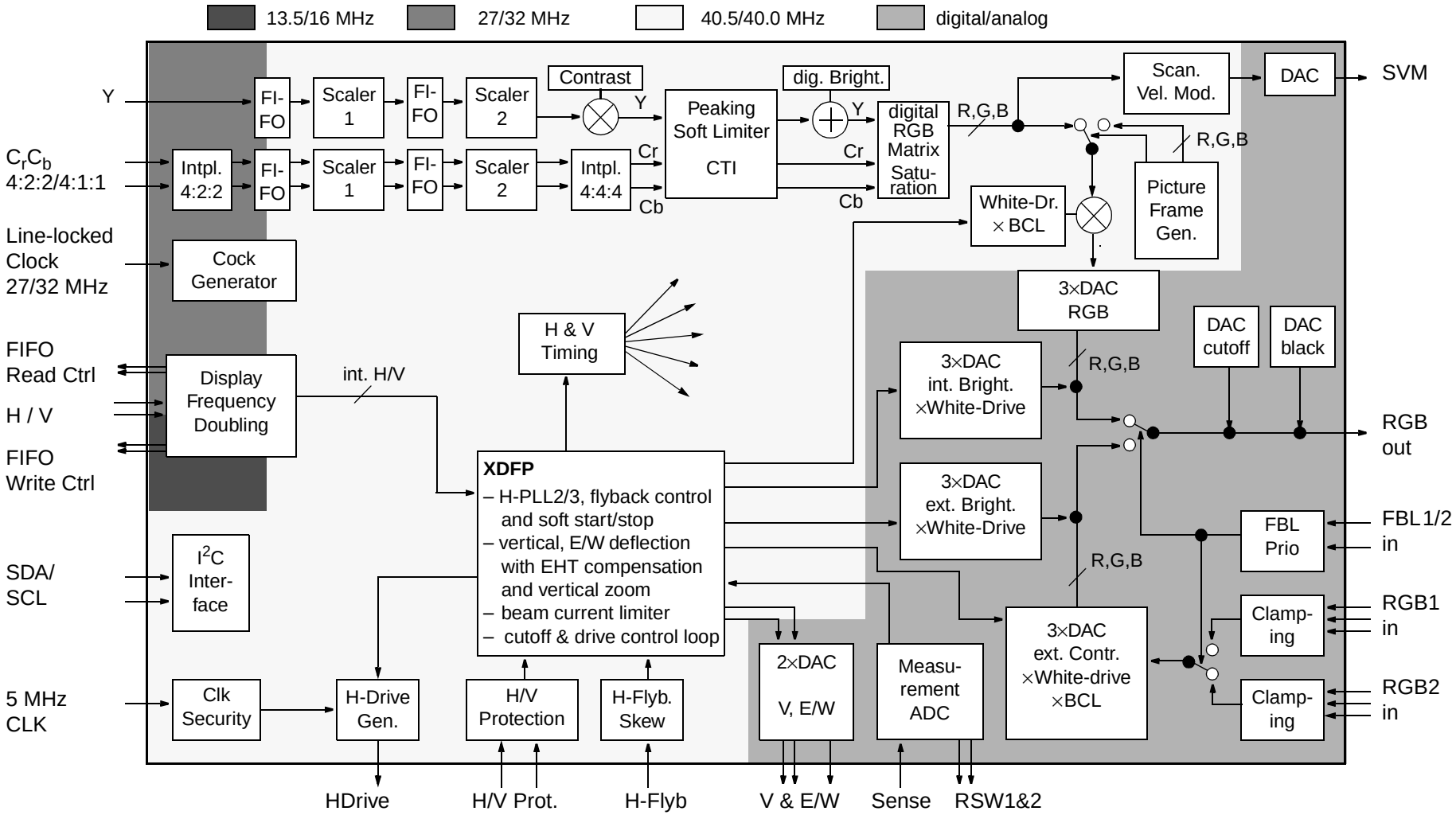


Fig. 2–7: Detailed block diagram of the DDP 3310B

2.2. Analog Back-End

The digital RGB signals are converted to analog RGB using three video digital to analog converters (DAC) with 10-bit resolution. The analog RGB-outputs are current outputs with current-sink characteristics. The maximum current drawn by the output stage is obtained with peak white RGB.

Each RGB signal has two additional DAC's with 9-bit resolution to adjust analog brightness (40 % of the full RGB range) and cutoff / black level (60 % of the full RGB range). An additional fixed current is applied for the blanking level.

In order to define accurate color on different CRT displays, you must exactly adjust what color the CRT phosphorous produces to display the color on screen. To have the same colors for the life of the display, a build-in automatic tube control loop checks and adjusts the black level on every field and white point every third field.

The back-end allows insertion of two external analog RGB signals. The RGB signals are key-clamped and inserted into the main RGB by the Fast-Blank switch. The external RGB signals can be adjusted independently as regarding DC-level (brightness) and magnitude (contrast). An external Half-Contrast signal can be used to reduce the output current of the internal RGB outputs to 50 %.

The controlling of the white-drive/analog brightness and also the external contrast and brightness adjustments is done via the internal processor.

2.2.1. Analog RGB Insertion

The DDP 3310B allows insertion of two external analog RGB signals. Each RGB signal is key-clamped and inserted into the main RGB by the Fast-Blank switch. The selected external RGB input can be overlaid or underlaid to the digital picture. The external RGB signals can be adjusted independently as regards DC level (brightness) and magnitude (contrast).

It depends on the Fast-Blank input signals and the programming of a number of I^2C-register settings which analog RGB input is selected. Both Fast-Blank inputs must be either active-Low or active-High.

All signals for analog RGB insertion (RIN1/2, GIN1/2, BIN1/2, FBLIN1/2, HCS) must be synchronized to the horizontal flyback, otherwise a horizontal jitter will be visible. The DDP 3310B has no means for timing correction of the analog RGB input signals.

Table 2–4: RGB Input Selection

Input Signals		I^2C Settings		Analog RGB Outputs
FBLIN1	**FBLIN2**	**FBPOL**	**FBPRIO**	
0	0	0	x	Video
0	1	0	x	RGB input 2
1	0	0	x	RGB input 1
1	1	0	0	RGB input 1
1	1	0	1	RGB input 2
0	0	1	0	RGB input 1
0	0	1	1	RGB input 2
0	1	1	x	RGB input 1
1	0	1	x	RGB input 2
1	1	1	x	Video

Note: with following I^2C settings
FBFOH1 = FBFOH2 = FBFOL1 = FBFOL2 = 0

2.2.2. Half-Contrast Control

Insertion of transparent text pages or OSD onto the video picture is often difficult to read, especially if the video contrast is high. The DDP 3310B allows contrast reduction of the video background by means of a Half-Contrast input (HCS pin). This input can be supplied with a fast switching signal (similar to the Fast-Blank input), typically defining a rectangular box in which the video picture is displayed with reduced contrast. The analog RGB inputs are still displayed with full contrast.

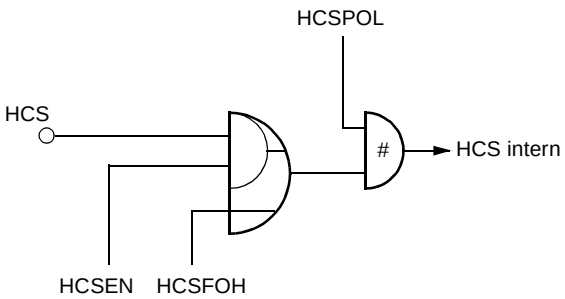


Fig. 2–8: Half-Contrast switch logic

2.2.3. Fast-Blank Monitor

The presence of external analog RGB sources can be detected by means of a Fast-Blank monitor. The status of the selected Fast-Blank input can be monitored via an I^2C register. There is a 2-bit information, giving static and dynamic indication of a Fast-Blank signal. The static bit is directly reading the Fast-Blank input line, whereas the dynamic bit is reading the status of a flip flop triggered by the negative edge of the Fast-Blank signal.

With this monitor logic it is possible to detect if there is an external RGB source active and if it is a full-screen insertion or only a box. The monitor logic is connected directly to the FBLIN1 or FBLIN2 pin. Selection is done via I^2C register.

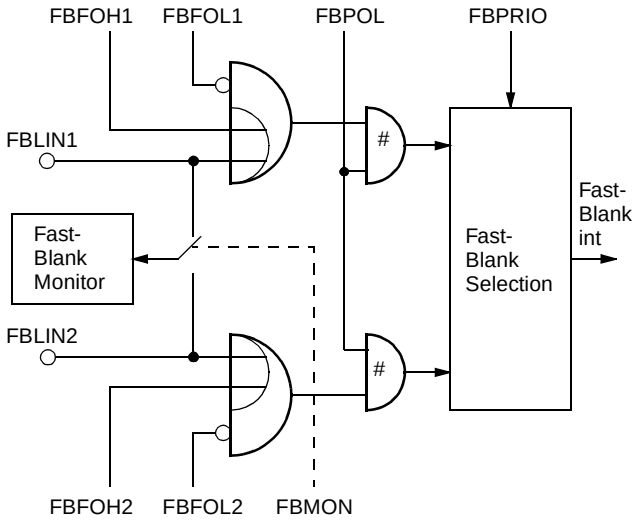


Fig. 2–9: Fast-Blank selection logic

2.2.4. CRT Measurement and Control

The display processor is equipped with an 8/12-bit PDM-ADC for all picture tube measuring purposes. This MADC is connected to the SENSE input pin, the input range is 0 to 1.6V.

Cutoff and white-drive current measurement are carried out with 8-bit resolution during the vertical blanking interval. The current range for cutoff measurement is set by connecting the resistor R1 to the SENSE input. Due to the fact of a 1:10 relation between cutoff and white-drive current, the range select 2 output (RSW2) becomes active for the white-drive measurement and connects R3 in parallel to R1, thus determining the correct current range. During the active picture, the MADC is used for the average beam current limiter with a 12-bit resolution. Again, a different measurement range is selected with active range select 1&2 outputs (RSW1&RSW2) connecting R2 in parallel to R3 and R1. See Fig. 2–10 and Fig. 2–11 for the corresponding timing. These measurements are typically done at the summation point of the picture tube cathode currents.

Another method uses two different current measurements. The range switch 1 pin (RSW1) can be used as a second Sense input, selectable by software. In this case, the cutoff and white-drive currents are measured as before at the SENSE input. The active picture measurement can be done with the second Sense input (RSW1). The signal may come (via a proper interface) from the low end of the EHT coil (CRT anode current). In this case, the resistor R2 in Fig. 2–10 has to be removed.

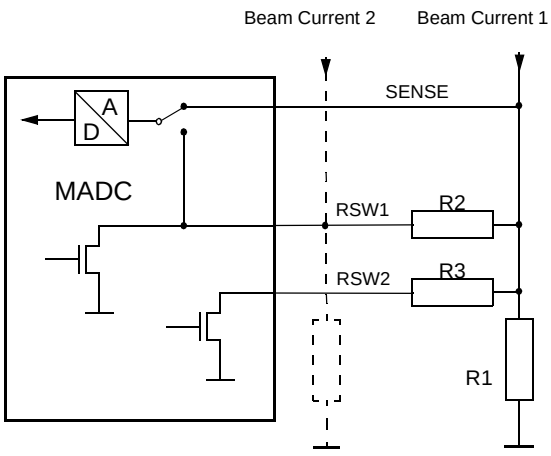


Fig. 2–10: MADC range switch

The picture tube measurement returns results on every field for:

– cutoff R

– cutoff G

– cutoff B

– white-drive R or G or B (sequentially)

Thus, a cutoff control cycle for RGB requires one field only while a complete white-drive control cycle requires three fields. During cutoff and white-drive measurement the average beam current limiter function (see Section 2.2.5.) is switched off. The amplitude of the cutoff and white-drive measurement lines can be programmed separately with IBRM and WDRM (see Fig. 2–11). The start line for the tube measurement (cutoff red) can be programmed via I^2C-bus (TML).

The built-in control loop for cutoff and white-drive can operate in three different modes selected by CUT(WDR)_GAIN and CUT(WDR)_DIS.

– The user control mode is selected by setting CUT(WDR)_GAIN = 0. In this mode the registers CUT(WDR)_R/G/B are used as direct control values for cutoff and drive using the whole 9-bit range. If the measurement lines are enabled (CUT(WDR)_DIS = 0) the user can read the measured cutoff & white drive values in the CUTOFF(WDRIVE)_R/G/B registers. An external software can now control the settings of the CUT(WDR)_R/G/B registers.

– The automatic mode is selected by setting CUT(WDR)_GAIN > 0 and CUT(WDR)_DIS = 0. In this mode, the registers CUT(WDR)_R/G/B are used as reference for the measured values (CUTOFF(WDRIVE)_R/G/B). Due to the 8-bit resolution of the ADC, only 8 LSB can be used as reference values. The calculated error is used with a small hysteresis (1,5 %) to adjust cutoff and drive. The higher the loop gain (CUT(WDR)_GAIN), the smaller the time constant for the adjustment.

– If the automatic mode was once enabled (CUT(WDR)_GAIN > 0), the control loop can be stopped by setting CUT(WDR)_DIS = 1. In this mode, the calculated cutoff and drive values will no longer be modified and the measurement lines are suppressed. Changes of the reference values (CUT(WDR)_R/G/B) have no effect.

If one of the calculated red, green, or blue white-drive values exceeds its maximal possible value (WDR_R/G/B>511), the white balance gets misadjusted. An automatic drive saturation avoidance prevents from this effect (WDR_SAT = 1) from occurring. If one drive value exceeds the maximum allowed threshold (MAX_WDR), the amplitude of the white-drive measurement line will be increased and decreased if one of them goes below the fixed threshold 475.

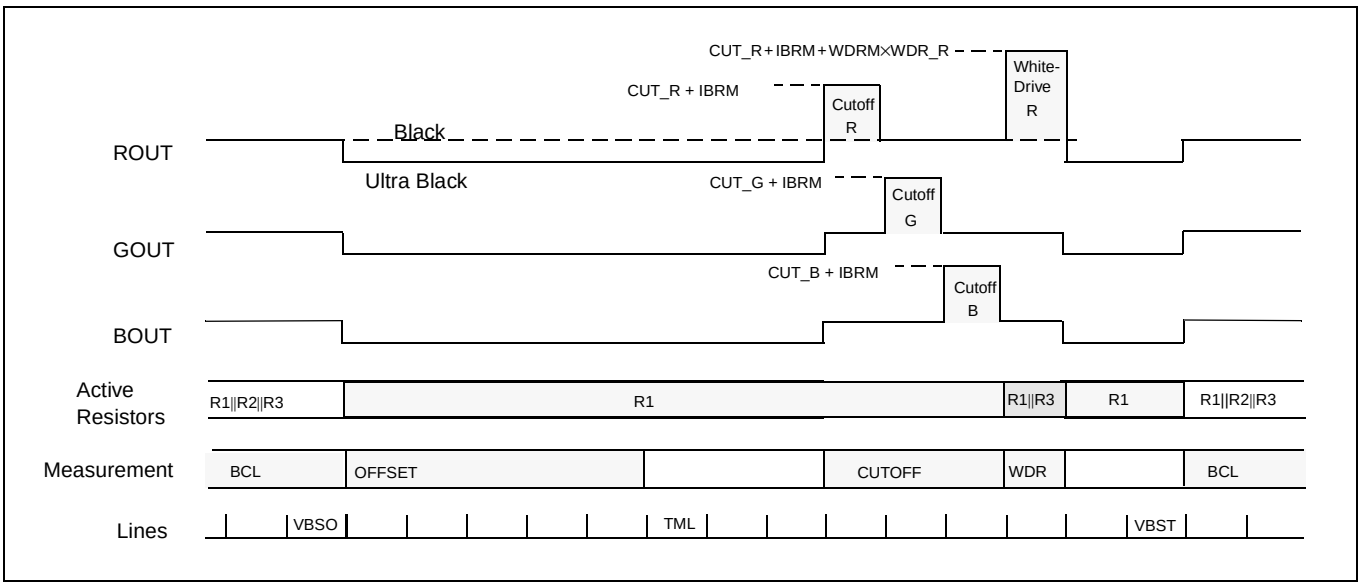


Fig. 2–11: MADC measurement timing

2.2.5. Average Beam Current Limiter

The average beam current limiter (BCL) works on both the digital YUV input and the inserted analog RGB signals by using either the sense input or the RSW1 input for the beam current measurement. The BCL uses a different filter to average the beam current during the active picture resulting in a 12-bit resolution. The filter bandwidth is approximately 4 kHz.

The beam current limiter allows the setting of a threshold current, a gain and an additional time constant. If the beam current is above the threshold, the excess current is low-pass filtered with the according gain and time constant. The result is used to attenuate the RGB outputs by adjusting the white-drive multipliers for the internal (digital) RGB signals and the analog contrast multipliers for the analog RGB inputs, respectively. The lower limit of the attenuator is programmable, thus a minimum contrast can always be set. If the minimum contrast is reached, the brightness will be decreased down to a programmable minimum as well. Typical characteristics of the BCL for different loop gains are shown in Fig. 2–12; for this example the tube has been assumed to have square-law characteristics.

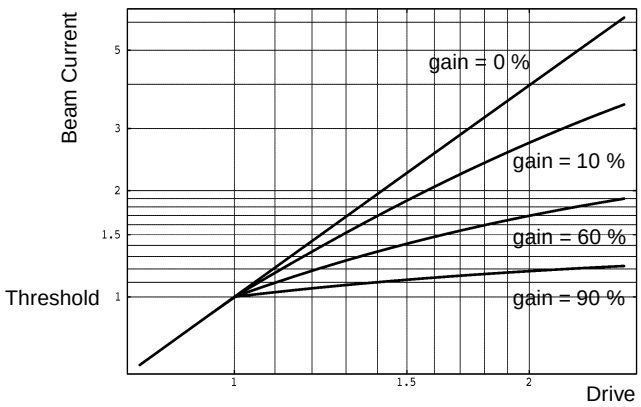


Fig. 2–12: Beam current limiter characteristics: beam current output vs. drive

2.3. Synchronization and Deflection

2.3.1. Deflection Processing

The deflection processing generates the signals for the horizontal and vertical drive (see Fig. 2–13). This block contains two numeric phase-locked loops and a security unit:

– PLL2 generates the horizontal and vertical timing, e.g. blanking, clamping, and sync signals. Phase and frequency are synchronized by the incoming sync signals.

– PLL3 adjusts the phase of the horizontal drive pulse and compensates for the delay of the horizontal output stage.

– The security unit observes the H-Drive output signal. With an external 5-MHz reference clock, this unit controls the H-Drive “off time” and period. In case of an incorrect H-Drive signal the security unit generates a free-running H-Drive signal divided down from the 5-MHz reference clock.

The DDP 3310B is able to synchronize various horizontal frequencies, even VGA frequencies. Allowed horizontal frequencies are listed in Table 2–5. The horizontal drive uses a high-voltage (8 V) open-drain output transistor.

2.3.2. Security Unit for H-Drive

The security unit observes the H-Drive output signal with an external 5-MHz reference clock. For different horizontal frequencies the security unit uses different ranges to control the H-Drive signal. Selecting a specific horizontal frequency via I^2C-register HFREQ automatically switches to the corresponding security range. The control ranges are listed in Table 2–5.

The window of the control range has to fit into a main control window which is selectable with the FREQSEL input pin. With a Low signal at this pin, the main control range is 28.8…34.4 µs and with a High signal, the main control range is 25.6…29.2 µs. This is to prevent malfunctions if the horizontal deflection stage is prepared for VGA frequencies.

The Horizontal Drive Output can be forced to the High level during Flyback. This means, the falling edge of the drive pulse occurs at the earliest to the end of the flyback pulse. This function can be enabled via the I^2C bus (EFLB).

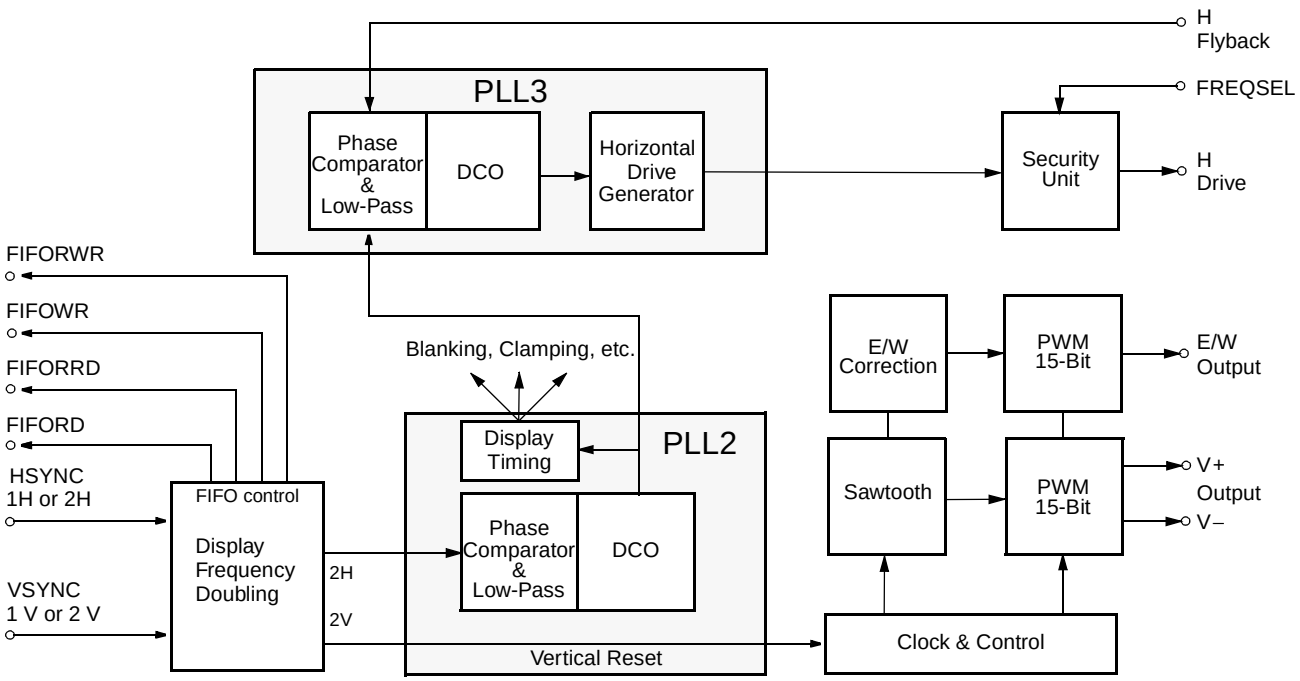


Fig. 2–13: Deflection processing block diagram

2.3.3. Soft Start/Stop of Horizontal Drive

In order to increase the energy supply of the horizontal deflection stage smoothly, a soft start decreases the drive frequency from 55 kHz to 31.25 kHz within 85 ms. The High time t_H is always 14.4 µs. This means, the duty factor decreases from 79.2 % to 45 % (see Fig. 2–14).

The soft stop is needed, when the protection circuitry wants to turn off the H-Drive. It has the inverse behavior of the soft start and ends with a High level at the HOUT Pin.

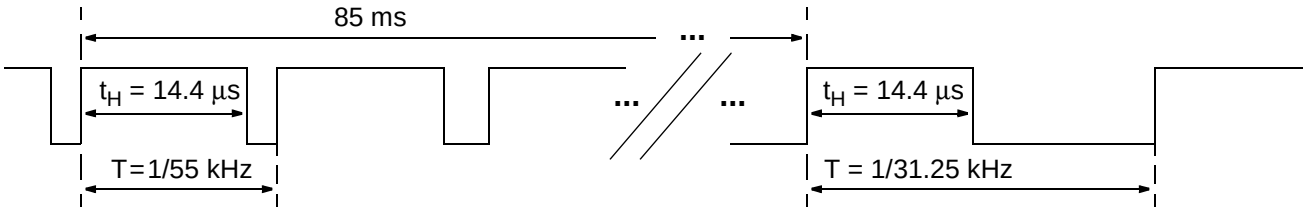


Fig. 2–14: Soft start with a duty factor of 14.4/32

Table 2–5: Allowed Horizontal Frequencies

Supply Clock (MHz)	Pixels per Line Supply Clk	Main Clock (in MHz)	Pixels per line Main Clk	Horizontal Frequency (Hz)	Minimum H-Drive Period (in µs)	Maximum H-Drive Period (in µs)	HFREQ (I^2C)
27	864	40.5	1296	31.24968	29.60	34.40	000
27	858	40.5	1287	31.46853	29.60	34.40	010
27	800	40.5	1200	33.750	28.80	30.60	100
27	768	40.5	1152	35.15625	27.80	29.20	001
27	720	40.5	1080	37.500	25.60	28.00	101
27	712	40.5	1068	37.92135	25.60	28.00	110
32	1024	40.0	1280	31.24952	29.60	34.40	000
32	944	40.0	1180	33.89776	28.80	30.60	100
32	912	40.0	1140	35.08747	27.80	29.20	001
32	852	40.0	1065	37.55869	25.60	28.00	101
32	844	40.0	1055	37.91469	25.60	28.00	110
40.5	1296	40.5	1296	31.24968	29.60	34.40	000

2.3.4. Horizontal Phase Adjustment

This section describes a simple way to get a correct horizontal frame position and clamp window for analog RGB insertion.

1. For a correct scaler function in panorama/waterglass mode, the digital input data should be centered to the active video input signal.
2. The clamping pulse for analog RGB insertion can be adjusted to the pedestal of the input signal with POFS2.
3. The horizontal raster position of the analog inserted RGB1/2 signal can be set to the desired frame position with POFS3.
4. The horizontal position of the digital RGB signal can be shifted to the left and right with NEWLIN. Following values allowed in respect to POFS2:
   – 90 < (POFS2+NEWLIN) – (Clk×SFIF) < 580
   – Clk = 3 @ LLC2 = 27 MHz
   – Clk = 2.5 @ LLC2 = 32 MHz
5. Now the positioning of horizontal blanking and the picture frame generator can be done.

2.3.5. Vertical Synchronization

The number of lines per field can be adjusted by software (LPFD). This number is used to calculate the vertical raster. The DDP synchronizes only to a vertical sync within a programmable detection window (LPFD ± VSYNCWIN). If there is no vsync, the DDP runs with maximum allowed lines and if the vertical frequency is to high, it runs with minimum allowed lines. The smaller the detection window, the slower the DDP gets synchronized to the incoming vertical sync. In case of an interlaced input signal, it is possible to display both fields at the same raster position by setting R_MODE to 1 or 2.

An automatic field length adaptation can be selected (VA_MODE). In this case, the vertical raster will be calculated according to the counted number of lines per field instead from LPFD. This is useful for video recorder search mode when the number of lines per field does not comply with the standard, or if you want to use a common value of LPFD for PAL and NTSC (e.g.: LPFD = 290; VSYNCWIN = 54).

2.3.6. Vertical and East/West Deflection

The calculations of the Vertical deflection and East/West correction waveforms are done in the internal processor. They are described as polynomials in x, where x varies from –0.5×zoom to +0.5×zoom for one field. For zoom>1 the range is limited between –0.5 and +0.5.

The vertical deflection waveform is calculated as follows (without EHT compensation):

$$V = vpos + ampl \cdot (x + lin \cdot x^2 + scorr \cdot x^3)$$

– VPOS defines the vertical raster position
– AMPL is the vertical raster amplitude (zoom≥1)
– LIN is the linearity coefficient
– SCORR is the coefficient for S-correction

The vertical sawtooth signal will be generated from a differential current D/A converter and can drive a DC coupled power stage. In order to get a faster vertical retrace timing, the output current of the vertical D/A-converter can be increased during the retrace for a programmable number of lines (FLYBL). The range between the end of the flyback and the beginning of the raster is also programmable (HOLDL).

The East/West deflection waveform, generated from a single-ended D/A converter, is given with the equation:

$$E/W = width + tcorr \cdot x + cush \cdot x^2 + corner \cdot x^4$$

– WIDTH is a DC value for the picture width
– TCORR is the trapezoidal correction
– CUSH is the pincushion correction
– CRNU is the upper corner correction
– CRNL is the lower corner correction

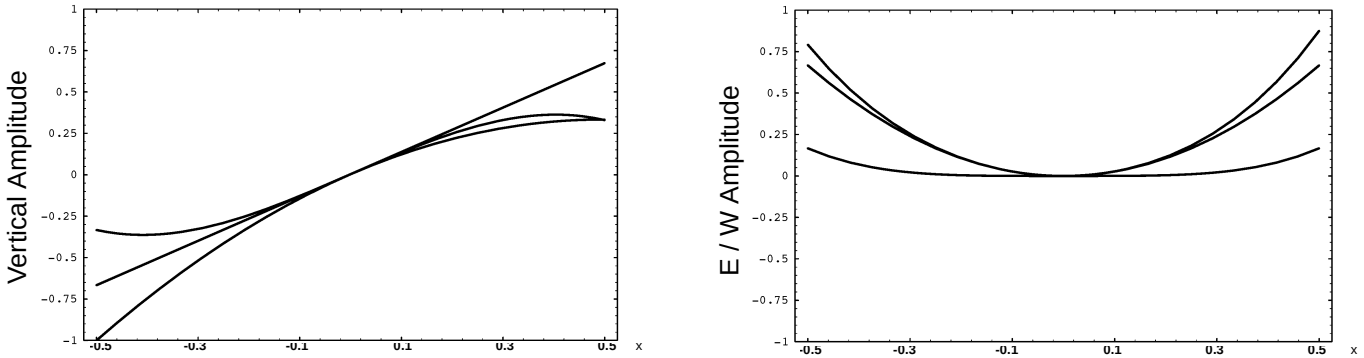


Fig. 2–15: Vertical and East/West deflection waveforms

2.3.7. Vertical Zoom

With vertical zoom, the DDP 3310B is able to display different aspect ratios of the source signal on tubes with 4:3 or 16:9 aspect ratio by adapting the corresponding raster.

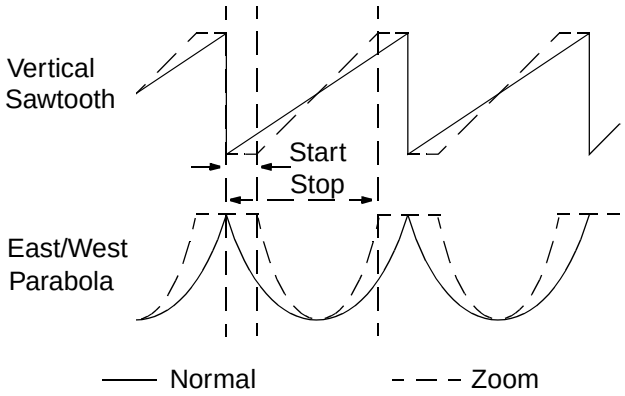


Fig. 2–16: Vertical zoom

2.3.8. EHT Compensation

The vertical deflection waveform can be scaled according to the average beam current. This is used to compensate the effects of electric high-tension changes due to beam current variations. EHT compensation for East/West deflection is done with an offset corresponding to the average beam current. The time constant of this process is freely programmable with a resolution of 18 bit. Both corrections can be enabled separately. The maximum scaling coefficient for vertical deflection is 1±x and the maximum offset for East/West is y, where x, y are adjustable from 0 to 0.25. The horizontal phase at the output HOUT can be influenced according to the average beam current in a range of ±1.5 µs.

2.3.9. Protection Circuitry

Picture tube and drive stage protection is provided through the following measurements:

– Vertical protection input: this pin watches the vertical sawtooth signal. In every field the sawtooth must descend below the lower threshold A and ascend above the upper threshold B. In this case the protection flag is set (sawtooth o.k.). If an error occurs the protection flag is cleared.
After approx. 10 fields with cleared flag, the RGB drive signals are blanked. The blanking is cancelled if the flag is set for 40 fields (see Fig. 2–17).

– Drive shutoff during flyback: this feature can be selected by software (EFLB)

– Safety input pin: This pin has two thresholds. The applied signal has to meet the following conditions:

1. threshold B must not be overshot
2. threshold A has to be exceeded permanently or at least once per line

otherwise the RGB signals are blanked . Both thresholds have a small hysteresis.

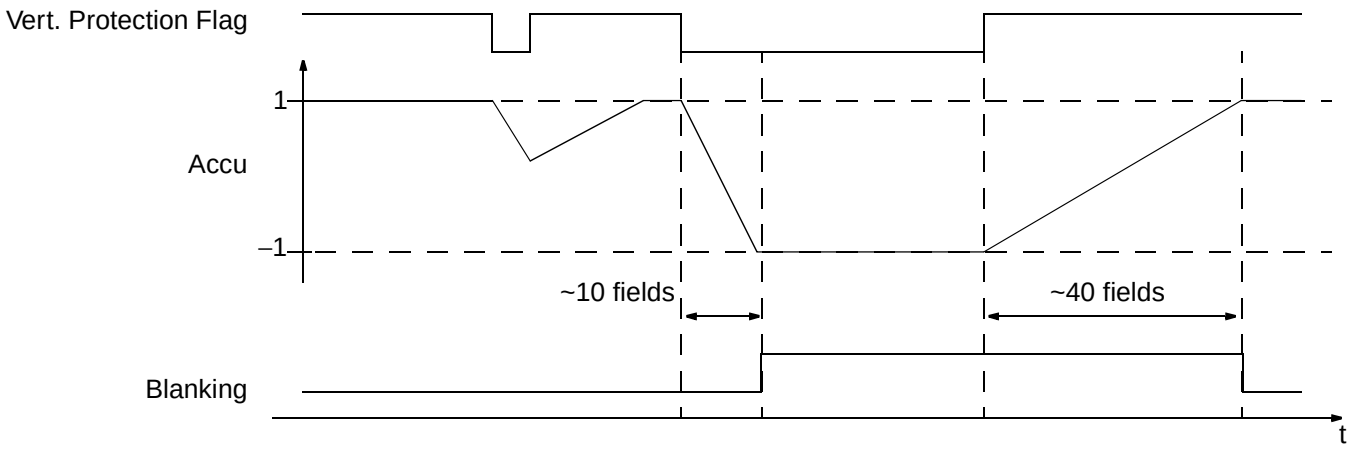


Fig. 2–17: Protection timing

2.3.10. Display Frequency Doubling

The DDP 3310B handles single or double vertical and horizontal input frequencies. The Display Frequency Doubling is used when single H/V frequencies are applied and a FIFO for video frequency doubling is used. In this mode it is mandatory to supply an active video signal to the HS pin, which is not vertical blanked.

Three different raster modes are selectable via I2C bus:

A A‘ B‘ B (reduced line flicker)
A A B B (improved vertical resolution)
A A B‘ B‘ (non-interlaced)

A/B means field A/B in original raster position and A‘/B‘ means field A/B in the opposite raster position.

A minimum field length filter can be switched on (DFD-FILT) to write only the smallest field length of the past up to four fields into the memory. This prevents read-before-write errors in signals with a strong changing field length (e.g. VCR signals).

2.3.11. General-purpose D/A Converter

There are two D/A converters realized as pulse width modulators. The resolution is 8 bit and the clock frequency is 20.25 MHz. The outputs are push-pull types. For a ripple-free output voltage, a first-order low-pass filter with a corner frequency <120 Hz should be applied. The D/A converters will be adjusted via I^2C-bus. They can be used to adjust two DC voltages, for example for horizontal raster position, raster tilt, or just as switching outputs when the values 0 and 255 are selected.

2.3.12. Clock and Reset

The DDP 3310B has the capability to accept different line-locked clock rates: 27, 32, and 40.5 MHz.This external clock rate is converted internally to a clock rate of 40.5 or 40 MHz by means of a PLL. Selection of external clock frequency is done with pins CM1 and CM0. See Table 2–6 for clock frequency selection. To ensure lock of PLL a reset pulse of at least 500 µs must be applied after power-up.

Table 2–6: Clock Frequency Selection

CM1	CM0	LLC2
0	0	27 MHz
0	1	32 MHz
1	0	40.5 MHz

2.3.13. Reset and Power-On

The IC has its own voltage supervision to generate an internal reset during power on or when the supply voltage (VSUPD) goes below ~4.5V. Also, a clock supervision of the 5-MHz clock keeps the internal reset active until a proper clock signal is detected (e.g. three clock cycles with the correct period). When the reset pin RESQ or the internal reset becomes active, all counters and registers are set to zero. When the reset pins are released, the internal reset is still active for approximately 4 µs. Then all registers are loaded with their default values listed in Table 3–3. This initialization takes about 100 µs. During and after reset, the HOUT signal remains High until a soft start (see Section 2.3.3.) will be performed by setting RAMP_EN.

3. Serial Interface

3.1. I²C-Bus Interface

Communication between the DDP 3310B and the external controller is done via I²C-bus. The DDP 3310B has an I²C-bus slave interface and uses I²C clock synchronization to slow down the interface if required.

Basically, there are two classes of registers in the DDP 3310B:

1. The first class are directly addressable I²C registers. They are embedded in the hardware. These registers are 8 or 16 bit wide.
2. The second class are “XDFP-REGISTERS”, which are used by the “XDFP” on-chip controller. These registers are all 16 bit wide and read- and writable. Communication with these registers requires I²C packets with a 16-bit XDFP-register address and 16-bit data.

Communication with both classes of registers (I²C and XDFP-REGISTERS) are performed via I²C; but the format of the I²C telegram depends on which type of register is being accessed.

The I²C-bus chip address of the DDP 3310B is given below:

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	1	0	1	1/0

3.2. I²C Control and Status Registers

The I²C-bus interface uses one level of subaddress. First, the bus address selects the IC, then a subaddress selects one of the internal registers. They have 8- or 16-bit data size; 16-bit registers are accessed by reading/writing two 8-bit data words.

– Writing is done by sending the device address first followed by the subaddress byte and one or two data bytes.

– For reading, the read address has to be transmitted first by sending the device write address, followed by the subaddress, a second start condition with the device read address, and reading one or two bytes of data.

Fig. 3–2 shows I²C protocol for read and write operations; the read operation requires an extra start condition and repetition of the chip address with read command set. Table 3–2 gives definitions of the I²C control and status registers.

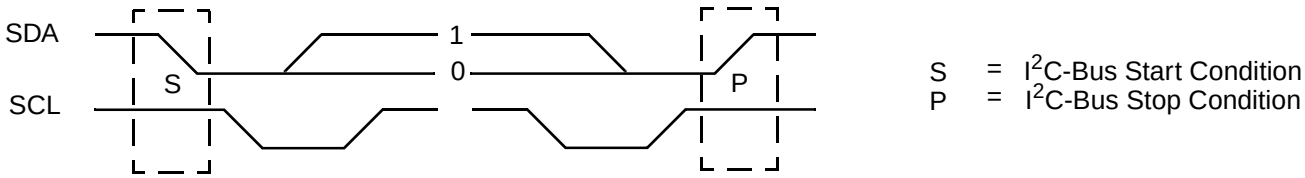


Fig. 3–1: I²C-Bus protocol (MSB first, data must be stable while clock is High)

Write to I²C Control Register :

S	1000 101	W	Ack	Sub-Addr.	Ack	1- or 2-Byte Data	Ack	P

Read from I²C Control Register :

S	1000 101	W	Ack	Sub-Addr.	Ack	S	1000 101	R	Ack	High-Byte Data	Ack	Low-Byte Data	Nak	P

W = 0 (Write Bit)
R = 1 (Read Bit)

S = Start Condition
P = Stop Condition

Ack = 0 (Acknowledge Bit from DDP 3310B = gray or controller = hatched)
Nak = 1 (Not Acknowledge Bit from controller = hatched or indicating an error state from DDP 3310B = gray)

Fig. 3–2: I²C-Bus protocol

3.3. XDFP Control and Status Registers

The second class are “XDFP-REGISTERS”, which are used by the XDFP on-chip controller. Access to these registers is achieved by subaddressing.

– Writing to these registers is done by sending the device write address first, followed by the XDFP-write subaddress, two address bits for the desired XDFP-register, and the two data bytes.

– For reading, the XDFP-register address has to be transmitted first by sending the device write address, followed by the XDFP-read subaddress and the two XDFP-register address bytes. Without sending a stop condition, reading of the addressed data is done by sending the device read address and reading two bytes of data.

Fig. 3–3 shows I^2C protocol for read and write operations. Table 3–3 gives definitions of the XDFP control and status registers. If these registers are smaller than 16 bit, the remaining bits should be 0 on write and read operations. Due to the internal architecture, the IC cannot react immediately to an I^2C request, which interacts with the on-chip controller. The maximum response timing is approximately 20 ms. If the addressed controller is not ready for further transmissions on the I^2C-bus, the clock line SCL is pulled low. This puts the current transmission into a wait state. After a certain period of time, the clock line will be released and the interrupted transmission is carried on.

A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in Table 3–3.

Table 3–1: XDFP read/write address

XDFP Read address	h’13
XDFP Write address	h’12

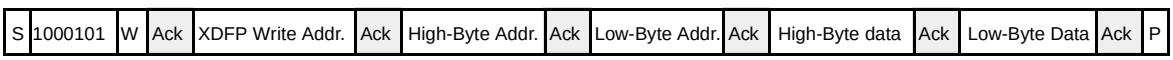
The register modes are

8/16- bit width
r read only register
w write only register
r/w write/read data register

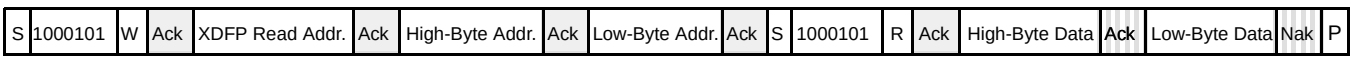
Note: set unused bits to ‘0‘!

The mnemonics used in the DDP 3310B demo software are given in the last column.

Write to XDFP Control Register:



Read from XDFP Control Register:



W = 0 (Write Bit)
R = 1 (Read Bit)

S = Start Condition
P = Stop Condition

Ack = 0 (Acknowledge Bit from DDP 3310B=gray or Controller = hatched)
Nak = 1 (Not Acknowledge Bit from Controller=hatched or indicating an error state from DDP 3310B=gray)

Fig. 3–3: XDFP protocol

Table 3–2: I²C Control Registers

I²C Control and Status Registers					
Subaddr.	**Mode**	**Function**		**Default**	**Name**
XDFP INTERFACE					
h'13	16-w	XDFP read address			DFPRD
		bit[[9:0]	10-bit XDFP RAM address		
		bit[15:10] 0	reserved, set to zero		
h'12	16-w	XDFP write address			DFPWR
		bit[[9:0]	10-bit XDFP RAM address		
		bit[15:10]	reserved, set to zero		
ANALOG FAST-BLANK MONITOR					
h'1E	8-r	Fast-Blank signal status			FBLSTAT
		bit[0] 0/1	FBLIN level Low/High		FBLEV
		bit[1]	FBLIN slope: 1 = falling edge occurred		FBSLO
		bit[7:2]	not used		
h'11	16-r/w	picture frame color, 12 bit wide			PFC
		bit[3:0] 0..15	blue amplitude	0	PFCB
		bit[7:4] 0..15	green amplitude	0	PFCG
		bit[11:8] 0..15	red amplitude	0	PFCR
		bit[15:12] 0	not used	0	
OUTPUT PINS					
h'10	8-r/w	output pin configuration			PSTR
		bit[2:0]	pin driver strength, FIFO control 7 = output tristate 6 = minimum strength 0 = maximum strength	0	PSTSY
		bit[3] 0/1	strong/weak driver strength PWM1	0	PSTPR1
		bit[4] 0/1	strong/weak driver strength PWM2	0	PSTPR2
		bit[5] 0/1	disable/enable internal resistor for vertical and East/West drive output	0	VEWXR
		bit[6] 0/1	High/Low-active horizontal flyback input	0	FLYPOL
		bit[7] 0/1	disable/enable following I/O pin: FIFO -controll signals, PWM1&2, HCS, R/G/BIN2, and VS2.	0	OSDOFF

Table 3–3: Control Registers of the XDFP

XDFP Control and Status Registers				
Subaddr.	**Mode**	**Function**	**Default**	**Name**
		INPUT FORMATTER		
h'1B0	16-r/w	Input format		INFMT
		bit [0] 0/1 4:2:2 / 4:1:1 mode	1	M411
		bit [1] 0/1 binary offset / 2's complement	1	COB
		bit [2] 0/1 enable / disable blanking to black (for luma and chroma input when HS = 0)	1	BLNK
		bit [4:3] 0...3 select color multiplex	0	CMUX
		SCALER CONTROL REGISTER		
h'1C1	16-r/w	scaler mode register	0	SCMODE PANO
		bit[1:0] scaler mode 0 linear scaling mode 1 non-linear scaling mode, 'panorama' 2 non-linear scaling mode, 'waterglass' 3 reserved		
		bit[2] reserved, set to 0		
		bit[13:3] reserved, set to 0		
		bit[14] 0 scaler update command, set to 1 to update only scaler mode register	0	SCMODUP
		bit[15] 0 scaler update command, set to 1 to update all scaler control registers	0	SCUPDATE
h'1C2	16-r/w	active video length for 1-h FIFO	720	FFLIM
		bit[11:0] 0...1295 length in pixels 720 LLC mode (864/h)		
h'1C3	16-r/w	scaler1 coefficient; this scaler compresses the signal.	1024	SCINC1
		bit[11:0] 1024..4095 compression by a factor c, the value c*1024 is required		
h'1C4	16-r/w	scaler2 coefficient; this scaler expands the signal.	682	SCINC2
		bit[11:0] 256..1024 expansion by a factor c, the value 1/c*1024 is required		
h'1C5	16-r/w	bit[11:0] 0...4095 scaler1/2 non-linear scaling coefficient	0	SCINC
h'1C6 ... h'1CA	16-r/w	scaler1 window controls (see Table 3–4)	0 ... 0	SCW1_1 ... SCW1_5
		bit[11:0] 0...4095 5 registers for control of the non-linear scaling		
h'1CB ... h'1CF	16-r/w	scaler2 window controls (see Table 3–4)	0 ... 0	SCW2_1 ... SCW2_5
		bit[11:0] 0...4095 5 registers for control of the non-linear scaling		

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
CHROMA CHANNEL						
h'1AF	16-r/w	luma/chroma matching delay				CRCTRL
		bit [2:0]	–2...2	variable chroma delay	0	CDEL
		bit [3]		not used, set to "0"	0	
		bit [4]	0/1	C_B (U) sample first / C_R (V) sample first	0	ENVU
		bit [5]		not used, set to "0"		
h'1AB	16-r/w	digital transient improvement				DTICTRL
		bit [3:0]	0..15	coring value	1	DTICO
		bit [7:4]	0..15	DTI gain	5	DTIGA
		bit [8]	0/1	narrow/wide bandwidth mode	1	DTIMO
LUMA CHANNEL						
h'1B1	16-r/w	bit [14:9]	0..63	picture contrast in steps of 1/32	32	CTM
h'19A	16-r/w	bit [8:0]	–256..255	luma DC-offset	0	BRM
h'1AA	16-r/w	luma peaking filter, the gain at high frequencies and small signal amplitudes is: 1 + (k1+k2)/8				PK1
		bit [3:0]	0..15	k1: peaking level undershoot	4	PKUN
		bit [7:4]	0..15	k2: peaking level overshoot	4	PKOV
		bit [8]	0/1	peaking value normal/inverted (peaking/softening)	0	PKINV
h'1AE	16-r/w	luma peaking filter, coring				PK2
		bit [4:0]	0..31	coring level	3	COR
		bit [7:5]		peaking reduction	0	PKRD
			000	100 %		
			001	80 %		
			01x	60 %		
			100	50 %		
			101	40 %		
			11x	30 %		
		bit [8]	0/1	peaking filter center frequency High/Low	0	PFS
h'18A	16-r/w	luma soft limiter, slope A and B				LSLS
		bit [3:0]		slope segment A	0	LSLSA
		bit [7:4]		slope segment B	0	LSLSB
h'18E	16-r/w	luma soft limiter, limit A				LSLA
		bit [7:0]		luma soft limiter absolute limit (unsigned)	255	LSLAL
		bit [8]	0/1	modulation off/on (resolution enhancement)	0	LSLM
h'192	16-r/w	luma soft limiter, limit B			300	LSLTB
		bit [8:0]		luma soft limiter segment B tilt point (unsigned)		
h'196	16-r/w	bit [8:0]		luma soft limiter segment A tilt point (unsigned)	250	LSLTA

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
INVERSE MATRIX						
h'1B9 h'1B8	16-r/w	picture matrix coefficient R–Y = MR1M/64*C_B + MR2M/64*C_R				
		bit [15:7]	–256... 255		0	MR1M
		bit [15:7]	–256... 255		86	MR2M
h'1B7 h'1B6	16-r/w	picture matrix coefficient G–Y = MG1M/64*C_B + MG2M/64*C_R				
		bit [15:7]	–256... 255		–22	MG1M
		bit [15:7]	–256... 255		–44	MG2M
h'1B5 h'1B4	16-r/w	picture matrix coefficient B–Y = MB1M/64*C_B + MB2M/64*C_R				
		bit [15:7]	–256... 255		113	MB1M
		bit [15:7]	–256... 255		0	MB2M
h'1B2	16-r/w	bit [15:9]	0...63 –1	picture saturation in steps of 1/32; reserved mode to use old MATRIX coefficients and CTM addresses from B1	–1	SATM
h'1B3	16-r/w	bit [14:8]	0...127	limit for picture contrast × saturation in steps of 1/32	80	SATLIM
PICTURE FRAME GENERATOR						
h'197	16-r/w	picture frame insertion contrast R (amplitude range:0 to 255)				
		bit [7:4]	0..13 14,15	R amplitude = PFCR · (PFRCT + 4) invalid	8	PFRCT
h'193	16-r/w	picture frame insertion contrast G (amplitude range:0 to 255)				
		bit [7:4]	0..13 14,15	G amplitude = PFCG · (PFGCT + 4) invalid	8	PFGCT
h'18F	16-r/w	picture frame insertion contrast B (amplitude range:0 to 255)				
		bit [7:4]	0..13 14,15	B amplitude = PFCB · (PFBCT + 4) invalid	8	PFBCT
h'1D5	16-r/w	bit [10:0]	0...1295 0 7FF	horizontal picture frame begin (see Table 2–5 for max. pixels per line) horizontally disabled full frame	0	PFGHB
h'1D6	16-r/w	bit [10:0]	0...1295	horizontal picture frame end (see Table 2–5 for max. pixels per line)	0	PFGHE
h'1AC	16-r/w	bit [8:0]	0...511 0	vertical picture frame start line (+128) vertically disabled	0	PFGVB
h'1A8	16-r/w	bit [8:0]	0...511	vertical picture frame end line	57	PFGVE
h'198	16-r/w	bit [7:0]	0/1:	disable/enable analog FastBlank input1/2 if bit[x] is set to 1, then the function is active for the respective signal priority	0	PBFB1
h'194	16-r/w	bit [2:0]	0...7	picture frame generator priority id	7	PFGID
		bit [8]	0/1	enable prio id for picture frame generator	1	PFGEN

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
SCAN VELOCITY MODULATION						
h'1A7	16-r/w	video mode coefficients				SVM1
		bit [5:0]	0...63	gain	60	SVG
		bit [8:6]	0...6	differentiator delay (0= filter off)	1	SVD
h'19F	16-r/w	limiter				
		bit [7:0]	0...255	limit value	100	SVLIM
		bit [8:5]	0	not used, set to"0"	0	
h'19B	16-r/w	delay and coring				SVM2
		bit [3:0]	0...15	delay of SVMOUT in steps of 12.5 ns (7 = SVMOUT vs. RGBOUT is 60ns)	7	SVDEL
		bit [7:4]	0...15	coring value	0	SVCOR
		bit [8]	0	not used, set to"0"		
TUBE MEASUREMENT						
h'19C	16-r/w	tube measurement line			10	TML
		bit [8:0]	0..511	start line for tube measurement (+2 lines)		
h'15F	16-r/w	bit[10:0]	0... 1295	Latch timing of madc data in pixels before the begin of horiz. blanking HBST	128	MADCLAT
h'186	16-r/w	white drive measurement control			384	WDRM
		bit [8:0]	0..511	RGB amplitude for white-drive beam current measurement		
h'168	16-r/w	bit[14:6]	0..511	Amplitude for cutoff measurement. It can be set to measure at higher cutoff current.	256	IBRM
h'171	16-r/w	measurement control word				MCTRL
		bit [8]	0/1	enable/disable ultra black blanking	0	ULBLK_DIS
		bit [9]	0/1	0: all outputs blanked (video mute) 1: normal mode	0	BLANK_DIS
		bit [10]	0/1	78/156 kHz bandwidth for cutoff and drive measurement	0	BW_SEL
		bit [11]	0/1	enable/disable white drive measurement	0	WDR_DIS
		bit [12]	0/1	enable/disable cutoff measurement	0	CUT_DIS
		bit [13]	0/1	disable/enable horizontal blanking during measurement	0	MBLANK
		bit [14]	0/1	disable/enable RSW1 Pin as input for beam current measurement	0	SMODE

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
BRIGHTNESS and CONTRAST						
h'165	16-r/w	bit[14:6]	0..511	analog contrast for external RGB	360	EXT_CONTR
h'166	16-r/w	bit[15:6]	–256..255	analog brightness for external RGB The range allows for both increase and reduction of brightness.	128	EXT_BRT
h'167	16-r/w	bit[15:6]	–256..255	internal analog brightness The range allows for both increase and reduction of brightness.	24	INT_BRT
BCL						
h'D7	16-r/w	bit[14:3]	0..4095	measured beam current, latched every line except during vertical blanking	0	BC
h'160	16-r/w	bit[15:4]	0... 2047 0...–2048	BCL threshold current if SENSE input used BCL threshold current if RSW1 input used (max. ADC output ~2047)	64	BCL_THRES
h'161	16-r/w	bit[8:0]	0...511	BCL time constant; 0 = off	0	BCL_TC
h'162	16-r/w	bit[14:6]	0...511	BCL loop gain	0	BCL_GAIN
h'163	16-r/w	bit[14:6]	0...511	BCL minimum contrast; (= 0..max contrast)	256	BCL_MIN_C
h'164	16-r/w	bit[14:6]	0...511	BCL minimum brightness; (= 0..max bright.)	256	BCL_MIN_B

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
CUTOFF and DRIVE						
h'169	16-r/w	bit[12:4]	0...511	reference for cutoff Red	511	CUT_R
h'16A	16-r/w	bit[12:4]	0...511	reference for cutoff Green	511	CUT_G
h'16B	16-r/w	bit[12:4]	0...511	reference for cutoff Blue	511	CUT_B
h'D3	16-r	bit[11:4]	0...255	measured cutoff Red	0	CUTOFF_R
h'D4	16-r	bit[11:4]	0...255	measured cutoff Green	0	CUTOFF_G
h'D5	16-r	bit[11:4]	0...255	measured cutoff Blue	0	CUTOFF_B
h'16C	16-r/w	bit[14:6]	0...511 0	gain for cutoff control loop; the reference values are taken directly as cutoff values	0	CUT_GAIN
h'16D	16-r/w	bit[12:4]	0...511	reference for White Drive Red	511	WDR_R
h'16E	16-r/w	bit[12:4]	0...511	reference for White Drive Green	511	WDR_G
h'16F	16-r/w	bit[12:4]	0...511	reference for White Drive Blue	511	WDR_B
h'D0	16-r	bit[11:4]	0...255	measured White Drive Red	0	WDRIVE_R
h'D1	16-r	bit[11:4]	0...255	measured White Drive Green	0	WDRIVE_G
h'D2	16-r	bit[11:4]	0...255	measured White Drive Blue	0	WDRIVE_B
h'170	16-r/w	bit[14:6]	0...511 0	gain for White Drive control loop; the reference values are taken directly as white drive values	0	WDR_GAIN
h'172	16-r/w	bit[14:6]	475 ...511	threshold for automatic drive saturation avoidance	491	MAX_WDR
h'1E9	16-r/w	bit[0]	0/1	disable/enable automatic drive saturation avoidance	0	WDR_SAT

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
DISPLAY FREQUENCY DOUBLING						
h'176	16-r/w	display frequency doubling control word				DFDCTRL
		bit[1:0]	display raster mode (A' = field A in raster B) 0 = A A' B' B 1 = A A B B 2 = A A B' B' 3=not used		0	DFDMODE
		bit[3:2]	minimum field length filter 0 = off 1 = 2 fields 2 = 3 fields 3 = 4 fields		0	DFDFILT
		bit[5:4]	input sync doubling switch 0 = leave H and V sync unchanged 1 = double VSYNC and leave HSYNC unchanged 2 = double HSYNC and leave VSYNC unchanged 3 = double H and V sync		0	DFDSW
		bit[6]	clock switch 0 = Clock from LLC2 pin divided by 2 1 = Clock from LLC1 pin		0	DFDCLK
		bit[7]	test bit, set to 0		0	
		bit[8]	0 1	automatic VS/VS2 polarity detection Low-active VS/VS2 input	0	VSYPOL
		bit[9]	0 / 1	High/Low-active HS input	0	HSYPOL
		bit[10]	0 / 1	VS / VS2 Pin is source of VSYNC	0	VSYSRC
		bit[11]	0 / 1	dis-/enable still picture (only available if display frequency doubling is enabled)	0	STILL
		bit[12]	0 / 1	High / Low-active FIFO controll signals	0	FIFOPOL
TIMING						
h'1A4	16-r/w	vertical blanking start			182	VBST
		bit [8:0]	0..511	first line of vertical blanking (+ 128 offset)		
h'1A0	16-r/w	vertical blanking stop			22	VBSO
		bit [8:0]	0..511	last line of vertical blanking		
h'1D3	16-r/w	bit[10:0]	0..1295	horizontal blanking start (see Table 2–5 for max. pixels per line)	253	HBST
h'1D4	16-r/w	bit[10:0]	0..1295	horizontal blanking stop (see Table 2–5 for max. pixels per line)	331	HBSO
h'1D2	16-r/w	bit[10:0]	0..1295	Start at active video relative to pixel counter. (see Table 2–5 for max. pixels per line)	330	NEWLIN
h'18b	16-r/w	bit [8:0]	0...511	start point of active video relative to incoming HS signal in steps of 2 LLC2 clocks; can be used e.g. for panning	0	SFIF

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers								
Subaddr.	**Mode**	**Function**					**Default**	**Name**
HORIZONTAL DEFLECTION								
h'1D1	16-r/w	bit [5:0]	20..35	horizontal drive pulse duration (High time)			30	HDRV
h'140	16-r/w	horizontal deflection control register						HCTRL
		bit [0]	0	reserved, set to 0			0	
		bit [1]	0/1	enable/disable vertical protection			0	VPROT_DIS
		bit [2]	0/1	enable/disable H-safety protection			0	HPROT_DIS
		bit [3]	0/1	disable/enable drive high during flyback			0	EFLB
		bit [4]	1	start ramp up/down			0	RAMP_EN
		bit [7:5]	0..7	horizontal frequency			0	HFREQ
				H-Freq. in kHz	pixels per line @LLC 27 MHz	32 MHz		
			000	31.25	864	1024		
			001	35.1	768	912		
			010	31.46	858	1024		
			100	33.8	800	944		
			101	37.5	720	852		
			110	37.9	712	844		
h'141	16-r/w	adjustable delay of PLL2, clamping, and blanking (relative to incoming hsync) adjust clamping pulse for analog RGB input					5	POFS2
		bit [15:1]	Range ±600, 1 step = 1 pixel clock					
h'144	16-r/w	adjustable delay of flyback, H/VSYNC and analog RGB (relative to PLL2) adjust horizontal drive or H/VSYNC					0	POFS3
		bit [15:1]	Range ±600, 1 step = 1 pixel clock					
h'145 h'142	16-r/w	PLL2/3 filter coefficients						
		bit [14:6]	0...511	proportional coefficient PLL3, c*2^–9			102	PKP3
		bit [14:6]	0...511	proportional coefficient PLL2, c*2^–9			184	PKP2
h'14A	16-r/w	bit[15:6]	–512...511	vertical angle			0	ANGLE
h'14B	16-r/w	bit[15:6]	–512...511	vertical bow			0	BOW
VERTICAL MODES								
h'1E2	16-r/w	bit [0]	0/1	VSYNC synchronized/ free running			0	VS_MODE
h'1E3	16-r/w	raster mode					0	R_MODE
		bit [1:0]	0	same input and output raster				
			1	field 2 is delayed (only A raster is written)				
			2	field 1 is delayed (only B raster is written)				
			3	not used				
h'1E8	16-r/w	bit [0]	0/1	automatic lines-per-field adaption (constant raster amplitude) off/on			0	VA_MODE

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
VERTICAL PARAMETERS						
h'152	16-r/w	bit [6:0]	0... 127	window (LPFD±VSYNWIN) for sync detection	32	VSYNWIN
h'153	16-r/w	bit [9:0]	0... 1023	lines per field	312	LPFD
h'154	16-r/w	bit [9:0]	0... 1023	number of hold lines	10	HOLDL
h'155	16-r/w	bit [9:0]	0... 1023	number of flyback lines (flyback booster active)	5	FLYBL
VERTICAL SAWTOOTH CORRECTION (%-values according to DAC range)						
h'14D	16-r/w	bit [15:8]	–128...127	vertical amplitude (±25 %)	0	AMPL
h'14E	16-r/w	bit [14:6]	0...510	zoom (0...100...200 %)	256	ZOOM
h'14F	16-r/w	bit [15:8]	–128...127	vertical picture position (± 50 %) (DC offset of Sawtooth output). This offset is independent of EHT compensation.	0	VPOS
h'150	16-r/w	bit [15:8]	–128...127	linearity (±10 %)	0	LIN
h'151	16-r/w	bit [15:8]	–128...127	S-correction (±8 %)	0	SCORR
EAST-WEST PARABOLA (%-values according to DAC range)						
h'157	16-r/w	bit [15:7]	–256..255	picture width (0...100 %)	51	WIDTH
h'158	16-r/w	bit [15:8]	–128...127	trapez correction (±100 %)	0	TCORR
h'159	16-r/w	bit [15:8]	–128...127	cushion correction (±100 %)	0	CUSH
h'15A	16-r/w	bit [15:8]	–128...127	upper corner correction (±100 %)	0	CRNU
h'15B	16-r/w	bit [15:8]	–128...127	lower corner correction (±100 %)	0	CRNL
EXTREME HIGH-TENSION (EHT) COMPENSATION (%-values according to DAC range)						
h'148	16-r/w	bit[15:6]	–512...511	EHT compensation coefficient for horizontal phase (±1.5µs)	0	EHTHP
h'149	16-r/w	bit[14:6]	0...511	EHT time constant for horizontal phase compensation 0 = off	0	EHTH_TC
h'147	16-r/w	bit[15:6]	–512...511	EHT compensation coefficient for horizontal amplitude (±100 %)	0	EHTH
h'15C	16-r/w	bit [15:6]	–512...511	EHT compensation coefficient for vertical amplitude (±25 %)	0	EHTV
h'15D	16-r/w	bit [14:6]	0...511	time constant for control of vertical and horizontal amplitude EHT compensation 0 = off	0	EHTV_TC

Table 3–3: Control Registers of the XDFP, continued

XDFP Control and Status Registers						
Subaddr.	**Mode**	**Function**			**Default**	**Name**
ANALOG RGB INSERTION						
h'17A	16-r/w	Fast-Blank interface mode				FBLMODE
		bit [0]	0 1	Fast-Blank from FBLIN1 pin force internal Fast-Blank signal to High	0	FBFOH1
		bit [1]	0/1	Fast-Blank active High/Low at FBLIN pin	0	FBPOL
		bit [2]	0 1	Fast-Blank from FBLIN1 pin force internal Fast-Blank signal to Low	0	FBFOL1
		bit[3]	 0 1	Fast-Blank priority FBLIN1>FBLIN2 FBLIN1<FBLIN2	0	FBPRIO
		bit [4]	0 1	Fast-Blank from FBLIN2 pin force internal Fast-Blank signal to Low	0	FBFOL2
		bit [5]	0 1	Fast-Blank from FBLIN2 pin force internal Fast-Blank signal to High	0	FBFOH2
		bit[6]	0/1	Fast-Blank monitor input select FBLIN1/2	0	FBMON
		bit[7]	0/1	disable/enable clamping for RGBIN1&2	0	CLAMP
		bit[8]	0/1	half contrast signal active High/Low at HCS pin	0	HCSPOL
		bit[9]	0/1	disable/enable half contrast switching	0	HCSEN
		bit[10]	0 1	half contrast signal from HCS pin force internal half contrast signal to High	0	HCSFOH
		bit[11]	0 1	clamp RGBIN1 to black (if CLAMP =1) clamp RGBIN1 to bias (if CLAMP =1)	0	C1_B
		bit[12]	0 1	clamp RGBIN2 to black (if CLAMP =1) clamp RGBIN2 to bias (if CLAMP =1)	0	C2_B
I²C-CONTROLLED 8-BIT PWM						
h'178	16-r/w	bit[7:0]	0..255	PWM1 data word	0	PWM1
h'179	16-r/w	bit[7:0]	0..255	PWM2 data word	0	PWM2
XDFP STATUS REGISTER						
h'0	16-r/w	firmware version number				VER
		bit[7:0]		firmware release	–	FW_REL
		bit[15:8]		hardware version number (TC)	–	HW_VER

3.3.1. Scaler Adjustment

In case of linear scaling, most of the scaler registers need not be set. Only the scaler mode, active video length, and the fixed scaler increments (SCINC1 / SCINC2) must be written.

For adjustment of the scaler for non-linear scaling, the parameters given in Table 3–4 should be used. An example for “panorama vision” mode is depicted in Fig. 3–4. It shows the scaling of the input signal and the variation of the scaling factor during the active video line. The scaling factor starts below 1, i.e. for the borders the video data is expanded and after it exceeds 1 it is compressed. When the picture center is reached, the scaling factor is kept constant. At the second border the scaling factor changes back symmetrically.

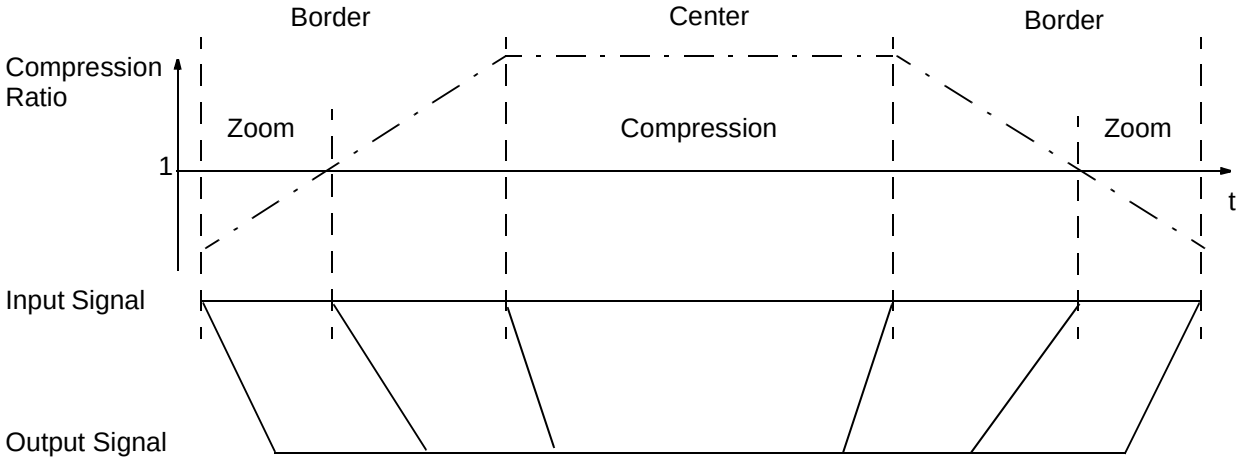


Fig. 3–4: Scaler operation for “panorama” mode

Table 3–4: Setup values for non-linear scaler modes

Mode	**27 MHz**				**32 MHz**			
	‘waterglass’ border 35 %		‘panorama’ border 30 %		‘waterglass’ border 35 %		‘panorama’ border 30 %	
Register	center 3/4	center 5/6	center 4/3	center 6/5	center 3/4	center 5/6	center 4/3	center 6/5
SCINC1	1099	1064	1024	1024	1195	1122	1024	1024
SCINC2	1024	1024	259	407	1024	1024	305	489
SCINC	60	65	56	38	54	42	68	46
FFLIM	715	717	758	796	833	845	831	871
SCW1 - 0	20	10	106	106	51	37	109	126
SCW1 - 1	156	123	106	106	161	166	125	126
SCW1 - 2	202	236	273	292	256	257	291	310
SCW1 - 3	338	349	273	292	366	386	307	310
SCW1 - 4	358	359	379	398	417	423	416	436
SCW2 - 0	20	10	186	177	51	37	168	175
SCW2 - 1	156	123	186	177	161	166	184	175
SCW2 - 2	384	417	354	363	373	368	350	359
SCW2 - 3	520	530	354	363	483	497	366	359
SCW2 - 4	540	540	540	540	534	534	534	534

4. Specifications

4.1. Outline Dimensions

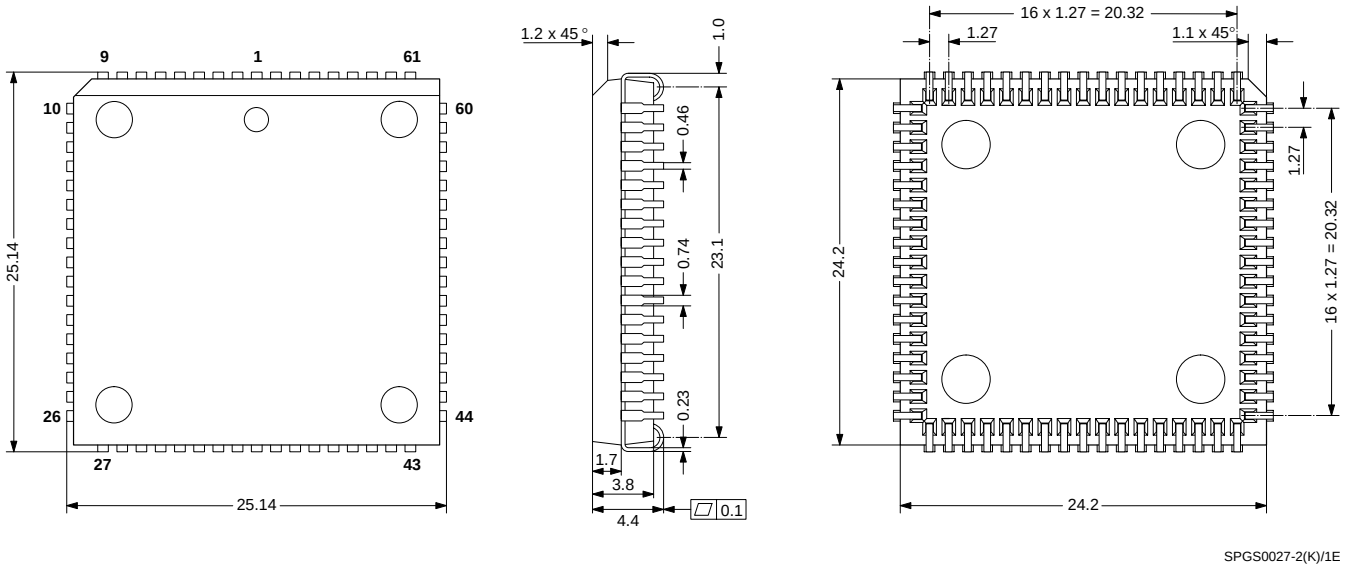


Fig. 4–1:
68-Pin Plastic Leaded Chip Carrier with heat spreader
(PLCC68K)
Weight approximately 4.8 g
Dimensions in mm

4.2. Pin Connections and Short Descriptions

NC = not connected
LV = if not used, leave vacant
X = obligatory; connect as described in circuit diagram

IN = Input
OUT = Output
SUPPLY = Supply Pin

Pin No. PLCCK 68-pin	Pin Name	Type	Connection (If not used)	Short Description
1	VSUPP	SUPPLY	X	Supply Voltage, Output Pin Driver
2	GNDP	SUPPLY	X	Ground, Output Pin Driver
3	VS2	IN	GNDD	Additional VSYNC input
4	FIFORRD	OUT	LV	FIFO Read counter Reset
5	FIFORD	OUT	LV	FIFO Read Enable
6	FIFOWR	OUT	LV	FIFO Write Enable
7	FIFORWR	OUT	LV	FIFO Write counter Reset
8	HOUT	OUT	X	Horizontal Drive Output
9	HFLB	IN	HOUT	Horizontal Flyback Input
10	SAFETY	IN	GNDO	Safety Input
11	VPROT	IN	GNDO	Vertical Protection Input

Pin No. PLCCK 68-pin	Pin Name	Type	Connection (If not used)	Short Description
12	FREQSEL	IN	X	Selection of H-Drive Frequency Range
13	CM1	IN	X	Clock Select 40.5 or 27/32 MHz
14	CM0	IN	X	Clock select 27/32 MHz
15	RSW2	OUT	LV	Range Switch2, Measurement ADC
16	RSW1	IN/OUT	LV	Range Switch1, Measurement ADC
17	SENSE	IN	GNDO	Sense ADC Input
18	GNDM	SUPPLY	X	Ground, MADC Input
19	VERT+	OUT	GNDO	Differential Vertical Sawtooth Output
20	VERT–	OUT	GNDO	Differential Vertical Sawtooth Output
21	EW	OUT	GNDO	Vertical Parabola Output
22	XREF	IN	X	Reference Input for RGB DACs
23	SVM	OUT	VSUPO	Scan Velocity Modulation
24	ROUT	OUT	VSUPO	Analog Output Red
25	GOUT	OUT	VSUPO	Analog Output Green
26	BOUT	OUT	VSUPO	Analog Output Blue
27	GNDO	SUPPLY	X	Ground, Analog Back-end
28	VSUPO	SUPPLY	X	Supply Voltage, Analog Back-end
29	VRD/BCS	IN	X	DAC Reference, Beam Current Safety
30	FBLIN1	IN	GNDO	Fast-Blank1 Input
31	RIN1	IN	GNDO	Analog Red1 Input
32	GIN1	IN	GNDO	Analog Green1 Input
33	BIN1	IN	GNDO	Analog Blue1 Input
34	FBLIN2	IN	GNDO	Fast-Blank2 Input
35	RIN2	IN	GNDO	Analog Red2 Input
36	GIN2	IN	GNDO	Analog Green2 Input
37	BIN2	IN	GNDO	Analog Blue2 Input
38	TEST	IN	GNDD	Test Pin
39	RESQ	IN	X	Reset Input, active low
40	PWM1	OUT	LV	I^2C-controlled DAC
41	PWM2	OUT	LV	I^2C-controlled DAC
42	HCS	IN	GNDD	Half-Contrast

Pin No. PLCCK 68-pin	Pin Name	Type	Connection (If not used)	Short Description
43	C0	IN	GNDD	Picture Bus Chroma (LSB)
44	C1	IN	GNDD	Picture Bus Chroma
45	C2	IN	GNDD	Picture Bus Chroma
46	C3	IN	GNDD	Picture Bus Chroma
47	C4	IN	GNDD	Picture Bus Chroma
48	C5	IN	GNDD	Picture Bus Chroma
49	C6	IN	GNDD	Picture Bus Chroma
50	C7	IN	GNDD	Picture Bus Chroma (MSB)
51	VSUPD	SUPPLY	X	Supply Voltage, Digital Circuitry
52	GNDD	SUPPLY	X	Ground, Digital Circuitry
53	LLC2	IN	X	System Clock Input (27/32/40.5 MHz)
54	Y0	IN	GNDD	Picture Bus Luma (LSB)
55	Y1	IN	GNDD	Picture Bus Luma
56	Y2	IN	GNDD	Picture Bus Luma
57	Y3	IN	GNDD	Picture Bus Luma
58	Y4	IN	GNDD	Picture Bus Luma
59	Y5	IN	GNDD	Picture Bus Luma
60	Y6	IN	GNDD	Picture Bus Luma
61	Y7	IN	GNDD	Picture Bus Luma (MSB)
62	LLC1	IN	VSUPD	Single Line-Locked Clock Input (13.5/16 MHz)
63	HS	IN	X	Horizontal Sync Input
64	VS	IN	GNDD	Vertical Sync Input
65	XTAL2	OUT	X	Analog Crystal Output (5-MHz Security Clock)
66	XTAL1	IN	X	Analog Crystal Input (5-MHz Security Clock)
67	SDA	IN/OUT	X	I^2C-Bus Data
68	SCL	IN/OUT	X	I^2C-Bus Clock

4.3. Pin Description

Pin 1 – Supply Voltage, Output Pin Driver **VSUPP***
This pin is used as supply for the following digital output pins: FIFORRD, FIFORD, FIFOWR, FIFORWR.

Pin 2 – Ground, Output Pin Driver **GNDP***
Output Pin Driver Reference

Pin 3 – Sync Signal Input **VS2** (Fig. 4–3)
Additional pin for the vertical sync information. Via I^2C-Register the used vertical sync can be switched between the inputs VS2 and VS (Pin 64)

Pin 4 – Reset for FIFO Read Counter **FIFORRD** (Fig. 4–4)
This signal is active-High and resets the read counter in the display frequency doubling FIFO.

Pin 5 – Read Enable for FIFO **FIFORD** (Fig. 4–4)
This signal is active-High and enables the read counter in the display frequency doubling FIFO.

Pin 6 – Write Enable for FIFO **FIFOWR** (Fig. 4–4)
This signal is active-High and enables the write counter in the display frequency doubling FIFO.

Pin 7 – Reset for FIFO Write Counter **FIFORWR** (Fig. 4–4)
This signal is active-High and resets the write counter in the display frequency doubling FIFO.

Pin 8 – Horizontal Drive **HOUT** (Fig. 4–5)
This open-drain output supplies the drive pulse for the horizontal output stage. A pull-up resistor has to be used (see Section 2.3.).

Pin 9 – Horizontal Flyback Input **HFLB** (Fig. 4–6)
Via this pin, the horizontal flyback pulse is supplied to the DDP 3310B (see Section 2.3.).

Pin 10 – Safety Input **SAFETY** (Fig. 4–6)
This input has two thresholds. A signal between the lower and upper threshold means normal function. Other signals are detected as malfunction (see Section 2.3.9.).

Pin 11 – Vertical Protection Input **VPROT** (Fig. 4–7)
The vertical protection circuitry prevents the picture tube from burn-in in the event of a malfunction of the vertical deflection stage. If the peak-to-peak value of the vertical sawtooth signal is too small, the RGB output signals are blanked (see Section 2.3.9.).

Pin 12 – H-Drive Frequency Range Select **FREQSEL** (Fig. 4–3)
This pin selects the frequency range for the horizontal drive signal (see Section 2.3.2.).

Pin 13 – Clock Select 40.5 or 27/32 MHz **CM1** (Fig. 4–3)
Low level selects 27/32 MHz, High level selects 40.5 MHz (see Section 2.3.12.).

Pin 14 – Clock Select 27 or 32 MHz **CM0** (Fig. 4–3)
Low level selects 27 MHz, High level selects 32 MHz (see Section 2.3.12.).

Pin 15 – Range Switch2 for Measuring ADC **RSW2** (Fig. 4–8)
This pin is an open-drain pull-down output. During cut-off measurement the switch is off. During white drive measurement the switch is on. Also during the rest of time it is on. (see Section 2.2.4.).

Pin 16 – Range Switch1 or Second Input for Measuring ADC **RSW1** (Fig. 4–9)
This pin is an open-drain pull-down output. During cut-off and white-drive measurement, the switch is off. During the rest of time it is on. The RSW1 pin can be used as second measurement ADC input (see Section 2.2.4.).

Pin 17 – Measurement ADC Input **SENSE** (Fig. 4–10)
This is the input of the analog to digital converter for the picture and tube measurement. Three measurement ranges are selectable with RSW1 and RSW2 (see Section 2.2.4.).

Pin 18 – Measurement ADC Reference Input **MGND**
This is the ground reference for the measurement A/D converter.

Pin 19 – Vertical Sawtooth Output **VERT+ (19)** (Fig. 4–11)
This pin supplies the drive signal for the vertical output stage. The drive signal is generated with 15-bit precision. The analog voltage is generated by a 4-bit current DAC with external resistor (6 kΩ for proper operation) and uses digital noise-shaping.

Pin 20 – Vertical Sawtooth Output inverted **VERT**– (Fig. 4–11)
This pin supplies the inverted signal of VERT+. Together with this pin, it can be used to drive symmetrical deflection amplifiers.

Pin 21 – East/West Parabola Output **EW** (Fig. 4–12)
This pin supplies the parabola signal for the East/West correction. The drive signal is generated with 15-bit precision. The analog voltage is generated by a 4-bit current DAC with external resistor and uses digital noise-shaping.

Pin 22 – DAC Current Reference **XREF** (Fig. 4–13)

External reference resistor for DAC output currents, typical 10 kΩ, to adjust the output current of the D/A converters. (see recommended operating conditions). This resistor has to be connected to analog ground as closely as possible to the pin.

Pin 23 – Scan Velocity Modulation Output **SVM** (Fig. 4–14)

This output delivers the analog SVM signal (see Section 2.1.11.). The D/A converter is a current sink like the RGB D/A converters. At zero signal the output current is 50 % of the maximum output current.

Pin 24, 25, 26 – Analog RGB Output **ROUT, GOUT, BOUT** (Fig. 4–14)

These pins are the analog Red/Green/Blue outputs of the back-end. The outputs are current sinks.

Pin 27 – Ground, Analog Back-end **GNDO***

This pin has to be connected to the analog ground. No supply current for the digital stages should flow through this line.

Pin 28 – Supply Voltage, Analog Back-end **VSUPO***

This pin has to be connected to the analog supply voltage. No supply current for the digital stages should flow through this line.

Pin 29 – DAC Reference Decoupling/Beam Current Safety **VRD/BCS** (Fig. 4–13)

Via this pin, the DAC reference voltage is decoupled by an external capacitor. The DAC output currents depend on this voltage, therefore a pull-down transistor can be used to shut off all beam currents. A decoupling capacitor of 4.7 µF in parallel to 100 nF (low inductance) is required.

Pin 30, 34 – Fast-Blank Input **FBLIN1/2** (Fig. 4–7)

These pins are used to switch the RGB outputs to the external analog RGB inputs. FBLIN1 switches the RIN1, GIN1 and BIN1 inputs, FBLIN2 switches the RIN2, GIN2 and BIN2 inputs. The active level (Low or High) can be selected by software.

Pin 31, 32, 33 – Analog RGB Input1 **RIN1, GIN1, BIN1** (Fig. 4–15)

These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can by switched to the analog RGB outputs with the Fast-Blank signal. The analog back-end provides separate brightness and contrast settings for the external analog RGB signals (see Section 2.2.1. and Fig.).

Pin 35, 36, 37 – Analog RGB Input2 **RIN2, GIN2, BIN2** (Fig. 4–15)

These pins are used to insert an external analog RGB signal, e.g. from a SCART connector which can by switched to the analog RGB outputs with the Fast-Blank signal. The analog back-end provides separate brightness and contrast settings for the external analog RGB signals (see Section 2.2.1. and Fig.).

Pin 38 – Test Input **TEST** (Fig. 4–16)

This pin enables factory test modes. For normal operation it must be connected to ground.

Pin 39 – Reset Input **RESQ** (Fig. 4–16)

A low level on this pin resets the DDP 3310B.

Pin 40 – Adjustable DC Output 1 **PWM1** (Fig. 4–17)

This output delivers a DC voltage with a resolution of 8 bit, adjustable over the I^2C bus. The output is driven by a push-pull stage. The PWM frequency is appr. 79.4 kHz. For a ripple-free voltage a first order lowpass filter with a corner frequency <120 Hz should be applied.

Pin 41 – Adjustable DC Output 2 **PWM2** (Fig. 4–17)

See pin 40.

Pin 42 – Half-Contrast Input **HCS** (Fig. 4–18)

Via this input pin the output level of the D/A-converted internal RGB signals can be reduced by 6 dB. Inserted external analog RGB signals remain unchanged.

Pin 43...50 – Picture Bus Chroma **C0...C7** (Fig. 4–3)

The Picture Bus Chroma lines carry the multiplexed color component data. For the 4:1:1 input signal (4-bit chroma) the pins C4...C7 are used.

Pin 51 – Supply Voltage, Digital Circuitry **VSUPD***

Pin 52 – Ground, Digital Circuitry **GNDD***

Digital Circuitry Input Reference

Pin 53 – Main Clock Input **LLC2 (53)** (Fig. 4–16)

This is the input for the line-locked clock signal. The frequency can be 27, 32, or 40.5 MHz.

Pin 54...61 – Picture Bus Luma **Y0...Y7** (Fig. 4–3)

The Picture Bus Luma lines carry the digital luminance data.

Pin 62 – Line-Locked Clock Input **LLC1** (Fig. 4–16)

This is the reference clock for the single frequency input sync signals required in a FIFO application. The frequency can be 13.5, 16, or 20.25 MHz.

Pin 63 – Sync Signal Input **HS** (Fig. 4–3)
This pin gets the horizontal sync information. Either single or double horizontal frequency or VGA horizontal sync signal.

Pin 64 – Sync Signal Input **VS** (Fig. 4–3)
This pin gets the vertical sync information. Either single or double vertical frequency or VGA vertical sync signal.

Pin 65, 66 – Crystal Output / Input **XTAL2 / XTAL1** (Fig. 4–19)
These pins are connected to an 5-MHz crystal oscillator. The security unit for the HOUT signal uses this clock signal as reference.

Pin 67 – I^2C Data Input/Output **SDA** (Fig. 4–20)
Via this pin the I^2C-bus data are written to or read from the DDP 3310B.

Pin 68 – I^2C Clock Input **SCL** (Fig. 4–20)
Via this pin, the clock signal for the I^2C-bus will be supplied. The signal can be pulled down by an internal transistor.

*** Application Note**:
All ground pins should be connected separately with short and low-resistive lines to a central power supply ground. Accordingly, all supply pins should be connected separately with short and low-resistive lines to the power supply. Decoupling capacitors from VSUPP to GNDP, VSUPD to GNDD, and VSUPO to GNDO are recommended to be placed as closely as possible to the pins.

4.4. Pin Configuration

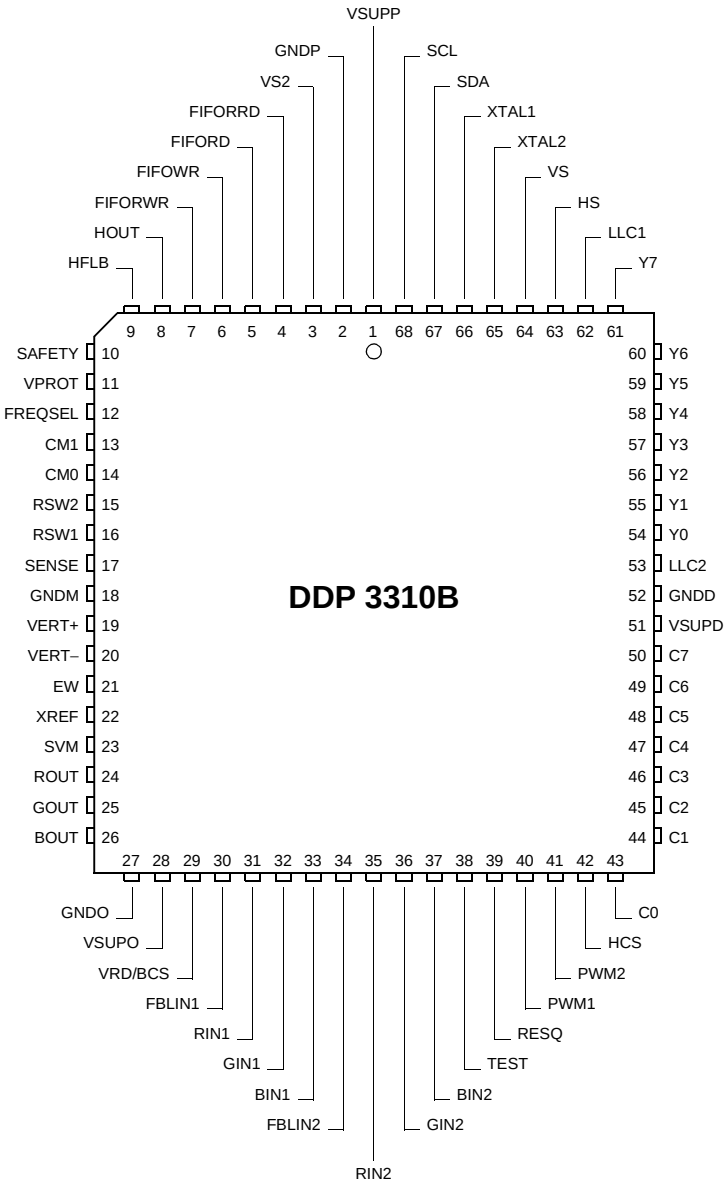


Fig. 4–2: 68-pin PLCCK package

4.5. Pin Circuits

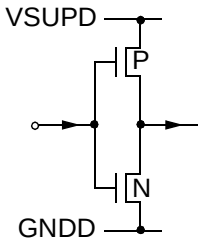


Fig. 4–3: Input pins 3, 12, 13, 14, 43 to 50, 54 to 61, 63, and 64 (VS2, FREQSEL, CM1, CM0, C[7:0], Y[7:0], HS, VS)

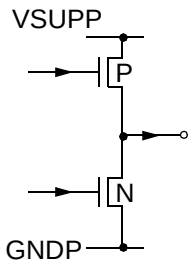


Fig. 4–4: Output pins 4 to 7 (FIFORRD, FIFORD, FIFOWR, FIFORWR)

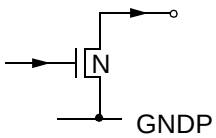


Fig. 4–5: Output pin 8 (HOUT)

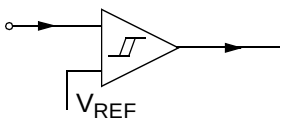


Fig. 4–6: Input pins 9 to 11 (HFLB, SAFETY, VPROT)

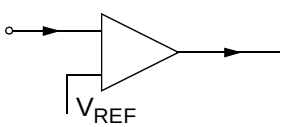


Fig. 4–7: Input pins 30 and 34 (FBLIN1, FBLIN2)

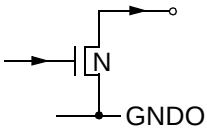


Fig. 4–8: Output pin 15 (RSW2)

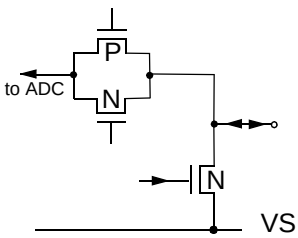


Fig. 4–9: Input/Output pin 16 (RSW1)

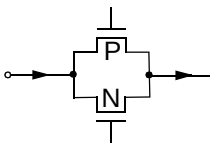


Fig. 4–10: Input pin 17 (SENSE)

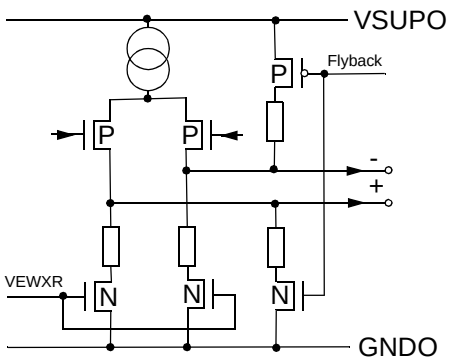


Fig. 4–11: Output pins 19 and 20 (VERT+, VERT–)

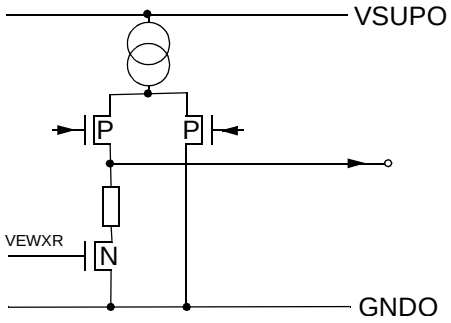


Fig. 4–12: Output pin 21 (EW)

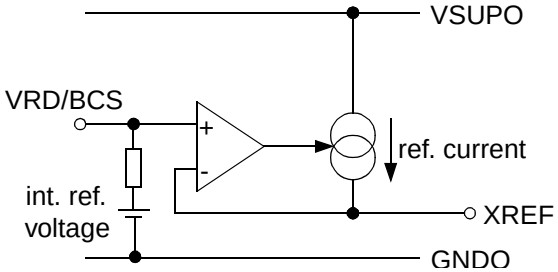


Fig. 4–13: Input pins 22 and 29 (XREF, VDR/BCS)

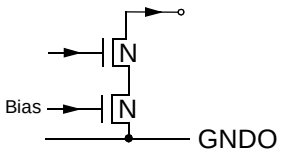


Fig. 4–14: Output pins 23 to 26
(SVM, ROUT, GOUT, BOUT)

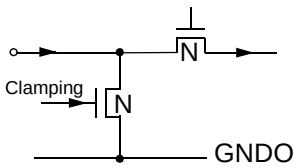


Fig. 4–15: Input pins 31 to 33 and 35 to 37
(R/G/BIN1, R/G/BIN2)

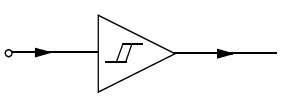


Fig. 4–16: Input pins 38, 39, 53, and 62
(TEST, RESQ, LLC2, LLC1)

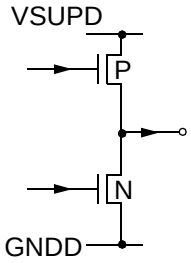


Fig. 4–17: Output pins 40 and 41 (PWM1, PWM2)

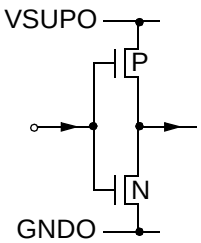


Fig. 4–18: Input pin 42 (HCS)

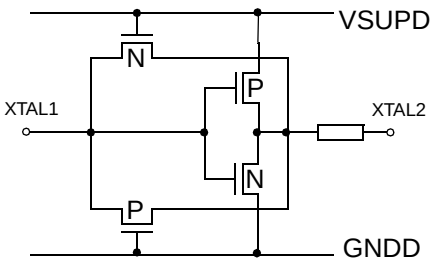


Fig. 4–19: Input pin 66 (XTAL1), Output pin 65 (XTAL2)

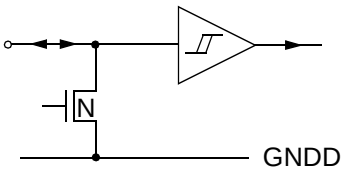


Fig. 4–20: Input/Output pins 67 and 68 (SDA, SCL)

4.6. Electrical Characteristics

4.6.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T_A	Ambient Operating Temperature	–	0	65	°C
T_C	Case Temperature	–	0	105	°C
T_S	Storage Temperature	–	–40	125	°C
V_{SUP}	Supply Voltage	All Supply Pins	–0.3	6	V
V_I	Input Voltage	All Inputs	–0.3	$V_{SUP(P/D/O)}$+0.3	V
V_O	Output Voltage	All Outputs (except HOUT)	–0.3	$V_{SUP(P/D/O)}$+0.3	V
V_{GD}	Voltage between different ground pins	All Ground Pins	–	0.3	V

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

4.6.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature		0	–	65	°C
V_{SUP}	Supply Voltages, all Supply Pins (except output pin driver supply)		4.75	5.0	5.25	V
V_{SUPP}	Output Pin Driver Supply Voltage	VSUPP	3.0	5.0	5.25	V
f_{sys}	Clock Frequency	LLC2	25.1	–	43.3	MHz
R_{xref}	RGB – DAC Current Defining Resistor	XREF	9.5	10	10.5	kΩ

4.6.3. Recommended Crystal Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
f_P	Parallel Resonance Frequency @ C_L=16 pF	XTAL1 XTAL2	–	5	–	MHz
R_R	Series Resonance Resistance @ C_L=16 pF, f_P=5 MHz		–	–	150	Ω
C_0	Shunt (Parallel) Capacitance		–	–	6	pF
C_{Lext} see Remarks!	External Load Capacitances (from both crystal pins connected to GNDD)		–	27	–	pF
Remarks:	External capacitors at each crystal pin to ground are required. They are necessary to tune the effective load capacitance (including the capacitance of the printed circuit board and the IC package) to the required load capacitance C_L of the crystal. A higher capacitance will result in a lower clock frequency. The exact value of the matching capacitor should be determined in the actual application (PCB layout). $C_{Lext} = 2 (C_L - C_{PCB} - C_{PACK})$					

4.6.4. Characteristics

Min./Max. values at: T_A = 0 to 65 °C, $V_{SUP(P/D/O)}$ = 4.75 to 5.25 V, R_{xref} = 10 kΩ, f = 27 MHz
Typical values at: T_C = 70 °C, $V_{SUP(P/D/O)}$ = 5 V, R_{xref} = 10 kΩ, f = 27 MHz

4.6.4.1. General Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
I_{VSUPO}	Current Consumption Analog Back-end	VSUPO	–	65	–	mA
I_{VSUPD}	Current Consumption Digital Processing	VSUPD	–	225	–	mA
I_{VSUPP}	Current Consumption Output Pin Driver	VSUPP	–	10	–	mA
P_{TOT}	Total Power Dissipation		–	1.5	–	W
I_L	Input and Output Leakage Current (if not otherwise specified)		–	–	0.1	µA

4.6.4.2. Line-locked Clock Inputs: LLC1, LLC2 (see Fig. 4–21)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	LLC1 LLC2	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
t_{SK}	Clock skew		–	–	±6	ns	
t_R, t_F	Clock Rise / Fall Time		–	–	5	ns	
C_{IN}	Input Capacitance		–	5	–	pF	
$1/T_{LLC1}$	Clock Frequency	LLC1	12.0	–	17.2	MHz	
t_{WL1}	Clock Low Time		26	–	–	ns	
t_{WH1}	Clock High Time		26	–		ns	
$1/T_{LLC2}$	Clock Frequency	LLC2	25.1	–	43.3	MHz	
t_{WL2}	Clock Low Time		7	–	–	ns	
t_{WH2}	Clock High Time		7	–	–	ns	

4.6.4.3. Luma, Chroma Inputs (see Fig. 4–21)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	Y[0...7] C[0...7]	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
t_{IS}	Input Setup Time		7	–	–	ns	
t_{IH}	Input Hold Time		6	–	–	ns	
C_{IN}	Input Capacitance		–	5	–	pF	

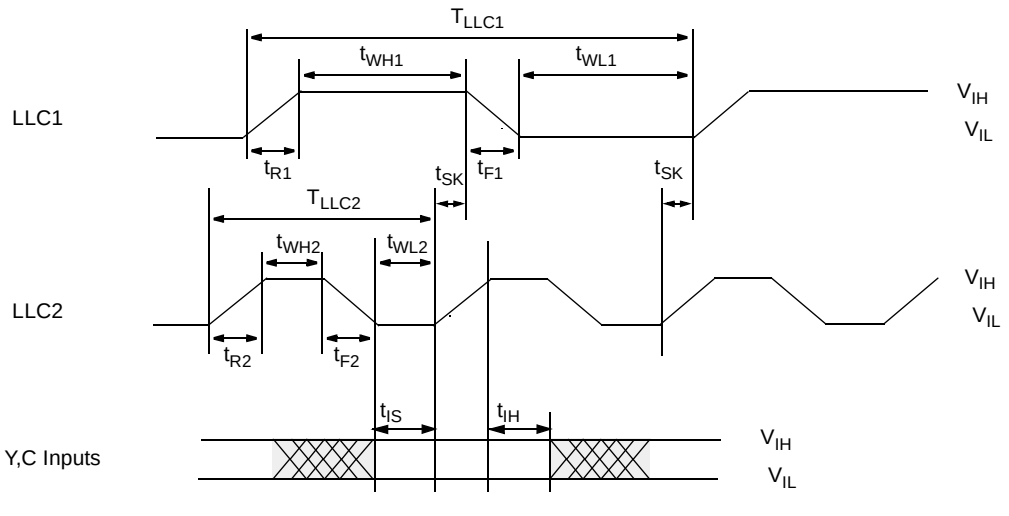


Fig. 4–21: Line-locked clock input pins and luma/chroma bus input timing

4.6.4.4. Reset Input, Test Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	RESQ TEST	–	–	2.0	V	
V_{IH}	Input High Voltage		3.2	–	–	V	
C_{IN}	Input Capacitance		–	5	–	pF	

4.6.4.5. Half-Contrast Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HCS	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
C_{IN}	Input Capacitance		–	5	–	pF	

4.6.4.6. I²C-Bus Interface

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	SDA SCL	–	–	1.5	V	
V_{IH}	Input High Voltage		3.0	–	–	V	
V_{OL}	Output Low Voltage		–	–	0.6	V	I_{OL} = 6 mA
I_{OL}	Output Low Current		–	–	10	mA	
C_{IN}	Input Capacitance		–	–	5	pF	
t_F	Signal Fall Time		–	–	300	ns	C_L = 400 pF
t_R	Signal Rise Time		–	–	300	ns	C_L = 400 pF
f_{SCL}	Clock Frequency	SCL	0	–	400	kHz	
t_{LOW}	Low Period of SCL		1.3	–	–	µs	
t_{HIGH}	High Period of SCL		0.6	–	–	µs	
t_{IS}	Input Data Set Up Time to SCL high	SDA	55	–	–	ns	
t_{IH}	Input Data Hold Time to SCL Low		55	–		ns	
t_{OS}	Output Data Set Up Time to SCL High		100	–	–	ns	
t_{OH}	Output Data Hold Time to SCL Low		15	–	900	ns	

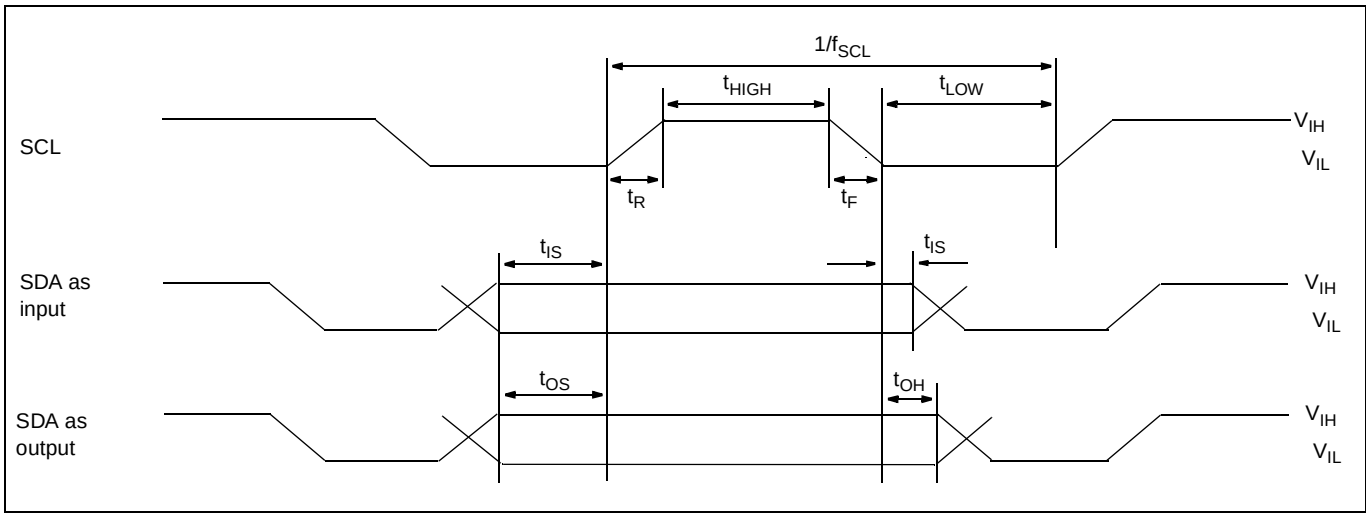


Fig. 4–22: I²C bus timing

4.6.4.7. Horizontal and Vertical Sync Inputs and Clock and Freqency Select Pins

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HS VS VS2 CM0 CM1 FREQSEL	–	–	0.8	V	
V_{IH}	Input High Voltage		2.0	–	–	V	
C_{IN}	Input Capacitance		–	5	–	pF	
t_{IS}	Input Setup Time	HS VS VS2	6	–	–	ns	
t_{IH}	Input Hold Time		7	–	–	ns	

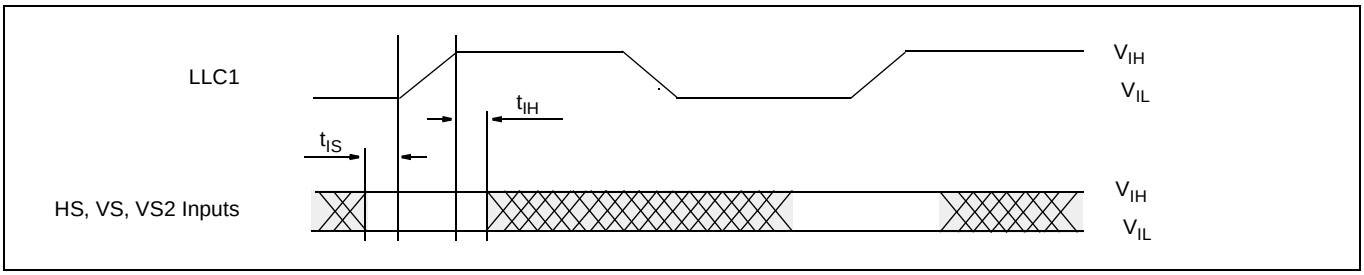


Fig. 4–23: Sync Inputs referenced to line-locked clock

4.6.4.8. Horizontal Flyback Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	HFLB	–	–	1.8	V	
V_{IH}	Input High Voltage		2.6	–	–	V	
V_{IHST}	Input Hysteresis		0.1	–	–	V	

4.6.4.9. FIFO Control Signals

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	FIFORRD FIFORD FIFORWR FIFOWR	–	–	0.4	V	I_{OL} = 1.6 mA I^2C[PSTSY] = 6
V_{OH}	Output High Voltage		VSUPP – 0.4	–	VSUPP	V	$-I_{OL}$ = 1.6 mA I^2C[PSTSY] = 6
t_{OT}	Output Transition Time		–	10	20	ns	C_{LOAD} = 30pF I^2C[PSTSY] = 6
I_{OL}	Output Current		–10	–	10	mA	

4.6.4.10. PWM Outputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	PWM1 PWM2	–	–	0.4	V	I_{OL} = 1.6 mA I^2C[PSTPR1/2] = 0
V_{OH}	Output High Voltage		VSUPD – 0.4	–	VSUPD	V	$-I_{OL}$ = 1.6 mA I^2C[PSTPR1/2] = 0
t_{OT}	Output Transition Time		–	–	20	ns	CLOAD = 10 pF Rlp = 4.7 kΩ Clp = 100 nF I^2C[PSTPR1/2] = 0

4.6.4.11. Horizontal Drive Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{OL}	Output Low Voltage	HOUT	–	–	0.4	V	I_{OL} = 10 mA
V_{OH}	Output High Voltage (Open-Drain Stage)		–	–	8	V	external pull-up resistor
t_{OF}	Output Fall Time		–	8	20	ns	C_{LOAD} = 30 pF
I_{OL}	Output Low Current		–	–	10	mA	

4.6.4.12. Vertical Protection Input (see Section 2.3.9.)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IA}	Input Threshold A	VPROT	1.2	1.0	0.8	V	
V_{IB}	Input Threshold B		1.7	1.5	1.3	V	
V_{IHST}	Input Hysteresis A and B		0.1	–	–	V	

4.6.4.13. Horizontal Safety Input (see Section 2.3.9.)

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{IA}	Input Threshold A	SAFETY	2.5	2.2	1.9	V	
V_{IB}	Input Threshold B		3.8	3.5	3.2	V	
V_{IHST}	Input Hysteresis A and B		0.1	–	–	V	

4.6.4.14. Vertical and East/West D/A Converter Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
	Resolution	EW VERT+ VERT–	–	15	–	bit	
V_{OMIN}	Minimum Output Voltage		–	0	–	V	R_{load} = 6.8 kΩ R_{xref} = 10 kΩ
V_{OMAX}	Maximum Output Voltage		2.82	3	3.2	V	R_{load} = 6.8 kΩ R_{xref} = 10 kΩ
I_{DACN}	Full scale DAC Output Current		415	440	465	µA	R_{xref} = 10 kΩ
PSRR	Power Supply Rejection Ratio		–	20	–	dB	

4.6.4.15. Sense A/D Converter Input

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{I255}	Input Voltage for code 255	SENSE RSW1	1.4	1.54	1.7	V	
C_0	Digital Output for zero Input		–	–	16	LSB	
R_I	Input Impedance		1	–	–	MΩ	
Range Switch Outputs							
R_{ON}	Output On Resistance	RSW1 RSW2	–	–	50	Ω	I_{OL} = 10 mA
I_{Max}	Maximum Current		–	–	15	mA	
I_{LEAK}	Leakage Current		–	–	600	nA	RSW High Impedance

4.6.4.16. Analog RGB and Fast-Blank Inputs

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{RGBIN}	External RGB Input Voltage Range	RIN1 GIN1 BIN1 RIN2 GIN2 BIN2	–0.3	–	1.1	V	
V_{RGBIN}	Nominal RGB Input Voltage Peak-to-Peak		0.5	0.7	1.0	V_{PP}	SCART Spec: 0.7 V ±3 dB
V_{RGBIN}	RGB Input Voltage for Maximum Output Current		–	0.44	–		Contrast setting: 511
			–	0.7	–		Contrast setting: 323
			–	1.1	–		Contrast setting: 204
C_{RGBIN}	External RGB Input Coupling Capacitor		–	10	–	nF	
	Clamp Pulse Width		1.6	–	–	µs	
C_{IN}	Input Capacitance		–	–	13	pF	
I_{IL}	Input Leakage Current		–0.5	–	0.5	µA	Clamping OFF, V_{IN} = –0.3...3 V
V_{CLIP}	RGB Input Voltage for Clipping Current		–	2	–	V	
V_{CLAMP}	Clamp Level at Input		40	60	80	mV	Clamping ON
V_{INOFF}	Offset Level at Input		–10	–	10	mV	Extrapolated from V_{IN} = 100 and 200 mV
V_{INOFF}	Offset Level Match at Input		–10	–	10	mV	Extrapolated from V_{IN} = 100 and 200 mV
R_{CLAMP}	Clamping-ON-Resistance		–	140	–	Ω	
V_{FBLOFF}	FBLIN Low Level	FBLIN1 FBLIN2	–	–	0.5	V	
V_{FBLON}	FBLIN High Level		0.9	–	–	V	
$V_{FBLTRIG}$	Fast-Blanking Trigger Level typical		–	0.7	–		
t_{PID}	Delay Fast Blanking to RGB_{OUT} from midst of FBLIN-transition to 90% of RGB_{OUT} transition		–	8	15	ns	Internal RGB = 3.75 mA (Full Scale) Internal Brightness = 0 External Brightness = 1.5 mA (Full Scale) RGBin = 0 V_{FBLOFF} = 0.4 V V_{FBLON} = 1.0 V Rise and fall time = 2 ns
	Difference of Internal Delay to External RGBin Delay		–5	–	+5	ns	
	Switch-Over-Glitch		–	0.5	–	pAs	Switch from 3.75 mA (int.) to 1.5 mA (ext.)

4.6.4.17. Analog RGB Outputs, D/A Converters

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Internal RGB Signal D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	10	–	bit	
I_{OUT}	Full Scale Output Current		3.6	3.75	3.9	mA	R_{ref} = 10 kΩ
I_{OUT}	Differential Non-Linearity		–	–	1	LSB	
I_{OUT}	Integral Non-Linearity		–	–	2	LSB	
I_{OUT}	Glitch Pulse Charge		–	0.5	–	pAs	Ramp signal, 25 Ω output termination
I_{OUT}	Rise and Fall Time		–	3	–	ns	10 % to 90 %, 90 % to 10 %
I_{OUT}	Intermodulation		–	–	–50	dB	2/2.5 MHz full scale
I_{OUT}	Signal to Noise		+50	–	–	dB	Signal: 1MHz full scale Bandwidth: 10MHz
I_{OUT}	Matching R-G, R-B, G-B		–2	–	2	%	
	R/B/G Crosstalk one channel talks two channels talk		–	–	–46	dB	Passive channel: I_{OUT} =1.88 mA Crosstalk-Signal: 1.25 MHz, 3.75 mA_{PP}
	RGB Input Crosstalk from external RGB one channel talks two channels talk three channels talk		 – – –	 – – –	 –50 –50 –50	 dB dB dB	
Internal RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{BR}	Full Scale Output Current relative		39.2	40	40.8	%	Ref to max. digital RGB
I_{BR}	Full Scale Output Current absolute		–	1.5	–	mA	
I_{BR}	Differential Non-Linearity		–	–	1	LSB	
I_{BR}	Integral Non-Linearity		–	–	2	LSB	
I_{BR}	Match R-G, R-B, G-B		–2	–	2	%	
I_{BR}	Match to digital RGB R-R, G-G, B-B		–2	–	2	%	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
RGB Output Cutoff D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{CUT}	Full Scale Output Current relative		58.8	60	61.2	%	Ref to max. digital RGB
	Full Scale Output Current absolute		–	2.25	–	mA	
	Differential Non-Linearity		–	–	1	LSB	
	Integral Non-Linearity		–	–	2	LSB	
	Matching to digital RGB R-R, G-G, B-B		–2	–	2	%	
RGB Output Ultrablack D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	1	–	bit	
I_{UB}	Full Scale Output Current relative		19.6	20	20.4	%	Ref to max. digital RGB
	Full Scale Output Current absolute		–	0.75	–	mA	
External RGB Voltage/Current Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{EXOUT}	Full Scale Output Current relative		96	100	104	%	Ref. to max. Digital RGB V_{IN} = 0.7 V_{PP}, contrast = 323
	Full Scale Output Current absolute		–	3.75	–	mA	Same as Digital RGB
CR	Contrast Adjust Range		–	16:511	–		
	Gain Match R-G, R-B, G-B		–2	–	2	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 323
	Gain Match to RGB-DACs R-R, G-G, B-B		–3	–	3	%	Measured at RGB Outputs V_{IN} = 0.7 V, contrast = 323
	R/B/G Input Crosstalk one channel talks two channels talk		–	–	–46	dB	Passive channel: V_{IN} = 0.7 V, contrast = 323 Crosstalk signal: 1.25 MHz, 3.75 mA_{PP}
	RGB Input Crosstalk from Internal RGB one channel talks two channels talk tree channels talk		–	–	–50	dB	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
	RGB Input Noise and Distortion	ROUT GOUT BOUT	–	–	–50	dB	V_{IN}=0.7 V_{PP} at 1 MHz contrast = 323 Bandwidth: 10 MHz
	RGB Input Bandwidth -3 dB			15	–	MHz	V_{IN} = 0.7 V_{PP}, contrast =323
	RGB Input THD		– –	–50 –40	– –	dB dB	Input signal 1 MHz Input signal 6 MHz V_{IN} = 0.7 V_{PP} contrast =323
	Differential Non-Linearity of Contrast Adjust		–	–	1.0	LSB	V_{IN} = 0.44V
	Integral Non-Linearity of Contrast Adjust		–	–	7	LSB	
V_{RGBO}	R,G,B Output Voltage		–1.0	–	0.3	V	Referred to V_{SUPO}
	R,G,B Output Load Resistance		–	–	100	Ω	Ref. to V_{SUPO}
V_{OUTC}	RGB Output Compliance		–1.5	–1.3	–1.2	V	Ref. to V_{SUPO} Sum of max. Current of RGB-DACs and max. Current of Int. Brightness DACs is 2 % degraded
External RGB Brightness D/A Converter Characteristics							
	Resolution	ROUT GOUT BOUT	–	9	–	bit	
I_{EXBR}	Full-Scale Output Current relative		39.2	40	40.8	%	Ref to max. digital RGB
	Full Scale Output Current absolute		–	1.5	–	mA	
	Differential Non-Linearity		–	–	1	LSB	
	Integral Non-Linearity		–	–	2	LSB	
	Matching R-G, R-B, G-B		–2	–	2	%	
	Matching to digital RGB R-R, G-G, B-B		–2	–	2	%	

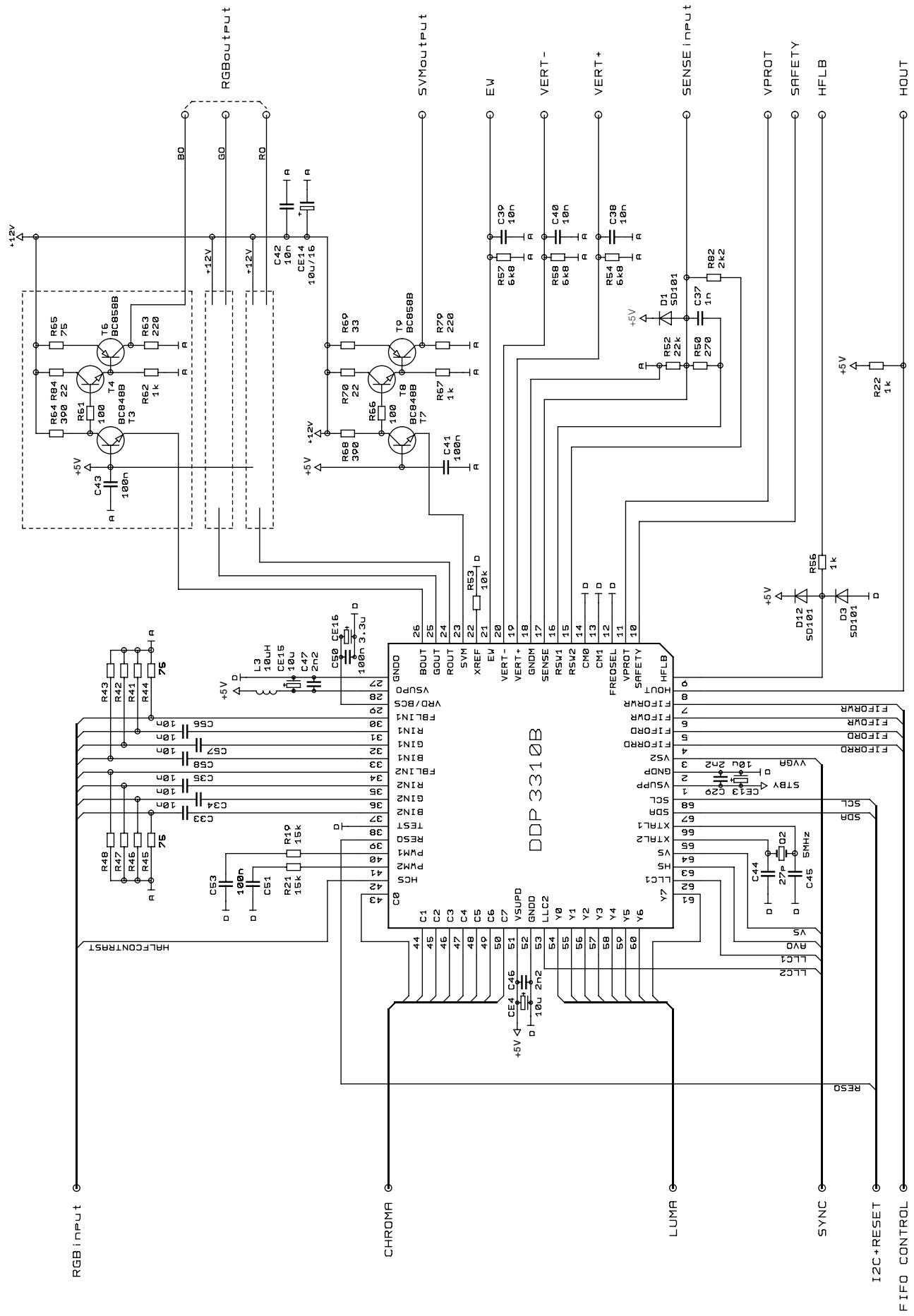
4.6.4.18. Scan Velocity Modulation Output

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
	Resolution	SVMOUT	–	8	–	bit	
I_{OUT}	Full-Scale Output Current		1.55	1.875	2.25	mA	
I_{OUT}	Differential Non-Linearity		–	–	0.5	LSB	
I_{OUT}	Integral Non-Linearity		–	–	1	LSB	
I_{OUT}	Glitch Pulse Charge		–	0.5	–	pAs	Ramp, output line is terminated on both ends with 50 Ω
I_{OUT}	Rise and Fall Time		–	3	–	ns	10 % to 90 %, 90 % to 10 %

4.6.4.19. DAC Reference, Beam Current Safety

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
V_{DACREF}	DAC-Ref. Voltage	VRD/BCS	2.38	2.50	2.67	V	
	DAC-Ref. Output resistance	VRD/BCS	18	25	32	kΩ	
V_{XREF}	DAC-Ref. Voltage Bias Current Generation	XREF	2.25	2.34	2.43	V	R_{xref} = 10 kΩ

5. Application Circuit



6. Data Sheet History

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