

# SONY

# CXA1008P/1009P

## High-speed Sample and Hold Amplifiers

### Description

CXA1008P/1009P are bipolar IC's developed for the purpose of sample holding video signals and other signals at high-speed.

### Features

- Maximum sampling frequency  
CXA1008P 35 MHz  
CXA1009P 18 MHz
- Linearity 0.08% (Typ.)
- Clock input level ECL compatible
- Low power consumption  
CXA1008P 680 mW (Typ.)  
CXA1009P 420 mW (Typ.)

### Structure

Bipolar silicon monolithic IC.

### Applications

- A/D converter and other analog signal processing
- Other general applications.

### Block Diagram

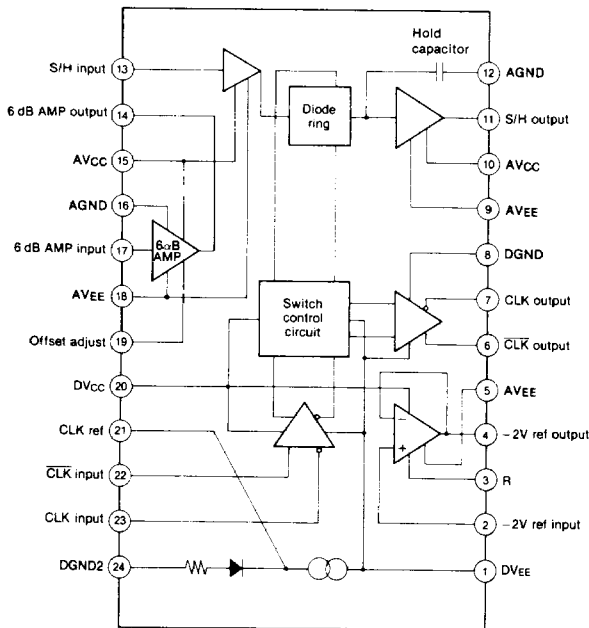
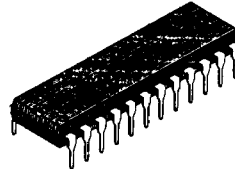


Fig. 1

24pin DIP(Plastic)



### Function

High-speed hold circuit, wide band 6 dB amplifier, A/D reference power supply, A/D clock output circuit.

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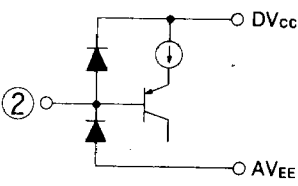
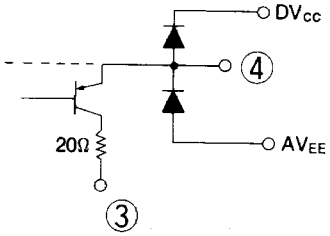
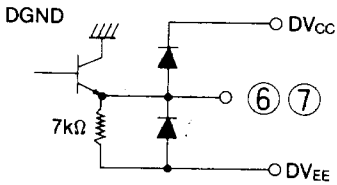
**Absolute Maximum Ratings ( $T_a = 25^\circ\text{C}$ )**

•Supply voltage	$V_{CC}$	+ 5.5	V
	$V_{EE}$	-6.0	V
•Operating temperature	$T_{opr}$	-20 to +75	$^\circ\text{C}$
•Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
•Allowable power dissipation	$P_D$	1.2	W

**Recommended Operating Conditions**

•Supply voltage	$V_{CC}$	+ 4.75 to 5.25V
	$V_{EE}$	-4.75 to -5.45V

Pin Description

No.	Symbol	Equivalent circuit	Description
1	DV <sub>EE</sub>		Digital V <sub>EE</sub> (-5V)
2	-2V ref input		reference voltage input for A/D converter
3	R		Pulldown terminal for external R (30Ω typically)
4	-2V ref output		reference voltage output for A/D converter
5	AV <sub>EE</sub>		Analog V <sub>EE</sub> (-5V)
6	CLK output		CLK output for A/D converter
7	CLK output		CLK output for A/D converter
8	DGND		Digital GND
9	AV <sub>EE</sub>		Analog V <sub>EE</sub> (-5V)
10	AV <sub>CC</sub>		Analog V <sub>CC</sub> (+5V)

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No.	Symbol	Equivalent circuit	Description
11	S/H output		S/H output
12	AGND		Analog GND
13	S/H input		S/H input
14	6dB AMP output		Output terminal of 6dB amplifier
15	AV <sub>CC</sub>		Analog V <sub>CC</sub> (+5V)
16	AGND		Analog GND

No.	Symbol	Equivalent circuit	Description
17	6dB AMP input		6dB AMP input
18	AV <sub>EE</sub>		Analog V <sub>EE</sub> (-5V)
19	offset adjust		6dB AMP DC offset adjust terminal
20	DV <sub>CC</sub>		Digital V <sub>CC</sub> (+5V)
21	CLK ref		CLK reference output
22	CLK input		CLK input (Note: connect to 21 PIN or input ECL CLK signal)
23	$\overline{\text{CLK}}$ input		$\overline{\text{CLK}}$ input (Note: input ECL CLK signal)
24	DGND		Digital GND

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## CXA1008P

Electrical Characteristics (Ta = 25°C, VCC = +5V, VEE = -5V)  
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V <sub>IH</sub>	-0.9	-0.8		V
		V <sub>IL</sub>		-1.6	-1.5	V
CLK Reference voltage (pin 21)		V <sub>CLKREF</sub>	-1.3	-1.2	-1.1	V
Analog input voltage range	$\Delta V < 1.2V$ *1	V <sub>INS</sub>	-3		3	V
Output voltage range		V <sub>outs</sub>	-3		3	V
Power Supply		I <sub>CC</sub>	48	60	78	mA
	without -2V ref.	I <sub>EE1</sub>	48	60	78	mA
	with -2V ref. R <sub>LI</sub> = 50Ω *2	I <sub>EE2</sub>	80	100	125	mA
Input bias current	$-2V < V_{in} < 2V$	I <sub>Bias</sub>		15	30	μA
Output impedance		Z <sub>OS</sub>		20	40	Ω
Voltage gain ratio		G <sub>vs</sub>	0.99	1.0	1.01	
Full power bandwidth	V <sub>in</sub> = 2V <sub>p-p</sub> (-3dB)	BW		12		MHz
Power supply rejection ratio		SVR <sub>s</sub>		-40		dB
Hold mode feed through	f <sub>in</sub> = 4MHz V <sub>in</sub> = 1 V <sub>p-p</sub> , CLK open	HMTH		-50	-40	dB
Clock leak	V <sub>in</sub> = 0V	CLLEAK		10	50	mV
Linearity	f <sub>in</sub> = 19.53kHz (10/512MHz) f <sub>CLK</sub> = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to -2V	HMDR		2	20	mV/μs
Acquisition time	$\Delta V = 1.2V$	T <sub>aq</sub>		8	12	ns
		T <sub>set</sub>		25		ns
DC offset voltage	f <sub>CLK</sub> = 5MHz	V <sub>offset</sub>		± 15	± 100	mV
Maximum sampling frequency		f <sub>CLKH</sub>	35			MHz
Minimum sampling frequency		f <sub>CLKL</sub>			5	MHz
Differential gain (D.G.)	V <sub>in</sub> = NTSC 40 IRE mode ramp.	DG		0.5	1.0	%
Differential phase (D.P.)	f <sub>CLK</sub> = 20MHz	DP		0.5	1.0	deg

(R<sub>LI</sub> = 50Ω. see Fig. 3)

CXA1009P

Electrical Characteristics (Ta = 25°C, VCC = +5V, VEE = -5V)  
S/H section (see Fig. 3)

Item	Condition	Symbol	Min.	Typ.	Max.	Unit
Digital input voltage		V <sub>IH</sub>	-0.9	-0.8		V
		V <sub>IL</sub>		-1.6	-1.5	V
CLK Reference voltage (pin 21)		V <sub>CLKREF</sub>	-1.3	-1.2	-1.1	V
Analog input voltage range	$\Delta V < 1.2V$ *1	V <sub>INS</sub>	-3		3	V
Output voltage range		V <sub>outs</sub>	-3		3	V
Power supply		I <sub>CC</sub>	25	35	45	mA
	without -2V ref.	I <sub>EE1</sub>	25	35	45	mA
	with -2V ref. R <sub>LI</sub> = 50Ω *2	I <sub>EE2</sub>	60	75	98	mA
Input bias current	-2V < V <sub>in</sub> < 2V	I <sub>BIASS</sub>		9	18	μA
Output impedance		Z <sub>OS</sub>		20	40	Ω
Voltage gain ratio		G <sub>VS</sub>	0.99	1.0	1.01	
Full power bandwidth	V <sub>in</sub> = 2V <sub>p-p</sub> (-3dB)	BW		6		MHz
Power supply rejection ratio		SVR <sub>S</sub>		-40		dB
Hold mode feed through	f <sub>in</sub> = 4MHz V <sub>in</sub> = 1 V <sub>p-p</sub> , CLK open	HMTH		-50	-40	dB
Clock leak	V <sub>in</sub> = 0V	CLLEAK		10	50	mV
Linearity	f <sub>in</sub> = 19.53kHz (10/512MHz) f <sub>CLK</sub> = 10MHz *3	Lin		0.08	0.15	%
Hold mode droop	input voltage range, 0 to -2V	HMDR		2	10	mV/μs
Acquisition time	$\Delta V = 1.2V$	T <sub>aq</sub>		12	20	ns
Settling time	Settle to ±0.2% of F.S. see the Timing Chart	T <sub>set</sub>		36		ns
DC offset voltage	f <sub>CLK</sub> = 5MHz	V <sub>offset</sub>		±15	±100	mV
Maximum sampling frequency		f <sub>CLKH</sub>	18			MHz
Minimum sampling frequency		f <sub>CLKL</sub>			2	MHz
Differential gain (D.G.)	V <sub>in</sub> = NTSC 40 IRE more ramp	DG		0.5	1.0	%
Differential phase (D.P.)	f <sub>CLK</sub> = 15MHz	DP		0.5	1.0	deg

- \*1 ΔV is voltage change during one sampling period.
- \*2 Power consumption is I<sub>CC</sub> × 5V + I<sub>EE1</sub> × 5V + 40mA × 1.8V.
- \*3 Input voltage waveform

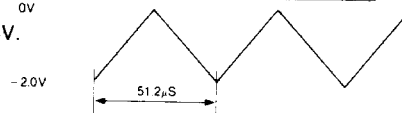


Fig. 2

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## 6dB amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input voltage range	*3	$V_{INA}$	-1.3		+0.8	-1.3		+0.8	V
Band width (-3dB)	$V_{in} = 1V_{pp}$	W	45	55		15	25		MHz
Input bias current	$-1V < V_{in} < 1V$	$I_{Bias A}$		9	20		5	10	$\mu A$
Output impedance		$Z_{OA}$		4	10		4	10	$\Omega$
Voltage gain	*4	$G_{VA}$	5.1	6.0	6.9	5.1	6.0	6.9	dB
Power supply rejection ratio		$SVR_A$		-40			-40		dB

\*3 2ndary harmonic: -40dB  $f_{in} = 3.58MHz$ \*4  $f_{in} = 3.58MHz$   $V_{in} = 1V_{pp}$ 

## CLK OUT section (see Fig. 3)

Item		Condition	Symbol	CXA1008P			CXA1009P			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
Output voltage	Amplitude	$R_{L2} = 1.5 K\Omega$ see Fig. 3	$V_{CLK}$	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low level		$V_{CLKL}$	-1.2	-1.1	-0.9	-1.2	-1.1	-0.9	V
Rise time			$t_r$		7	10		7	10	ns
Fall time			$t_f$		5	8		5	8	ns
CLK Delay 1			$\tau_{D1}$	20	28	34	36	38	45	ns
CLK Delay 2			$\tau_{D2}$	14	22	28	24	26	33	ns

-2V<sub>ref</sub> amp section (see Fig. 3)

Item	Condition	Symbol	CXA1008P			CXA1009P			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Voltage gain ratio	$V_{ref} = -2V$ $R_{L1} = 50\Omega$	GVR	0.9	1.0	1.1	0.9	1.0	1.1	
Input bias current	$-3V < V_{in} < 0V$	$I_{Bias R}$		5	10		5	10	$\mu A$
Output impedance		$Z_{OR}$		2	10		2	10	$\Omega$



Electrical Characteristics Test Circuit

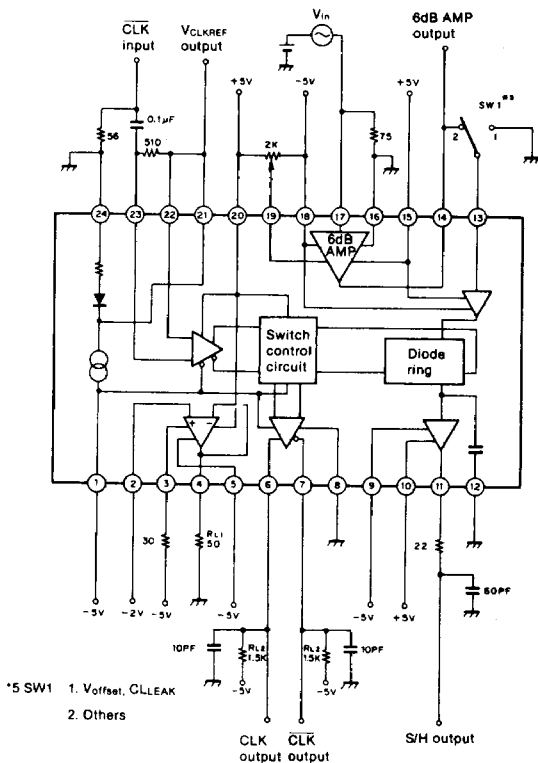


Fig. 3

Timing Chart

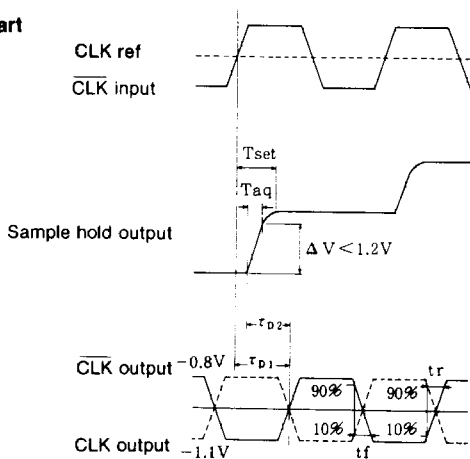


Fig. 4

**Description of Functions**

CXA1008P/1009P are the monolithic ICs incorporating a high-speed sample hold circuit, a wide band 6 dB amp, reference power supply for A/D converter, and a clock output section, and operate up to a sampling frequency of 35/18 MHz.

CXA1008P/1009P can compose in 20/15 MS/s A/D converter system in combination with a CX20052A. CXA1008P/1009P form, with the input of a single phase or 2-phase ECL clock input, a new sampling signal. For this reason, the sampling period remain unchanged even when the frequency or duty of the input sampling CLK signal changes.

•Wide band 6 dB AMP.

In-phase amp with a band width over 45/15 MHz amplifies ordinary TV signal (1Vp-p) to a 2Vp-p signal which gives the highest accuracy when processed in CX20052A.

•CLK output section

When used in combination with an A/D converter such as CX20052A, the CLK timing between the S/H circuit and the A/D converter needs to be adjusted, and up to 20/15 MHz, CXA1008P/1009P generate CLK timing signals for driving the A/D converter, and output 2-phase CLK at 300 mVp-p from pins 6 and 7. With this output, no separate CLK is required to combine with an A/D converter.

•CXA1008P/1009P incorporate a buffer amp to provide a reference voltage for the A/D converter.

**Application Circuit**

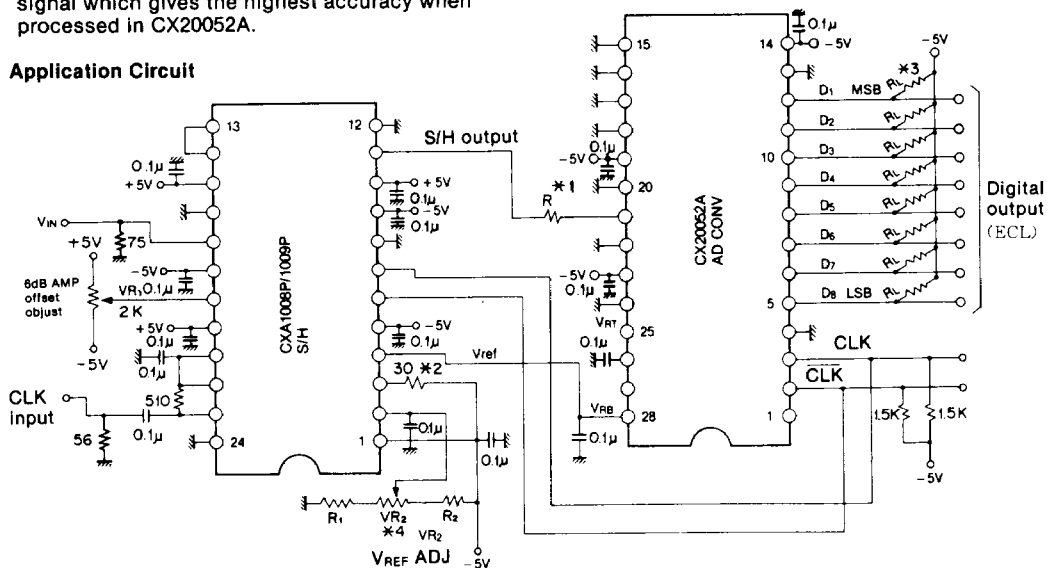


Fig. 5 Connection of CXA 1008P/1008P with CX20052A (1)

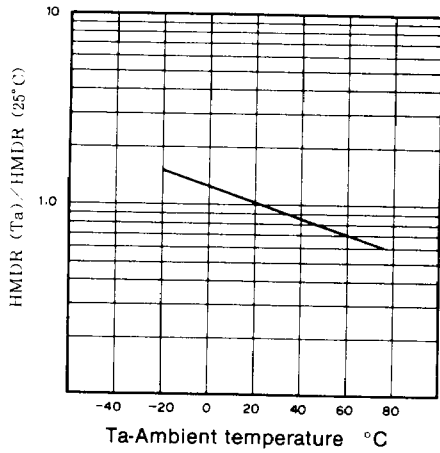
- \*1 R is a ringing preventing resistor. Select between 10 to 50Ω
- \*2 Pulldown R for Vref
- \*3 RL = 4.3kΩ
- \*4 R1 = 1kΩ, VR2 = 2kΩ, R2 = 2kΩ

**Notes on Application**

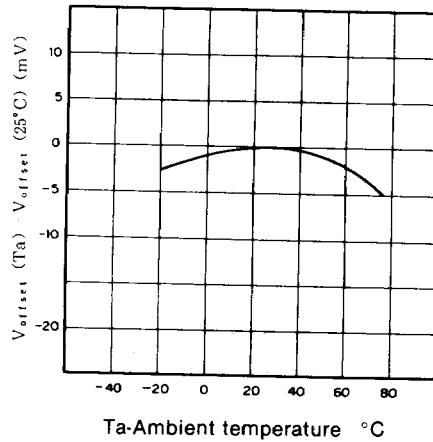
1. Unless sufficiently stable power supply and GND voltage in the high-frequency range are used, the device characteristics deteriorates. For this reason, bring the power supply bypass capacitor as near to this IC as possible, and make the pattern to the power supply and to the earth terminal as wide as feasible.
2. To reduce CLK leak, use waveforms similar to sine waves as far as possible, up to the CLK input. For satisfactory operation, a CLK input amplitude of around 300mV is enough.
3. When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.

Changes in Characteristics with Temperature

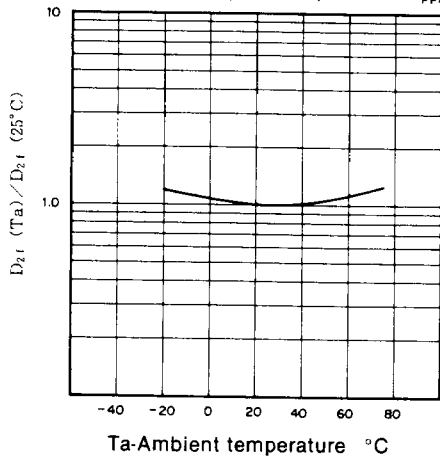
Hold Mode Droop Rate



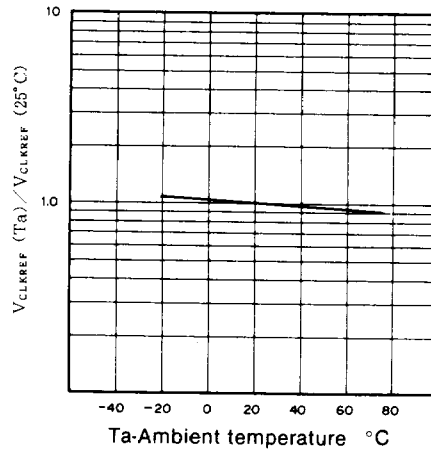
Offset Voltage Between S/H Input & Output



6dB AMP 2ndary Harmonic Level  
(3.58MHz, Vin = 1Vpp)

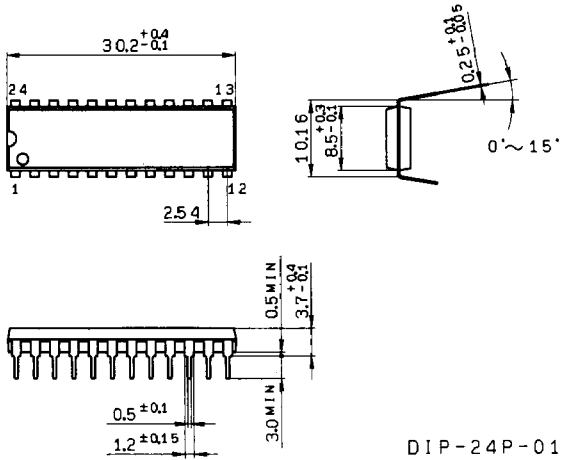


CLK Ref Voltage



Package Outline Unit : mm

24pin DIP(Plastic) 400mil 2.0g



DIP-24P-01

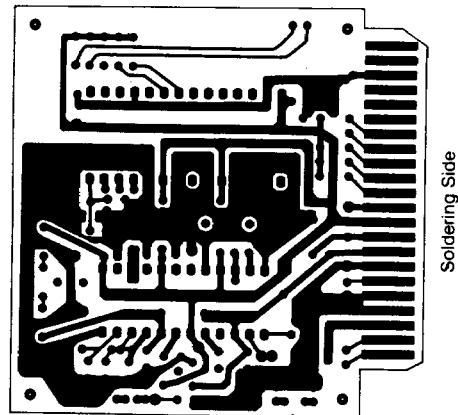
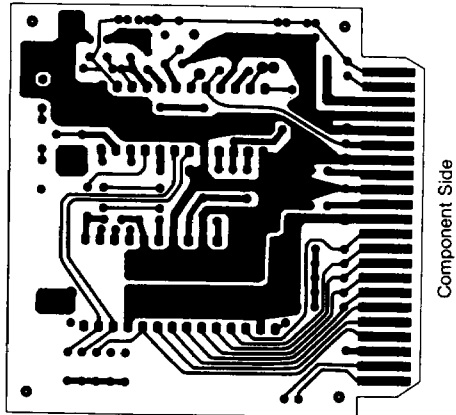
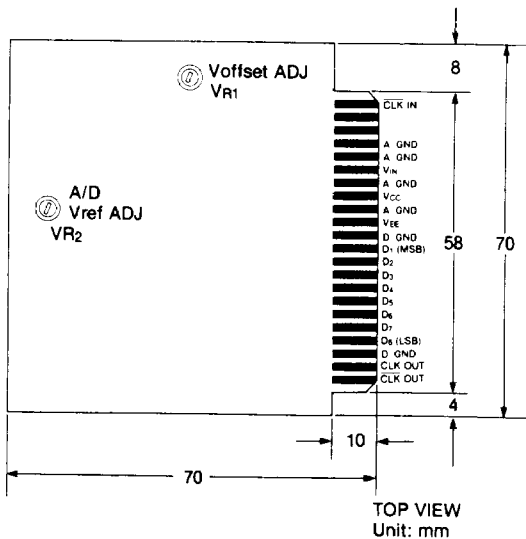
# 8bit, 20/15MHz A/D Converter Evaluation Board with CXA1008P/CXA1009P S/H.

## Description

CX20052A PCB-3A/3B is an 8 bit A/D converter board for video signal processing. A high speed S/H IC CXA1008P/1009P and a high speed 8 bit A/D converter CX20052A are assembled on single small printed circuit board.  
 CX20052A PCB-3A with CXA1008P mounted, operates up to 20 MHz of conversion rate, and CX20052A PCB-3B with CXA1009P mounted, operates up to 15 MHz of conversion rate.

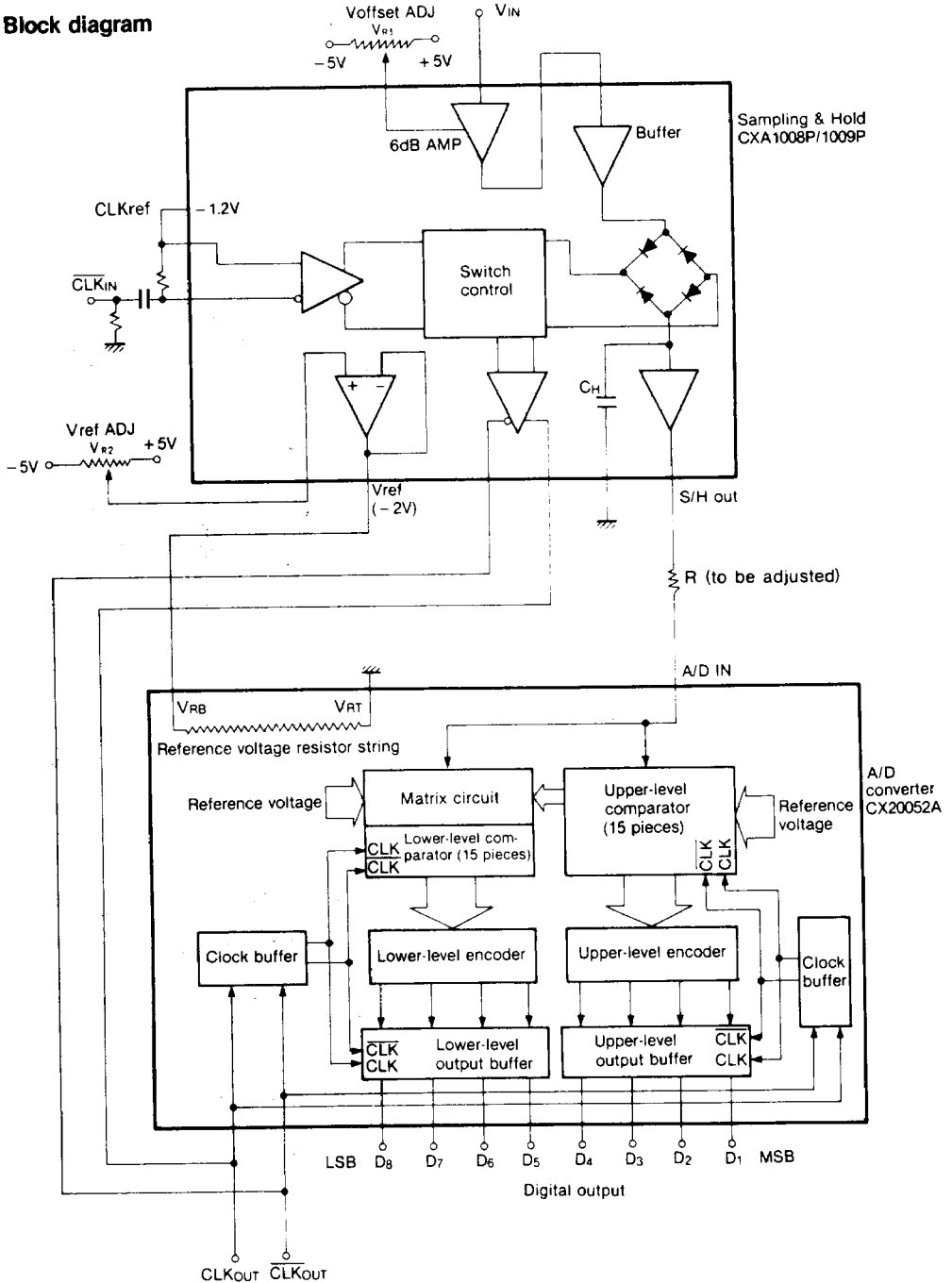
## Features

- Resolution 8 bit  $\pm 1/2$  LSB
- Conversion rate 20 MHz CX20052A PCB-3A  
15 MHz CX20052A PCB-3B
- Analog input level 1Vp-p
- Digital output level ECL level
- Power supply  $\pm 5V$



CX20052A PCB-3A/3B Pattern

1. Block diagram



2. Characteristics

1. Supply Voltage

(Ta = 25°C, VEE = -5V, VCC = 5V)

Item		Symbol	Min	Typ	Max	Unit
VCC	+5V	CX20052A ICC		70	80	mA
		PCB-3A IEE		220	240	mA
VEE	-5V	CX20052A ICC		50	60	mA
		PCB-3B IEE		200	220	mA

2. Analog Input (VIN)

Item	Symbol	Min	Typ	Max	Unit
AC Input Voltage Amplitude	VIN			1	V
Offset Adjustable Range		±1.5	±2.0		V
Input Impedance	Zin				
CX20052APCB-3A			75		Ω
CX20052APCB-3B			75		Ω

3. Digital Input (CLK IN)

Item	Symbol	Min	Typ	Max	Unit
Input Voltage (p-p)	VCLK	0.3	0.8	4	V
Input Impedance	ZINCL		50		Ω

4. Digital Output (D1 - D8) (1.5kΩ to VEE)

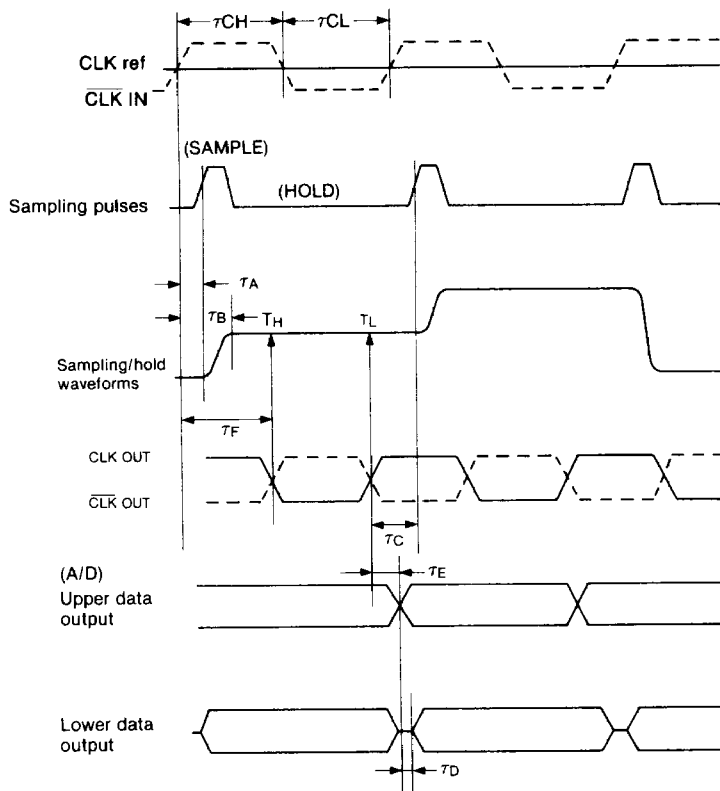
Item	Symbol	Min	Typ	Max	Unit
Output Voltage	VOH	-0.90	-0.75		V
	VOL		-1.50	-1.35	V

5. Clock Output (CLKOUT, CLKOUT) (See timing chart)

Item	Symbol	CX20052A PCB-3A			CX20052A PCB-3B			Unit	
		Min	Typ	Max	Min	Typ	Max		
Output voltage	Amplitude	VCLK	0.2	0.3	0.4	0.2	0.3	0.4	V
	Low Level	VCLKL	-1.2	-1.1	-0.9	-1.2	-1.1	-0.9	V
Rise time	tr		6	10		6	10	ns	
Fall time	tf		12	15		12	15	ns	
CLK Delay	TF	20	28	34	36	38	45	ns	



3. Timing Chart



$T_H$  shows a timing when the A/D latches upper 4 bits.  
 $T_L$  shows a timing when the A/D latches lower 4 bits.

Item	Symbol	CX20052A PCB-3A			CX20052A PCB-3B			Unit
		Min	Typ	Max	Min	Typ	Max	
Clock in	$T_{CH}$		25			33		ns
	$T_{CL}$		25			33		ns
Sampling delay	$T_A$		6			12		ns
	$T_B$		25			36		ns
Clock out	$T_F$	20	28	34	36	38	45	ns
Data delay	$T_E$			8			8	ns
	$T_D$			4			4	ns



#### 4. Adjustment

- (1) Offset Voltage (Voffset ADJ)  
VR<sub>1</sub> should be adjusted so that the S/H output meets the input voltage range of the A/D (0 to -2V).
- (2) A/D reference voltage (Vref ADJ).  
The reference voltage of the A/D (TP5) is to be -2V. VR<sub>2</sub> should be adjusted.

#### 5. Output Data Format

The input of the A/D converter IC (S/H out) is quantized in 8 bit within the reference voltage range of V<sub>RT</sub> and V<sub>RB</sub>. The V<sub>RT</sub> and V<sub>RB</sub> are set at 0V and -2V respectively on the printed circuit board.

Step	A/D input signal voltage		Digital output code	
			MSB	LSB
0 0 0	over	0. 0 0 0 0 V	1 1 1 1 1 1 1 1	
		0. 0 0 0 0 V (V <sub>RT</sub> )	1 1 1 1 1 1 1 1	
.		.	.	
.		.	.	
1 2 7		-0. 9 9 6 1 V	1 0 0 0 0 0 0 0	
1 2 9		-1. 0 0 3 9 V	0 1 1 1 1 1 1 1	
.		.	.	
.		.	.	
2 5 5		-2. 0 0 0 0 V (V <sub>RB</sub> )	0 0 0 0 0 0 0 0	
	under	-2. 0 0 0 0 V	0 0 0 0 0 0 0 0	

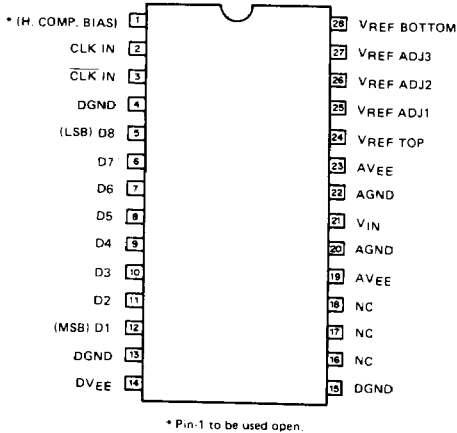
#### 6. Note on application

- (1) Although the pull down resistors (RL: 4.3kΩ) are mounted on the PCB, additional pull down is recommended in an external circuit. The output current at the A/D output terminal should not exceed 10 mA.
- (2) Digital output data should be latched by an external circuit to achieve a rated performance. Output data can be latched at a rising edge of CLK<sub>out</sub>.  
CLK<sub>OUT</sub> AND  $\overline{\text{CLK}}_{\text{OUT}}$  should be reshaped by an ECL line receiver such as MC10116 in an external circuit.
- (3) The reference voltage is derived from the V<sub>EE</sub> by a simple resistor dividing network. The power supply (±5V) should be stabilized to reduce voltage drift of the reference voltage.
- (4) To reduce CLK leak, use waveforms similar to sine waves as far as possible up to the CLK input. For satisfactory operation, a CLK input amplitude of around 300m V<sub>PP</sub> is enough.
- (5) When the S/H input deviates over 1.2V during one sampling period, the output may contain errors.





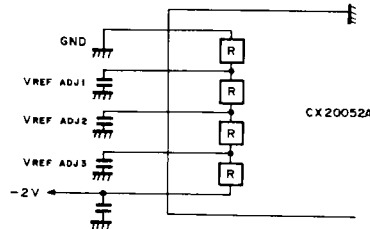
**Additional Information on CX20052A  
Pin Configuration (Top View)**



**Pin Description**

No.	Symbol	Description
1	H-COMP BIAS	Pin connected to internal comparator. It should not be connected to outer circuit.
2	CLK IN	CLOCK input pin.
3	CLK IN	CLOCK input pin.
4	DGND	Ground pin of digital circuit.
15	DGND	Ground pin of digital circuit.
17	NC	Non-connection.
18	NC	
24	VREF (T)	Reference voltage pin. (0V)
25	VREF ADJ1	Reference voltage adjusting pin. (Usually it should be connected to GND through 0.047 μF capacitor.)
26	VREF ADJ2	
27	VREF ADJ3	
28	VREF (B)	Reference voltage pin. (-2.0V)

(\* ) Reference resistors have adjusting pins as shown below. Usually these pins are connected to GND through 0.047 μF capacitors. When an adjustment is required, they should be connected to GND or VREF (B) through resistors.



**Output Coding**

Step	Input signal voltage	Output digital code	
		MSB	LSB
000	0.0000V	11111111	
.	.	.	.
.	.	.	.
127	-0.9961V	10000000	
128	-1.0039V	01111111	
129	-1.0118V	01111110	
.	.	.	.
.	.	.	.
255	-2.0000V	00000000	