2N5114 SERIES – JANTX, JANTXV P-Channel JFETs

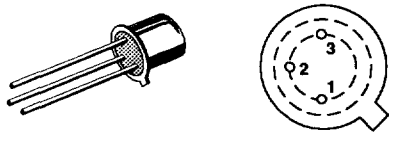
Siliconix incorporated

The 2N5114 Series are p-channel JFET analog switches designed to complement our n-channel 2N4856 Series. They feature low on-resistance and good off-isolation as well as the fast switching associated with JFETs. They are housed in TO-18 hermetic packages and available with JAN, JANTX, or JANTXV level processing.

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ MAX (pA)	t_{ON} MAX (ns)
2N5114	10	75	-500	16
2N5115	6	100	-500	30
2N5116	4	150	-500	42

For additional design information please see performance curves PSCIA.

TO-18 **BOTTOM VIEW**



1 SOURCE
2 GATE & CASE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J174 Series
- SOT-23, See SST174 Series
- Chips, See PSCIA Series Die

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	30	V
Gate-Source Voltage	V_{GS}	30	
Gate Current	I_G	-50	mA
Power Dissipation	P_D	500	mW
Power Derating		3	mW/°C
Operating Junction Temperature Range	T_J	-55 to 200	°C
Storage Temperature Range	T_{stg}	-65 to 200	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

2N5114 SERIES – JANTX, JANTXV

SPECIFICATIONS[a]				LIMITS							
					2N5114		2N5115		2N5116		
PARAMETER	SYMBOL	TEST CONDITIONS		TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC											
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = 1 µA, V_{DS} = 0 V		45	30		30		30		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = −15 V, I_D = −1 nA			5	10	3	6	1	4	
Saturation Drain Current[c]	I_{DSS}	V_{GS} = 0 V	V_{DS} = −18 V		−30	−90					mA
			V_{DS} = −15 V				−15	−60	−5	−25	
Gate Reverse Current	I_{GSS}	V_{GS} = −20 V, V_{DS} = 0 V		5		500		500		500	pA
			T_A = 150°C	0.01		1		1		1	µA
Gate Operating Current[d]	I_G	V_{DG} = −15 V, I_D = −1 mA		5							
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = −15 V	V_{GS} = 12 V	−10		−500					pA
			V_{GS} = 7 V	−10				−500			
			V_{GS} = 5 V	−10						−500	
		V_{DS} = −15 V, T_A = 150°C	V_{GS} = 12 V	−0.02		−1					µA
			V_{GS} = 7 V	−0.02				−1			
			V_{GS} = 5 V	−0.02						−1	
Drain-Source On-Voltage	$V_{DS(ON)}$	V_{GS} = 0 V	I_D = −15 mA	−1.0		−1.3					V
			I_D = −7 mA	−0.7				−0.8			
			I_D = −3 mA	−0.5						−0.6	
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, I_D = −1 mA				75		100		150	Ω
Gate-Source Forward Voltage[d]	$V_{GS(F)}$	I_G = −1 mA, V_{DS} = 0 V		−0.7							V
DYNAMIC											
Common-Source Forward Transconductance[d]	g_{fs}	V_{DG} = −15 V, I_D = −1 mA, f = 1 kHz		4.5							mS
Common-Source Output Conductance[d]	g_{os}			20							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V, f = 1 kHz				75		100		175	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz		20		25		25		27	pF
Common-Source Reverse Transfer Capacitance	C_{rss}	V_{DS} = 0 V, f = 1 MHz	V_{GS} = 12 V	5		7					
			V_{GS} = 7 V	6				7			
			V_{GS} = 5 V	6						7	
Equivalent Input Noise Voltage[d]	$\bar{e}_n$	V_{DG} = −10 V, I_D = −1 mA, f = 1 kHz		20							$nV/\sqrt{Hz}$
SWITCHING											
Turn-On Time	$t_{d(ON)}$	$V_{GS(ON)}$ = 0 V				6		10		12	ns
	t_r	P/N V_{DD} $I_{D(ON)}$ $V_{GS(OFF)}$ R_L R_G				10		20		30	
Turn-Off Time	$t_{d(OFF)}$	2N5114 −10V −15mA 20V 630Ω 100Ω 2N5115 −6V −7mA 12V 900Ω 220Ω 2N5116 −6V −3mA 8V 2000Ω 390Ω				6		8		10	
	t_f					15		30		50	

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 2%.
d. Not JEDEC registered.

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