BIPOLAR TRANSISTOR CHIPS

NPN Transistors

'MPS' Device Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @V_{CB} (V)	h_{FE} Min.	h_{FE} Max.	DC Current Gain @I_C (mA)	DC Current Gain @V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @I_C (mA)	f_T Min. (MHz)	f_T @I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Process
MPSA43C	500	200	200	6.0	100	160	40	—	30	10	0.5	20	50	10	4.0	—	—	BLA
MPSD01C	500	200	200	4.0	100	80	25	—	10	10	—	—	40	10	—	—	—	BLA
MPSD02C	600	140	140	4.0	100	80	25	—	10	10	—	—	40	10	—	—	—	VXA
MPSD03C	600	100	100	4.0	100	80	25	—	10	10	—	—	40	10	—	—	—	VXA
MPSD04C	500	25[3]	—	10	1000	20	2k	—	100	5.0	1.0	100	100	10	—	—	—	SQL
MPSD05C	800	25	25	4.0	1000	20	80	—	100	5.0	0.5	100	100	50	—	—	—	DAC
MPSD06C	500	25	25	4.0	1000	20	50	—	10	5.0	0.3	50	100	10	—	—	—	BBC
MPSL01C	600	140	120	5.0	1000	75	50	300	10	5.0	0.2	10	60	10	8.0	—	—	VXA
MPSU45C	1000	50	40	12	100	30	25k	150k	200	5.0	1.5	1000	100	200	6.0	—	—	BNB

NOTES:
1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

'D' Device Types

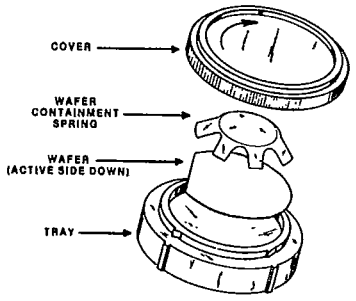
ELECTRICAL CHARACTERISTICS at T_A = 25°C

Device Type	I_C Max. (mA)	$V_{(BR)CBO}$ (V)	$V_{(BR)CEO}$ (V)	$V_{(BR)EBO}$ (V)	I_{CBO} Max. (nA)	I_{CBO} @V_{CB} (V)	h_{FE} Min.	h_{FE} Max.	DC Current Gain @I_C (mA)	DC Current Gain @V_{CE} (V)	$V_{CE(sat)}$ Max. (V)	$V_{CE(sat)}$ @I_C (mA)	f_T Min. (MHz)	f_T @I_C (mA)	C_{ob}[1] (pF)	t_s[1] (ns)	NF[1] (dB)	Process
D16P1C	500	18	12	12	100	18	6K	—	100	5.0	1.4	200	60	2.0	10	—	—	TPM
D33D21C	800	35[3]	25	5.0	100[3]	25	60	200	2.0	2.0	0.75	500	100	50	15	—	—	DAC
D33D22C	800	35[3]	25	5.0	100[3]	25	150	500	2.0	2.0	0.75	500	135	50	15	—	—	DAC
D33D24C	800	50[3]	40	5.0	100[3]	25	60	120	2.0	2.0	0.75	500	80	50	15	—	—	DAC
D33D25C	800	50[3]	40	5.0	100[3]	25	100	200	2.0	2.0	0.75	500	120	50	15	—	—	DAC
D33D26C	800	50[3]	40	5.0	100[3]	25	150	300	2.0	2.0	0.75	500	135	50	15	—	—	DAC
D33D27C	800	50[3]	40	5.0	100[3]	25	250	500	2.0	2.0	0.75	500	150	50	15	—	—	DAC
D33D29C	800	70[3]	60	5.0	100[3]	25	60	120	2.0	2.0	0.75	500	80	50	15	—	—	DAC
D33D30C	800	70[3]	60	5.0	100[3]	25	100	200	2.0	2.0	0.75	500	120	50	15	—	—	DAC
D40D4C	1000	60[3]	45	5.0	100[3]	60	50	150	100	2.0	0.5	500	—	—	—	—	—	DID
D40D5C	1000	60[3]	45	5.0	100[3]	60	120	360	100	2.0	0.5	500	—	—	—	—	—	DID
D40D10C	1000	90[3]	75	5.0	100[3]	90	50	150	100	2.0	1.0	500	—	—	—	—	—	DID
D40D11C	1000	90[3]	75	5.0	100[3]	90	120	360	100	2.0	1.0	500	—	—	—	—	—	DID

NOTES:
1) Maximum at typical JEDEC conditions.
2) µA.
3) $V_{(BR)CES}/I_{CES}$, as applicable.
4) mA.
5) $V_{(BR)CER}$ at R = 10Ω.

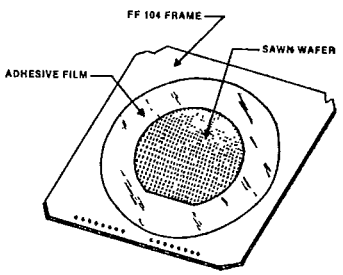
SEMICONDUCTOR CHIP PACKAGING

UNSCRIBED WAFER IN NATURAL POLYPROPYLENE TRAY



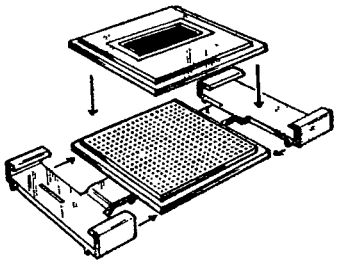
Dwg No. A-11,626

SAWN WAFER ON STRETCHED MEMBRANE



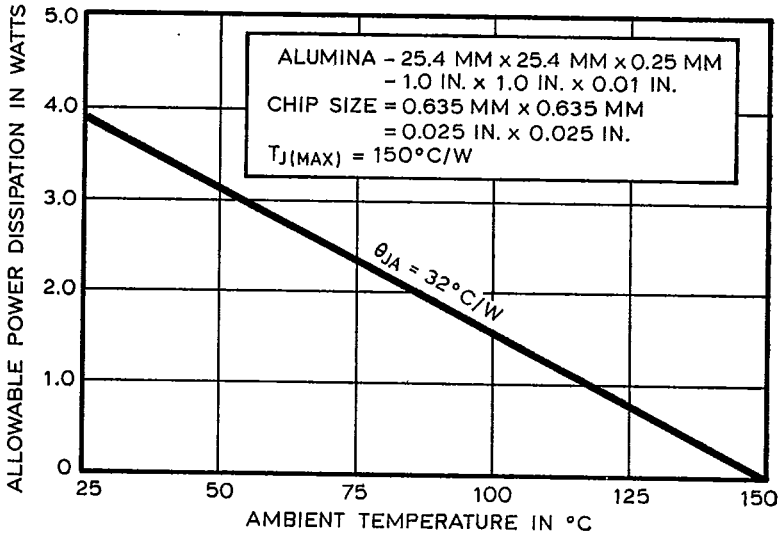
Dwg No. A-11,621

INDIVIDUAL COMPARTMENTS IN SEE-THROUGH PLASTIC BOX



Dwg. No. A-11,547

MAXIMUM ALLOWABLE POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



Dwg. No. A-13,625