

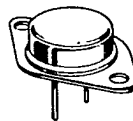
HIGH VOLTAGE NPN SILICON TRANSISTORS

... designed for use in high-voltage inverters, converters, switching regulators and line operated amplifiers.

- High Collector-Emitter Voltage – $V_{CEX} = 700$ Vdc
- Excellent DC Current Gain –
 $h_{FE} = 10$ (Min) @ $I_C = 2.5$ Adc
- Low Collector-Emitter Saturation Voltage –
 $V_{CE(sat)} = 0.8$ Vdc (Max) @ $I_C = 1.0$ Adc

**3.5 AMPERE
POWER TRANSISTORS
NPN SILICON**

**400 VOLTS
100 WATTS**



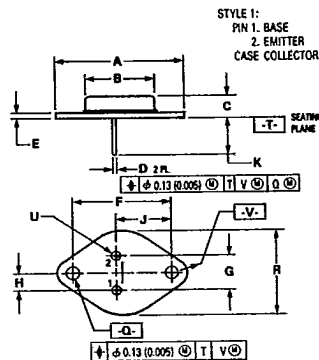
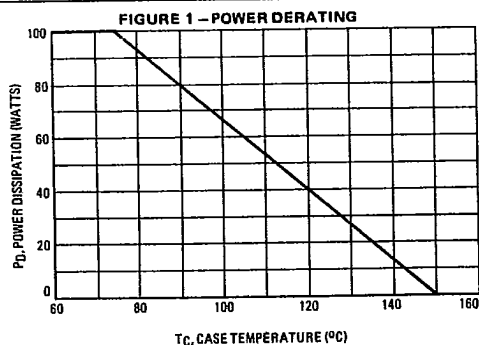
***MAXIMUM RATINGS**

Rating	Symbol	2N3902	Unit
Collector-Emitter Voltage	V_{CEO}	400	Vdc
Collector-Emitter Voltage	V_{CEX}	700	Vdc
Emitter-Base Voltage	V_{EB}	5.0	Vdc
Collector Current – Continuous	I_C	3.5	A dc
Base Current	I_B	2.0	A dc
Total Device Dissipation @ $T_C = 75^\circ\text{C}$ Derate above 75°C	P_D	100 1.33	Watts W/ $^\circ\text{C}$
Operating Junction Temperature Range	T_J	-65 to +150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +200	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	0.75	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANS_I Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	39.37	—	1.550
B	—	21.08	—	0.830
C	6.35	8.25	0.250	0.325
D	0.97	1.09	0.038	0.043
E	1.40	1.77	0.055	0.070
F	30.15 BSC		1.187 BSC	
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
J	16.89 BSC		0.665 BSC	
K	11.18	12.19	0.440	0.480
Q	3.94	4.19	0.151	0.165
R	—	28.67	—	1.050
U	4.83	5.33	0.190	0.210
V	3.84	4.19	0.151	0.165

**CASE 1-06
TO-204AA
(TO-3)**

***ELECTRICAL CHARACTERISTICS** ($T_C = 25^\circ\text{C}$ unless otherwise noted)

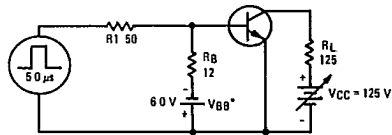
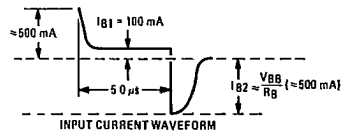
Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Sustaining Voltage ($I_C = 100\text{ mAdc}$, $I_B = 0$) (See Figure 12)	$V_{CE(sus)}$	325	—	Vdc
Collector Cutoff Current ($V_{CE} = 400\text{ Vdc}$, $I_B = 0$)	I_{CEO}	—	0.25	mAdc
Collector Cutoff Current ($V_{CE} = 700\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$) ($V_{CE} = 400\text{ Vdc}$, $V_{EB(off)} = 1.5\text{ Vdc}$, $T_C = 125^\circ\text{C}$)	I_{CEX}	—	2.5 0.5	mAdc
Emitter Cutoff Current ($V_{BE} = 5.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 1.0\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$) ($I_C = 2.5\text{ Adc}$, $V_{CE} = 5.0\text{ Vdc}$)	h_{FE}	30 10	90 —	—
Collector-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{CE(sat)}$	—	0.8 2.5	Vdc
Base-Emitter Saturation Voltage ($I_C = 1.0\text{ Adc}$, $I_B = 0.1\text{ Adc}$) ($I_C = 2.5\text{ Adc}$, $I_B = 0.5\text{ Adc}$)	$V_{BE(sat)}$	—	1.5 2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain-Bandwidth Product ($I_C = 0.2\text{ Adc}$, $V_{CE} = 10\text{ Vdc}$)	f_T	2.8	—	MHz

*Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

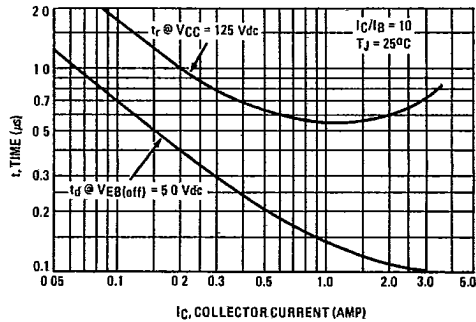
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FIGURE 2 – SWITCHING TIMES TEST CIRCUIT



5.0% Duty Cycle
 $t_r = 100\text{ ns}$

FIGURE 3 – TURN-ON TIME



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FIGURE 4 - THERMAL RESPONSE

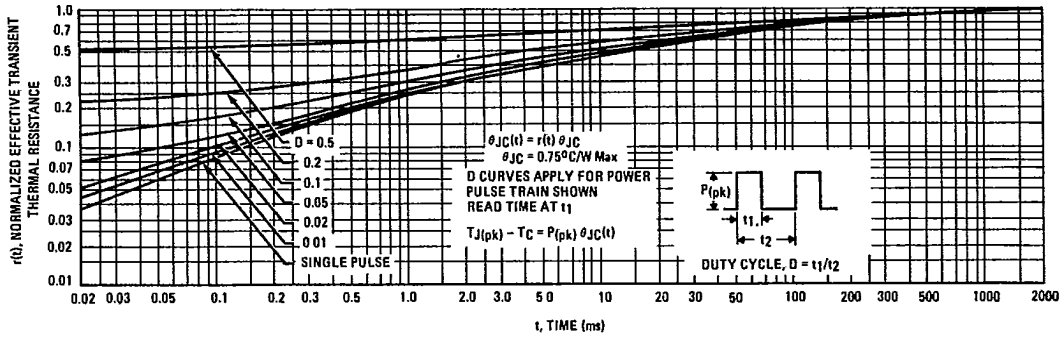
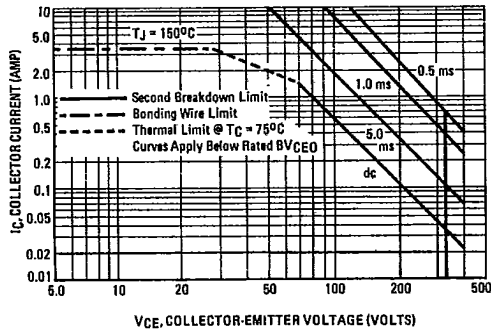


FIGURE 5 - ACTIVE-REGION SAFE-OPERATING AREA



There are two limitations on the power handling ability of a transistor: junction temperature and secondary breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on $T_{J(pk)} = 150^{\circ}\text{C}$; T_C is variable depending on conditions. Pulse curves are valid for duty cycles of 10% provided $T_{J(pk)} \leq 150^{\circ}\text{C}$. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by secondary breakdown.

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FIGURE 6 - TURN-OFF TIME

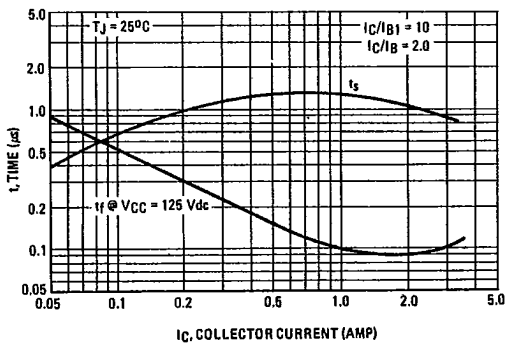


FIGURE 7 - CAPACITANCE

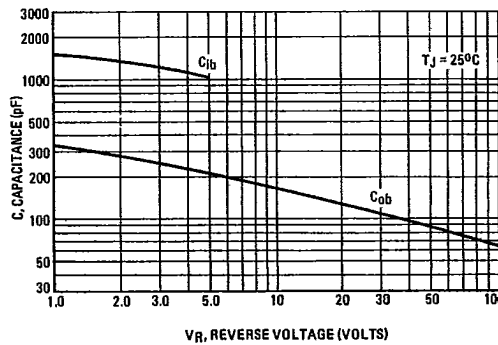


FIGURE 8 – DC CURRENT GAIN

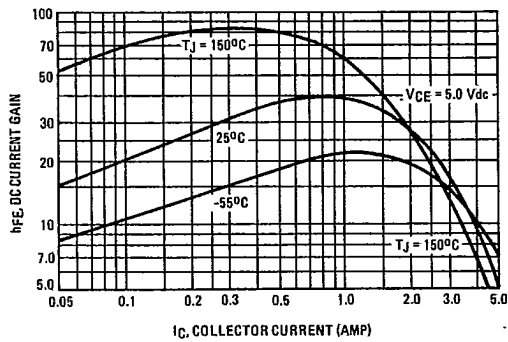


FIGURE 9 – "ON" VOLTAGES

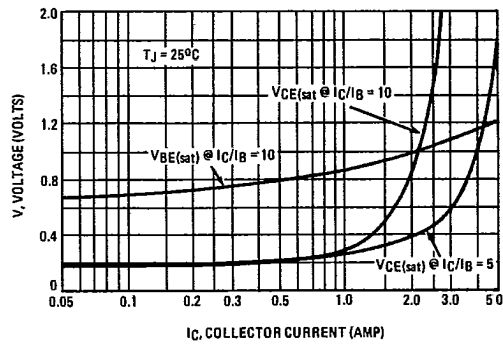


FIGURE 10 – COLLECTOR CUT-OFF REGION

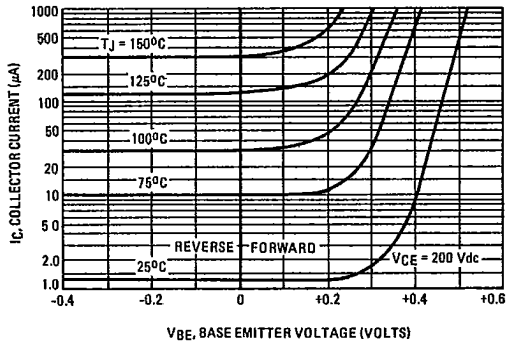


FIGURE 11 – TEMPERATURE COEFFICIENTS

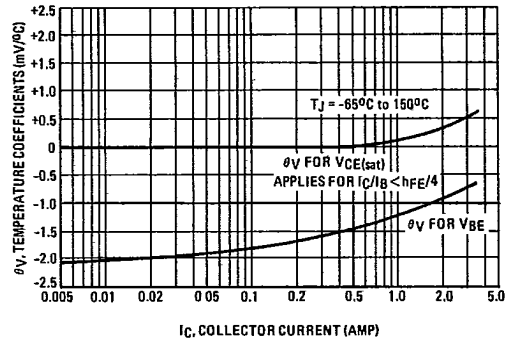
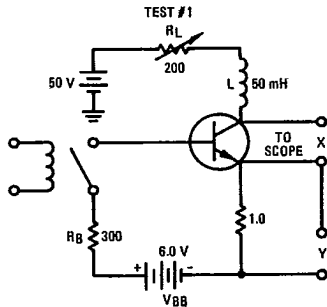
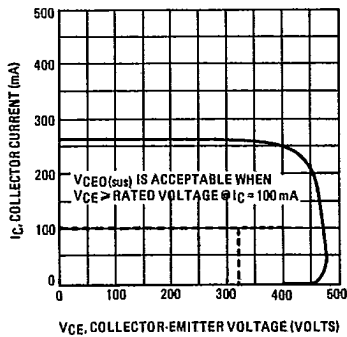


FIGURE 12 – COLLECTOR-EMITTER SUSTAINING VOLTAGE TEST CIRCUITS AND LOAD LINES



3