ESA8UN324(2/4)(A)-(60/70)(J/T)(G/S)-S

32MByte (8M x 32) CMOS EDO DRAM Module

General Description

The ESA8UN324(2/4)(A)-(60/70)(J/T)(G/S)-S is a high performance, EDO (Extended Data Out) 32-megabyte dynamic RAM module organized as 4M words by 32bits, in a 72-pin, leadless, single-in-line memory module (SIMM) package. ESA8UN3242(A) supports 2K refresh. ESA8UN3244(A) supports 4K refresh.

The module utilizes sixteen, Fujitsu MB811(7/6)405A-(60/70)PJ CMOS 4Mx4 EDO dynamic RAM in a surface mount package on an epoxy laminate substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

Control lines provided are such that byte control is possible.

Features

- High Density: 32MByte
- Fast Access Time of 60/70 ns (max.)
- Low Power: Active (60/70 ns)
  4.7/4.0 W (max.) - 2K
  3.4/2.9 W (max.) - 4K
  176mW (max.) - Standby (TTL)
  88mW (max.) - Standby (CMOS)
- TTL-compatible inputs and outputs
- Separate power and ground planes
- Single power supply of 5V±10%
- Height: 1.00 inch
- Devices: PCB accepts only 400mil QCAS device (ESA8UN3242)
  PCB accepts 300 and 400mil QCAS device (ESA8UN3242A)

ABSOLUTE MAXIMUM RATINGS

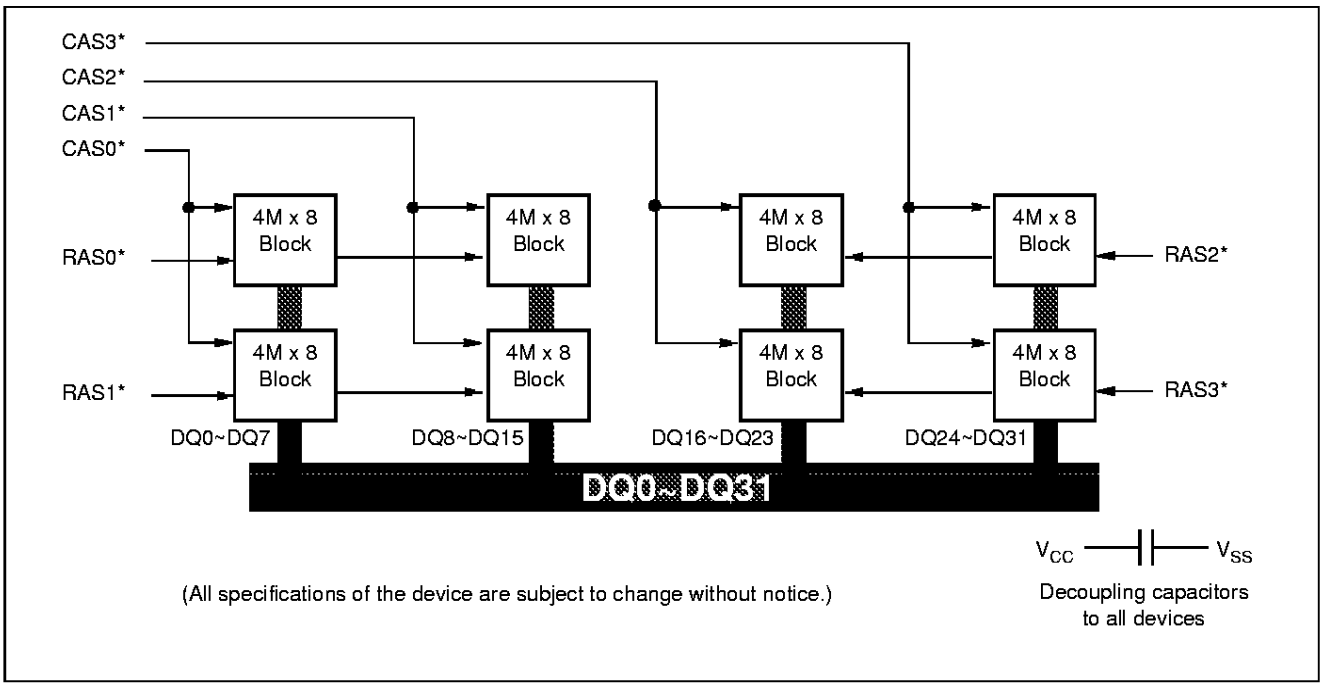
Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-1 to +7.0	V
Power Dissipation	P_T	8	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperate	T_{stg}	-55 to +125	°C
Short Circuit Output Current	I_{OS}	-50 to +50	mA

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0 to +70 °C)

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High voltage	2.4	-	V_{CC}+1	V
V_{IL}	Input Low voltage	-1	-	0.8	V

Functional Diagram



Notes:
1. A0 ~ A10/A11 to all devices (A11 is NC for 2K refresh module).
2. WE* to all devices.
3. OE* of all devices is grounded.
4. Each 4Mx8 Block consists of two 4Mx4 devices.

Pin Name

A0~A10†	Addresses for 2K Refresh Module	WE*	Write Enable
A0~A11	Row Addresses for 4K Refresh Module	PD1~PD4	Presence Detects
A0~A9	Column Addresses for 4K Refresh Module	V_{CC}	Power Supply
DQ0~DQ31	Data Inputs/Outputs	V_{SS}	Ground
CAS0*~CAS3*	Column Address Strobes	NC	No Connection
RAS0~RAS3	Row Address Strobes		

Presence Detect Pins

Pin	-60	-70
PD1	NC	NC
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation	Pin No.	Pin Designation
1	V_{SS}	19	A10	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	V_{SS}	57	DQ12
4	DQ1	22	DQ5	40	CAS0*	58	DQ28
5	DQ17	23	DQ21	41	CAS2*	59	V_{CC}
6	DQ2	24	DQ6	42	CAS3*	60	DQ29
7	DQ18	25	DQ22	43	CAS1*	61	DQ13
8	DQ3	26	DQ7	44	RAS0*	62	DQ30
9	DQ19	27	DQ23	45	RAS1*	63	DQ14
10	V_{CC}	28	A7	46	NC	64	DQ31
11	NC	29	A11†	47	WE*	65	DQ15
12	A0	30	V_{CC}	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ24	68	PD2
15	A3	33	RAS3*	51	DQ9	69	PD3
16	A4	34	RAS2*	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	V_{SS}

†: A11 is NC for 2K refresh module.

DC CHARACTERISTICS

(V_{CC} = 5.0V±10%, V_{SS} = 0V, T_A = 0 to +70 °C)

Parameter	Symbol	Test Condition	Refresh	60		70		Unit	Note
				Min.	Max.	Min.	Max.		
Operating Current	I_{CC1}	RAS*, CAS* cycling; t_{RC} = min.	2K	-	856	-	736	mA	1, 2
			4K	-	616	-	536		
Standby current	I_{CC2}	TTL Interface RAS*, CAS* = V_{IH} D_{out} = High-Z		-	32	-	32	mA	
		CMOS Interface RAS*, CAS* ≥ V_{cc} - 0.2V D_{out} = High-Z		-	16	-	16	mA	
RAS* -only Refresh Current	I_{CC3}	CAS* = V_{IH}; RAS*, Address cycling @ t_{RC} = min	2K	-	856	-	720	mA	2
			4K	-	616	-	536		
CAS*-before-RAS* Refresh Current	I_{CC4}	RAS*, CAS* cycling @ t_{RC} = min.	2K	-	856	-	736	mA	
			4K	-	616	-	536		
Fast Page Mode Current	I_{CC5}	RAS* = V_{IL}; CAS*, Address cycling @ t_{PC} = min	2K	-	856	-	736	mA	1, 3
			4K	-	616	-	536		
Input Leakage Current	I_{LI}	0V ≤ V_{in} ≤ V_{CC}+0.5V		-160	160	-160	160	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{out} ≤ V_{CC} D_{out} = Disable		-20	20	-20	20	µA	
Output High Voltage	V_{OH}	High I_{out} = -5 mA		2.4	-	2.4	-	V	
Output Low Voltage	V_{OL}	Low I_{out} = 4.5 mA		-	0.4	-	0.4	V	

Notes: 1. Values depend on load condition when the device is selected. Maximum Values are specified at the output open condition.
2. Address can be changed once or less while RAS* = V_{IL}.
3. Address can be changed once or less while CAS* = V_{IH}.

CAPACITANCE

(TA =+25°C, V_{CC} = 5.0V±10%=10V)

Parameter	Symbol	Max.	Unit	Note
Input Capacitance (Address)	C_{I1}	85	pF	1
Input Capacitance (RAS0*~RAS3*)	C_{I2}	25	pF	1
Input Capacitance (CAS0*~CAS3*)	C_{I3}	25	pF	1
Input Capacitance (WE*)	C_{I4}	85	pF	1
Input/Output Capacitance (DQ0~DQ31)	$C_{I/O}$	12	pF	1, 2

Notes: 1. Capacitance is measured with Boonton Meter or effective capacitance method.
2. CAS* = V_{IH} to disable D_{out}.

AC CHARACTERISTICS

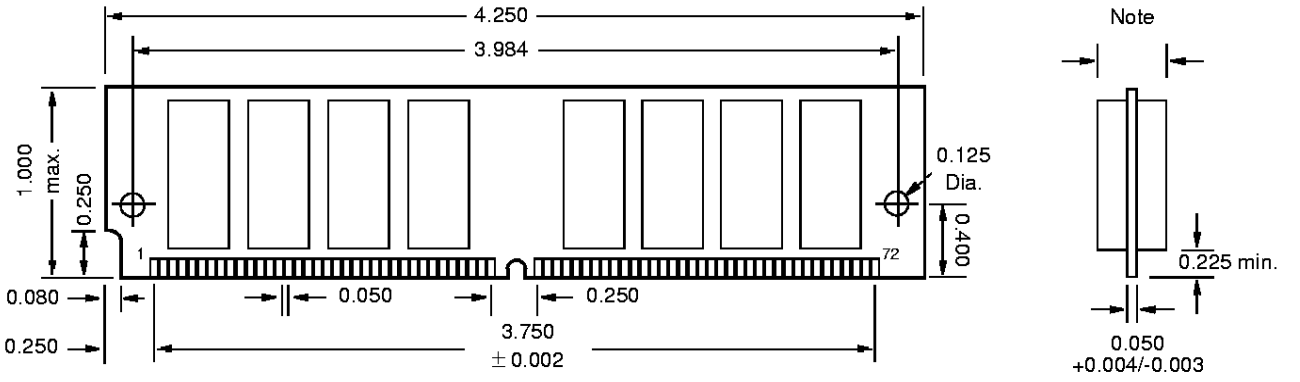
(TA = 0 to +70°C, V_{CC} = 5.0V±10%V, V_{SS} = 0V)

Parameter		Symbol	60		70		Unit	Notes
			Min	Max	Min	Max		
Random read/write cycle time		t_{RC}	110	-	130	-	ns	
Access time from RAS*		t_{RAC}	-	60	-	70	ns	3, 4
Access time from CAS*		t_{CAC}	-	15	-	20	ns	3, 4, 5
Access time from column address		t_{AA}	-	30	-	35	ns	3, 10
Output buffer turn-off time		t_{OFF}	0	15	0	17	ns	6
Transition time (rise and fall)		t_T	3	50	3	50	ns	2
RAS* precharge time		t_{RP}	40	-	50	-	ns	
RAS* pulse width		t_{RAS}	60	10000	70	10000	ns	
RAS* hold time		t_{RSH}	15	-	20	-	ns	
CAS* hold time		t_{CSH}	60	-	70	-	ns	
CAS* pulse width		t_{CAS}	15	10000	20	10000	ns	
RAS* to CAS* delay time		t_{RCD}	20	45	20	50	ns	4
RAS* to column address delay time		t_{RAD}	15	30	15	35	ns	10
CAS* to RAS* precharge time		t_{CRP}	5	-	5	-	ns	
Row address set-up time		t_{ASR}	0	-	0	-	ns	
Row address hold time		t_{RAH}	10	-	10	-	ns	
Column address set-up time		t_{ASC}	0	-	0	-	ns	
Column address hold time		t_{CAH}	12	-	15	-	ns	
Column address to RAS* lead time		t_{RAL}	30	-	35	-	ns	
Read command set-up time		t_{RCS}	5	-	5	-	ns	
Read command hold time to CAS*		t_{RCH}	0	-	0	-	ns	8
Read command hold time to RAS*		t_{RRH}	0	-	0	-	ns	
Write command hold time		t_{WCH}	12	-	15	-	ns	
Write command pulse width		t_{WP}	10	-	15	-	ns	
Write command to RAS* lead time		t_{RWL}	15	-	20	-	ns	
Write command to CAS* lead time		t_{CWL}	15	-	20	-	ns	
Data-in set-up time		t_{DS}	0	-	0	-	ns	9
Data-in hold time		t_{DH}	12	-	15	-	ns	9
Refresh period	(2048 cycles)	t_{REF}	-	32	-	32	ms	
	(4096 cycles)		-	64	-	64	ms	
Write command set-up time		t_{WCS}	0	-	0	-	ns	7
CAS* set-up time (CBR refresh)		t_{CSR}	10	-	10	-	ns	1
CAS* hold time (CBR refresh)		t_{CHR}	10	-	15	-	ns	1
RAS* precharge to CAS* hold time		t_{RPC}	5	-	5	-	ns	
Access time from CAS* precharge		t_{CPA}	-	35	-	40	ns	3, 11
Hyper Page mode cycle time		t_{HPC}	25	-	30	-	ns	
CAS* precharge time (Hyper Page)		t_{CP}	8	-	10	-	ns	
RAS* pulse width (Hyper Page)		t_{RASP}	—	200000	—	200000	ns	12

Notes:
1. An initial pulse of at least 200µs is required after power-up followed by a minimum of eight RAS* cycles before device operation is achieved.
2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumed to be 5 ns for all inputs.
3. Measure with a load equivalent of 2 TTL loads and 100pF.
4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) limit can be met; t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. This parameter defines the time at which the output achieves open circuit condition and is not referenced to V_{OH} or V_{OL}.
7. t_{WCS} is a non restrictive operating parameter. It is included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$(min.) the cycle is an early write cycle and the data-out pin will remain at high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the CAS* leading edge in early write cycles.
10. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
11. Access time is determined by the longer of t_{AA}, t_{CAC}, or t_{ACP}.
12. t_{RASC} defines RAS* pulse width in fast page mode cycles.

Physical Dimensions

72-pin SIMM



(All dimensions are in inches with ±0.005" tolerance unless otherwise specified. Do not scale drawing)

Notes: Thickness = 0.350 for SOJ DRAM
= 0.150 for TSOP DRAM

Ordering Information

E S A 8 U N 32 42 A _ - 60 J S - _ S

(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15)

(1) **Memory Type**
F : Fast Page Mode (FPM)
E : Extended Data Out (EDO)

(2) **Module Shape**
S : SIMM
D : DIMM
O : Small Outline DIMM

(3) **Module Pin Count**
A : 72-pin
B : 144-pin
C : 168-pin
D : 200-pin

(4) **Word Depth**
1 : 1M
2 : 2M
4 : 4M, etc.

(5) **Buffer Type**
B : Buffered
U : Unbuffered
R : Registered

(6) **Operating Voltage**
N : 5V
V : 3,3V

(7) **Data Width**
(ex. 8=x8, 32=x32, 72=x72 etc.)

(8) **Device Configuration / Refresh**
41 : 1Mx4, 1K Refresh Cycle
42 : 4Mx4, 2K Refresh Cycle
44 : 4Mx4, 4K Refresh Cycle
82 : 2Mx8, 2K Refresh Cycle
14 : 1Mx16, 4K Refresh Cycle
11 : 1Mx16, 1K Refresh Cycle

(9) **Module Revision *1**
Blank : Rev. 0
A : Rev. 1
B : Rev. 2 (etc.)

*1 When DRAM device or PCB is revised, the revision is changed

(10) **Power consumption**
Blank : Standard
L : Low Power

(11) **Speed**
50 : 50ns
60 : 60ns
70 : 70ns

(12) **Package of Component**
J : SOJ
T : TSOP

(13) **Module Lead Finish**
S : Solder Plate
G : Gold Plate

(14) **Private Brand Name *2**
Blank : Common Products
G : FMG Brand

*2 This column is applicable to custom modules, NOT applicable to JEDEC standard commodity products

(15) **Assembly & Test Site**
S : Smart Modular Technologies

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