Preliminary Information

1 Megabit Module XM28HC010 128K x 8 Bit

5 Volt, Byte Alterable High Speed E²PROM

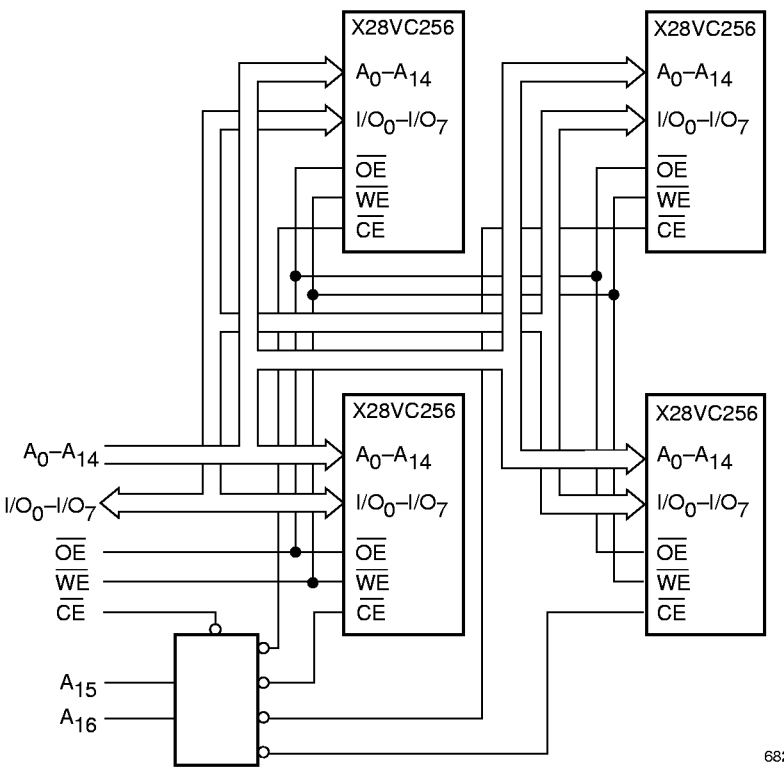
TYPICAL FEATURES

- High Speed 1 Megabit (128K x 8) E²PROM Module
- Access Time of 70 ns at –55°C to +125°C
- SIMPLE Byte and Page Write
  - —Single 5 Volt Supply
    - —No External High Voltages or V_{PP} Control Circuits
  - —Self Timed
    - —No Erase Before Write
    - —No Complex Programming Algorithms
    - —No Overerase Problem
- Base Memory Component: Xicor CMOS X28VC256
- JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package
- Pin Compatible with the X28C010 1Megabit Monolithic CMOS E²PROM
- Endurance: 100,000 Cycles
- Fast Write Cycle Times Supported by:
  - —Internal Program Cycle 5 ms Max.
  - —128-byte Page
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Status Bit
- High Rel Module Available with:
  - —100% MIL-STD-883 Compliant Components
- Software Data Protection

DESCRIPTION

The XM28HC010 is a high density 1 Megabit E²PROM comprised of four X28VC256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28HC010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28HC010.

FUNCTIONAL DIAGRAM



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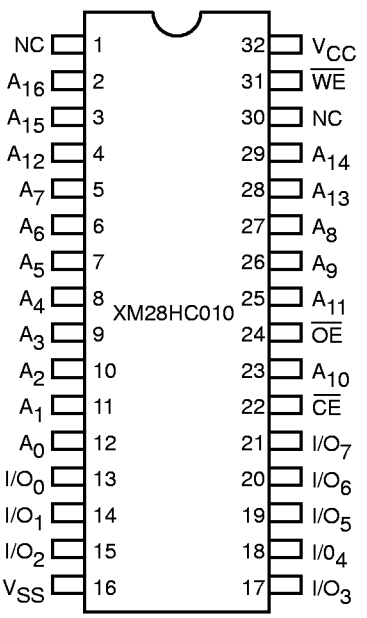
PIN CONFIGURATION



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DESCRIPTION (Cont.)

The XM28HC010 is available in commercial, industrial, and military temperature ranges. The High Rel module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28HC010 supports a 128-byte page write operation, this, combined with $\overline{DATA}$ Polling or Toggle Bit testing, effectively provides a 24µs/byte write cycle, enabling the module memory array to be rewritten in 3.2 seconds.

The XM28HC010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28HC010 provides the same high endurance and data retention as the base memory components.

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced (see Note 4).

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the XM28HC010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the XM28HC010.

PIN NAMES

Symbol	Description
A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

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DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The XM28HC010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms (see Note 4).

Page Write Operation

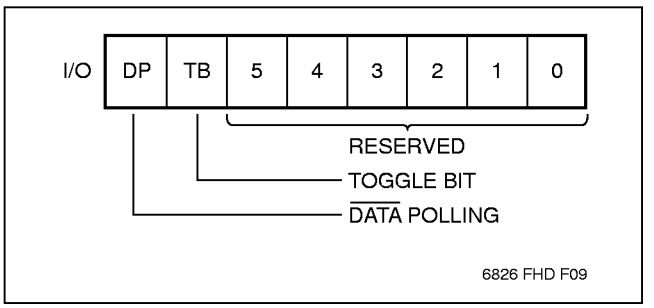
The page write feature of the XM28HC010 allows the entire memory to be written in 3.2 seconds. Page write allows two to 128 bytes of data to be consecutively written to the XM28HC010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to 127 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

Write Operation Status Bits

The XM28HC010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The XM28HC010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the XM28HC010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the XM28HC010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The XM28HC010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2. $\overline{\text{DATA}}$ Polling Bus Sequence

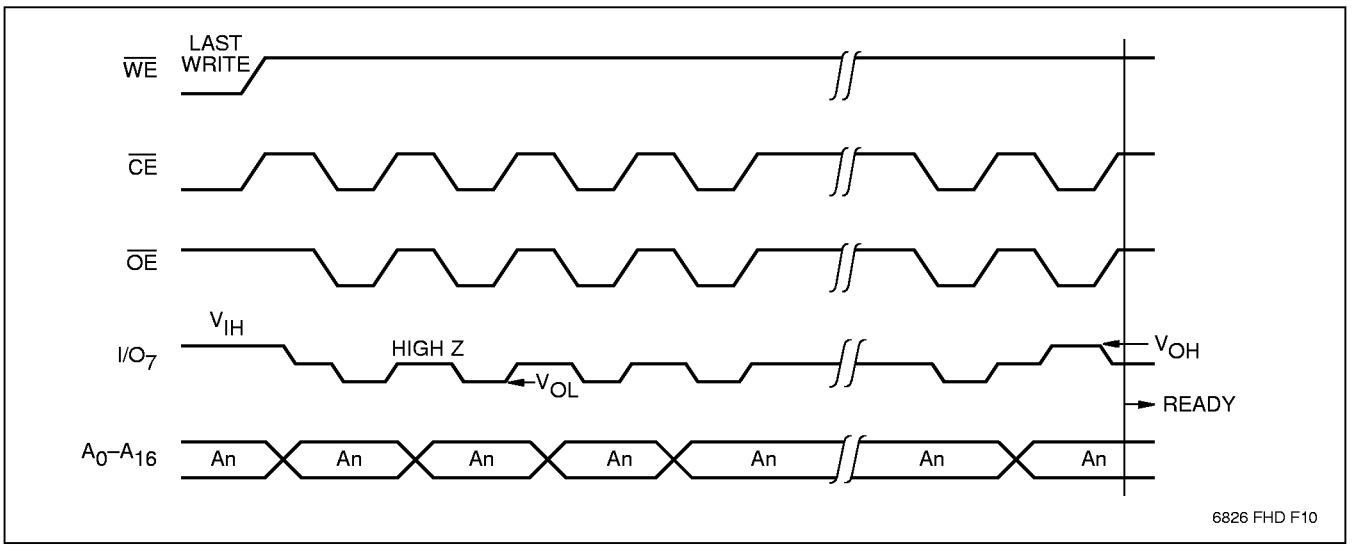
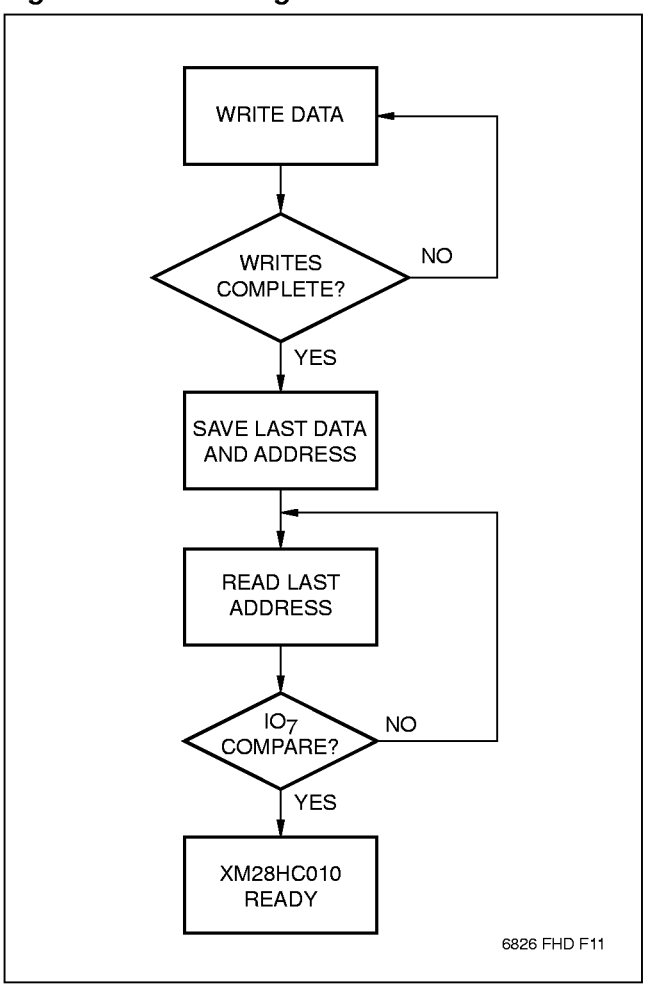


Figure 3. $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the XM28HC010. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

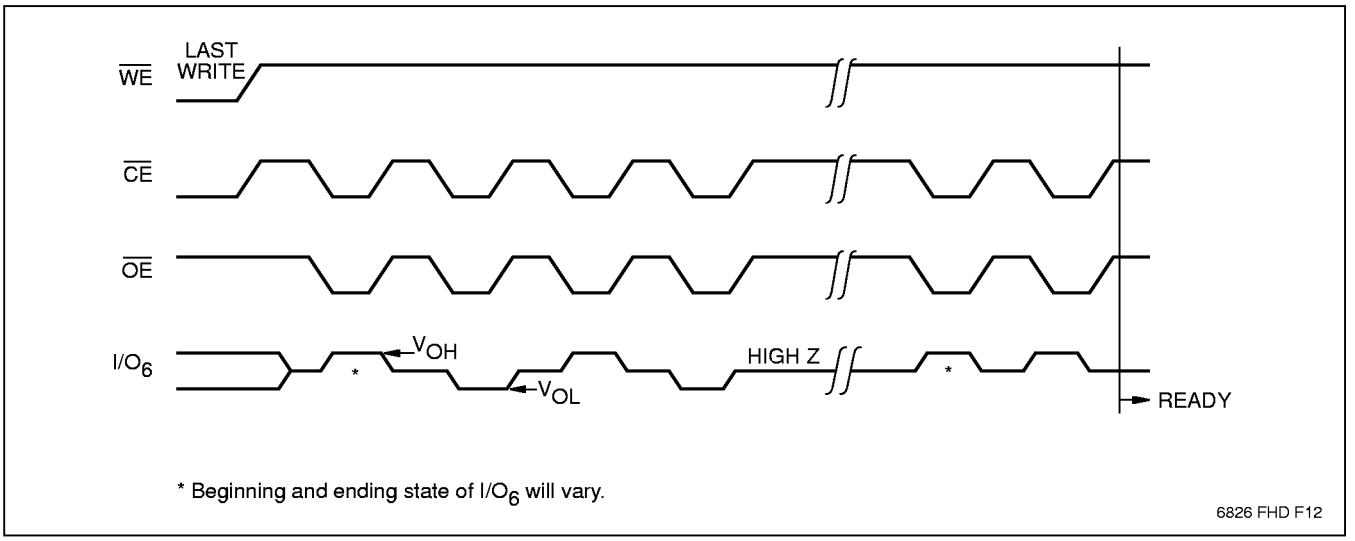
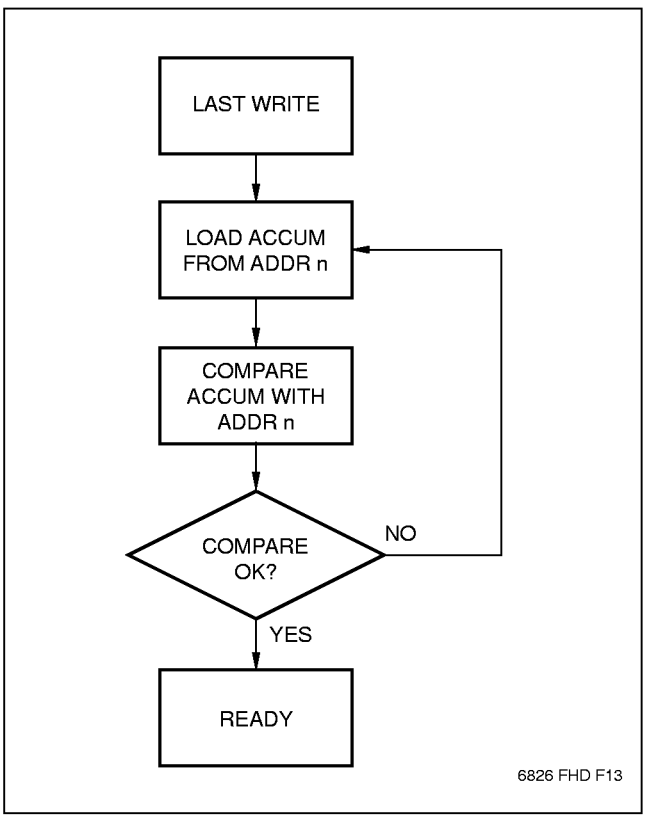


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple XM28HC010 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The XM28HC010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense—All functions are inhibited when V_{CC} is ≤ 3.5V.
- Write Inhibit—Holding $\overline{OE}$ LOW will prevent an inadvertent write cycle during power-on and power-off.

SOFTWARE DATA PROTECTION

The XM28HC010 does provide the Software Data Protection (SDP) feature. Because the module is comprised of four discrete X28VC256 LCCs, the algorithm will differ from the algorithm employed for the monolithic 1 Megabit X28HC010.

The module is shipped from Xicor with the Software Data Protection NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once V_{CC} is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described in the next section.

SOFTWARE COMMAND SEQUENCE

A_{15} and A_{16} are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 6 and 7. Because this involves writing to a nonvolatile bit the device will become protected after t_{WC} has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 8 and 9. This is a nonvolatile operation, and the host will have to wait a minimum t_{WC} before attempting to write new data.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

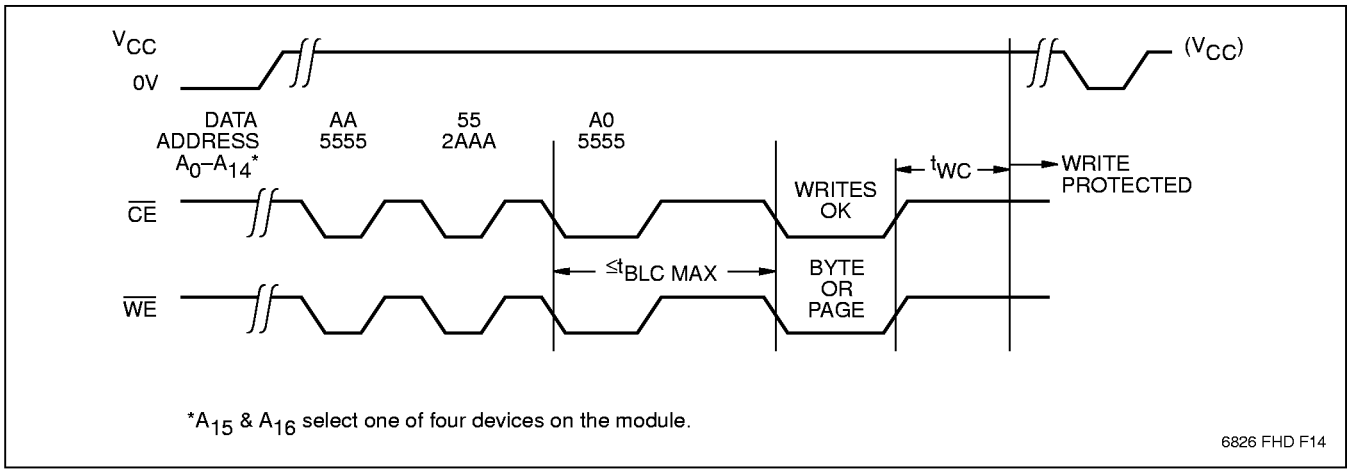
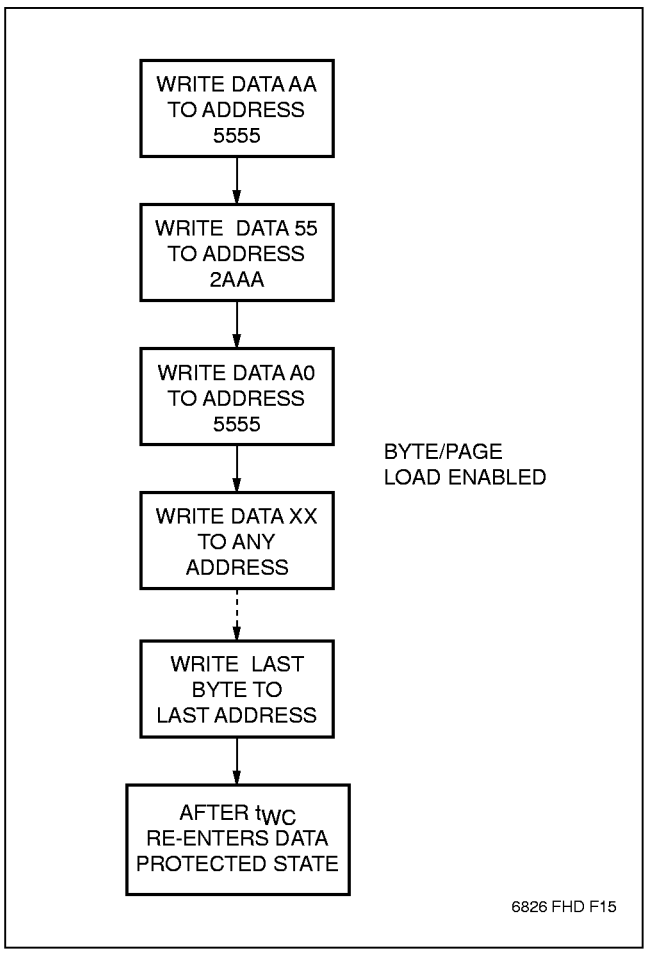


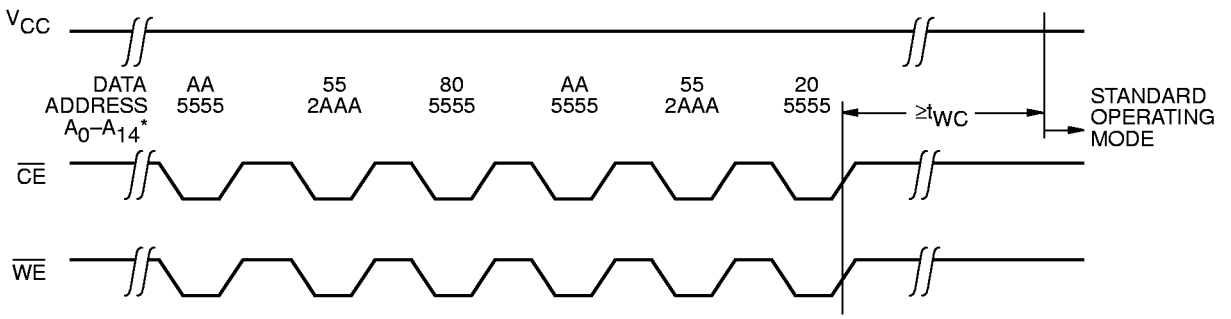
Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence



*A_{15} & A_{16} select one of four devices on the module.

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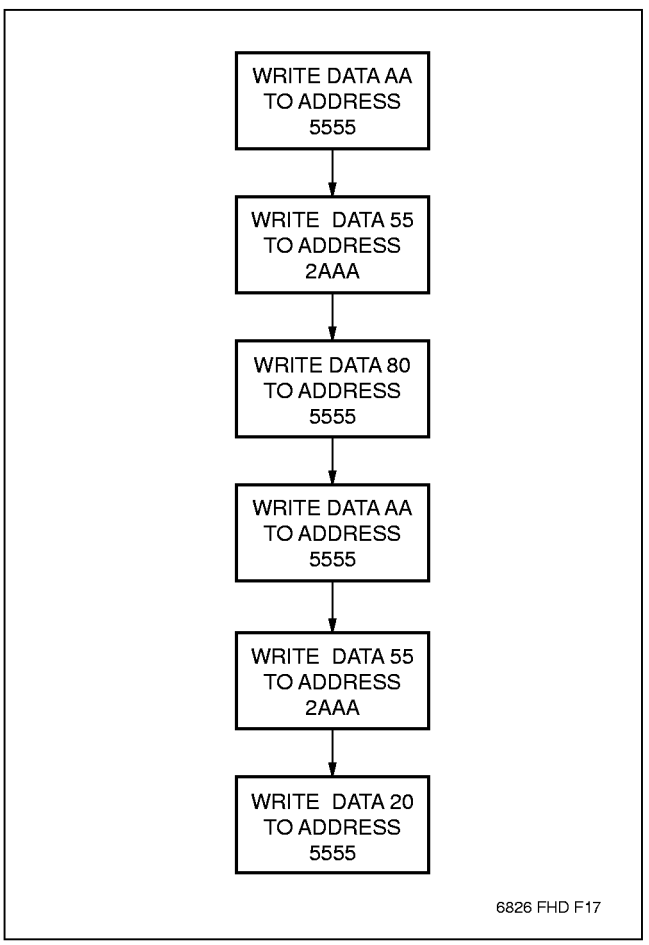
Figure 9. Software Sequence to Deactivate Software Data Protection



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In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the device will be in standard operating mode.

SYSTEM CONSIDERATIONS

Because the XM28HC010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28HC010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between V_{CC} and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... –1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

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D.C. OPERATING CHARACTERISTICS

XM28HC010 T_A = 0°C to +70°C, V_{CC} = +5V ± 10%, unless otherwise specified.
XM28HC010I T_A = –40°C to +85°C, V_{CC} = +5V ± 10%, unless otherwise specified.
XM28HC010M T_A = –55°C to +125°C, V_{CC} = +5V ± 10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active)		175	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O's = Open, 1 Device Active Address Inputs = .4V/2.4V Levels @ f = 10MHz
I_{SB}	V_{CC} Current (Standby) (TTL Inputs)		120	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O's = Open, Other Inputs = V_{IH}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}	Input Low Voltage	–0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 6 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –4 mA

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POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-up to Read Operation	100	µs
t_{PUW}(2)	Power-up to Write Operation	5	ms

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CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Test Conditions
$C_{I/O}$(2)	Input/Output Capacitance	40	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	24	pF	V_{IN} = 0V

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Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100pF

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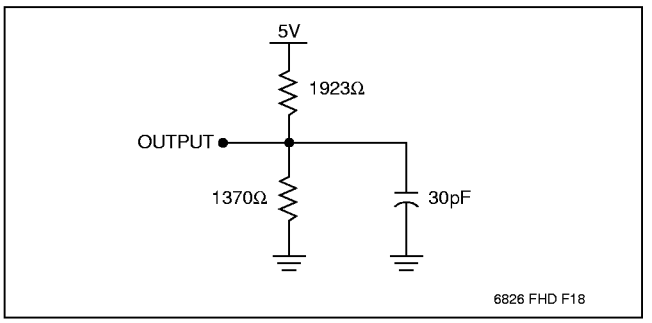
EQUIVALENT A.C. LOAD CIRCUIT



A.C. CHARACTERISTICS

XM28HC010 T_A = 0°C to + 70°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28HC010I T_A = –40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28HC010M T_A = –55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	XM28HC010-70		XM28HC010-90		XM28HC010-120		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70		90		120		ns
t_{CE}	Chip Enable Access Time		70		90		120	ns
t_{AA}	Address Access Time		70		90		120	ns
t_{OE}	Output Enable Access Time		35		40		50	ns
t_{LZ}(3)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output		35		40		50	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output		35		40		50	ns
t_{OH}	Output Hold from Address	0		0		0		ns

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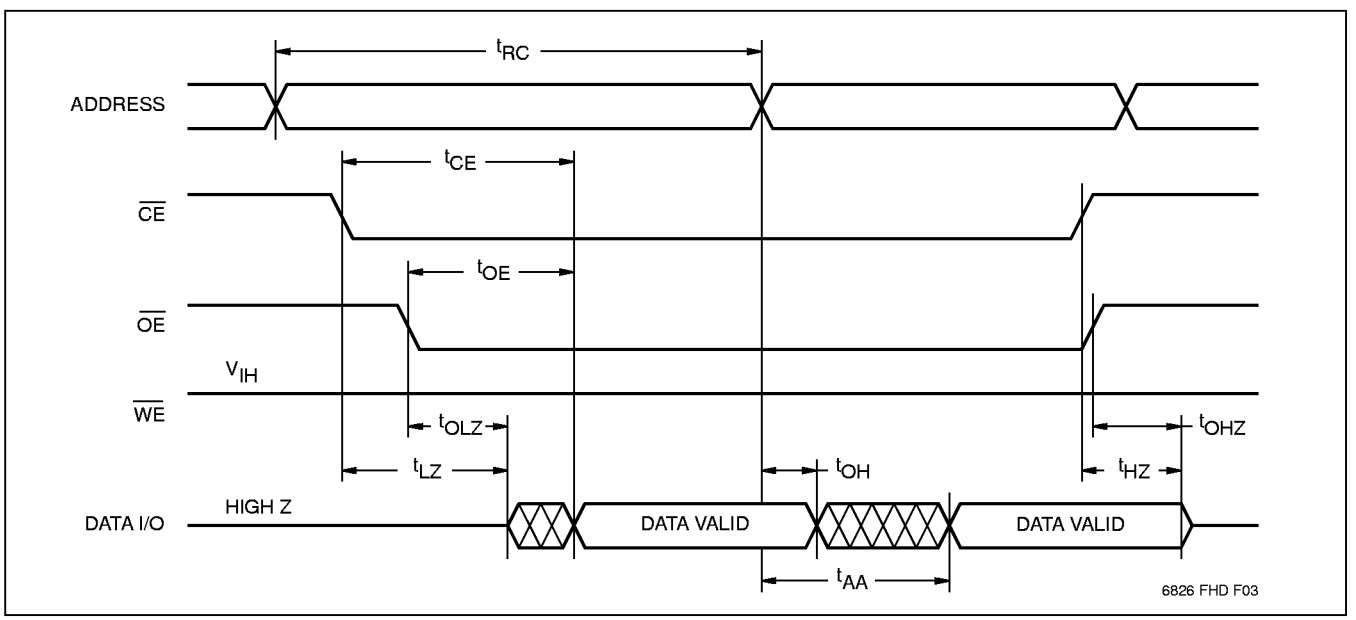
Read Cycle



Note: (3) t_{LZ} and t_{OLZ} are shown for reference only, they are periodically characterized and are not 100% tested.
(4) t_{HZ} and t_{OHZ} are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

Symbol	Parameter	$\overline{WE}$ Controlled Write		$\overline{CE}$ Controlled Write (5)		Units
		Min.	Max.	Min.	Max.	
t_{WC}(6)	Write Cycle Time		5		5	ms
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	50		75		ns
t_{CS}	Write Setup Time	25		0		ns
t_{CH}	Write Hold Time	0		25		ns
t_{CW}	$\overline{CE}$ Pulse Width	75		75		ns
t_{OES}	$\overline{OE}$ High Setup Time	0		0		ns
t_{OEH}	$\overline{OE}$ High Hold Time	0		25		ns
t_{WP}	$\overline{WE}$ Pulse Width	50		75		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		100		ns
t_{DV}	Data Valid		1		1	µs
t_{DS}	Data Setup	50		50		ns
t_{DH}	Data Hold	0		25		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	0.150	100	0.150	100	µs

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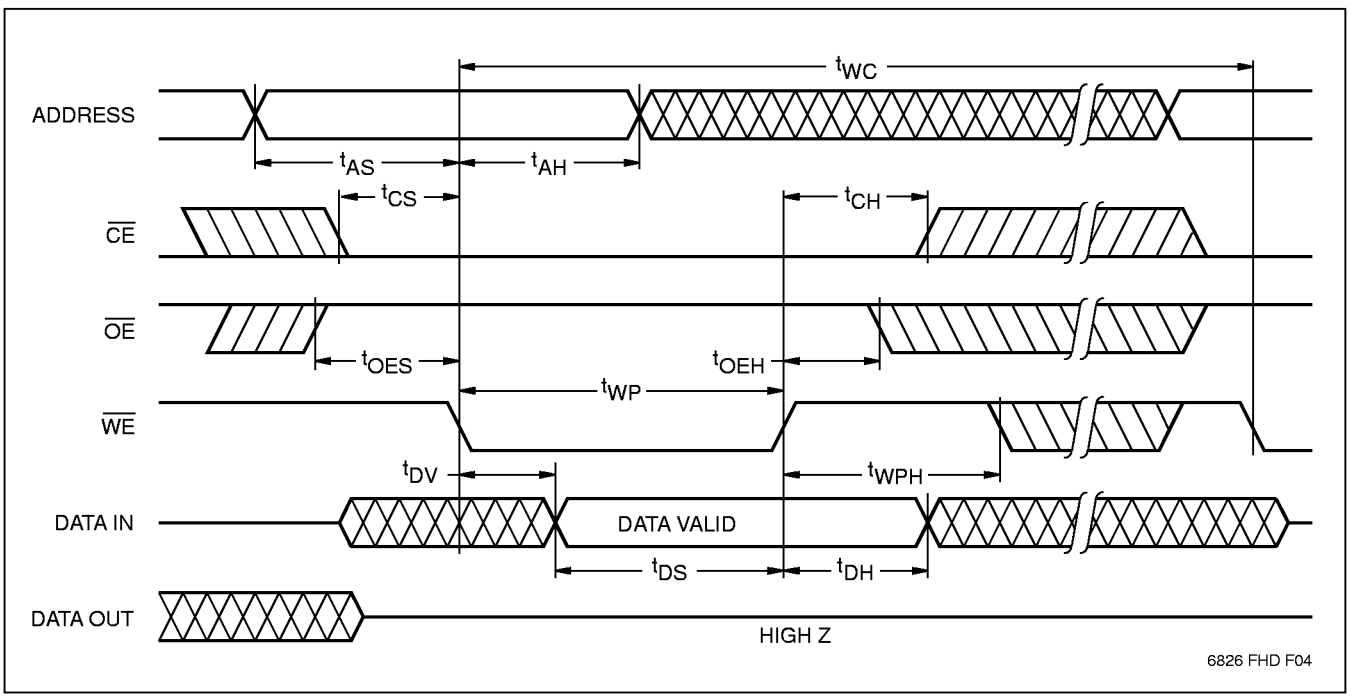
$\overline{WE}$ Controlled Write Cycle



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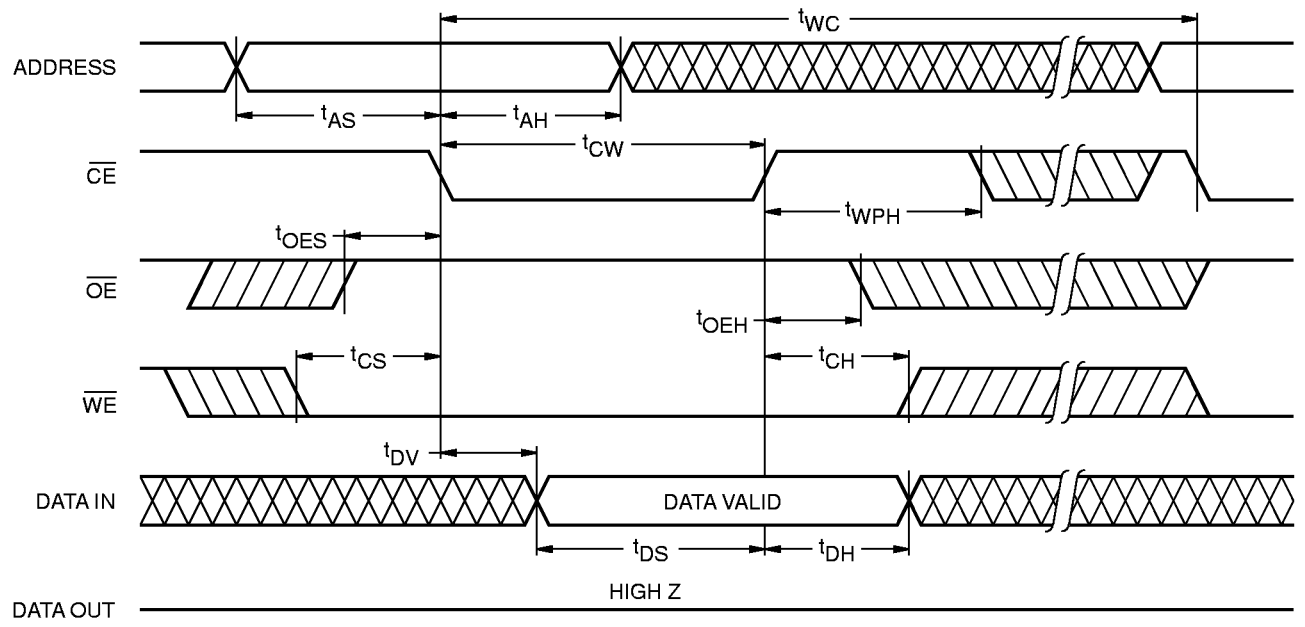
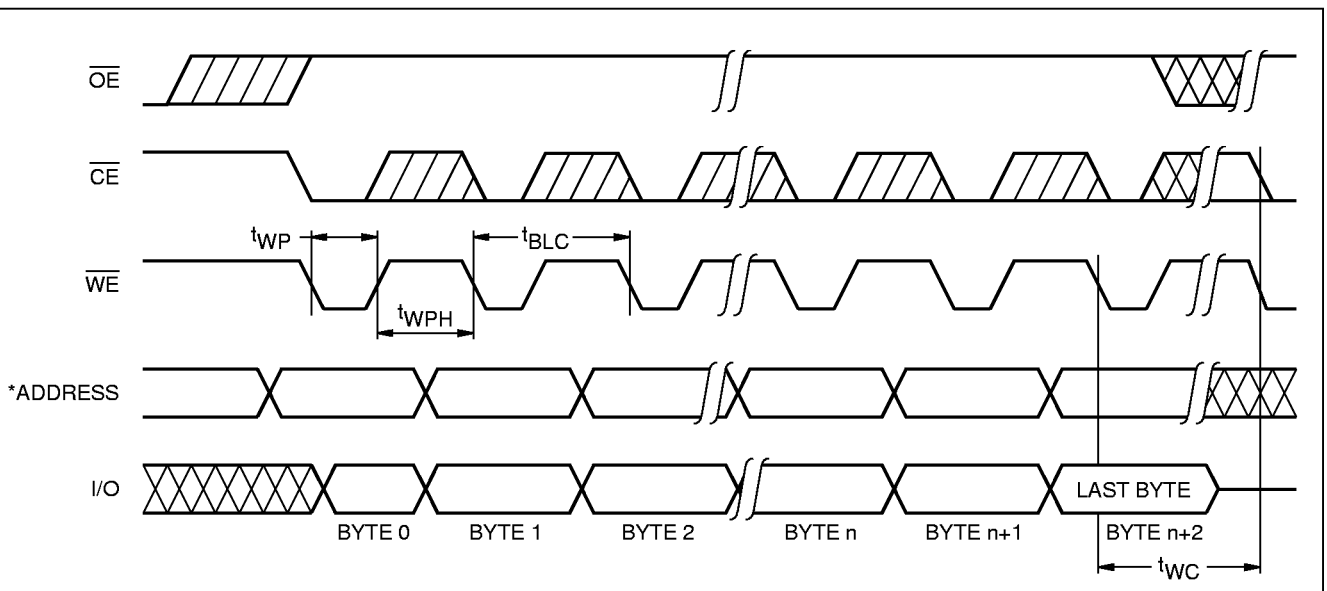
Note: (5) Due to the inclusion of the decoder IC on board the module the $\overline{WE}$ and $\overline{CE}$ write controlled timings will vary. When utilizing the $\overline{CE}$ controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a $\overline{WE}$ controlled write operation $\overline{CE}$ must be a minimum 125 ns to accommodate the additional setup time required.

(6) tWC is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to complete the interval write operation.

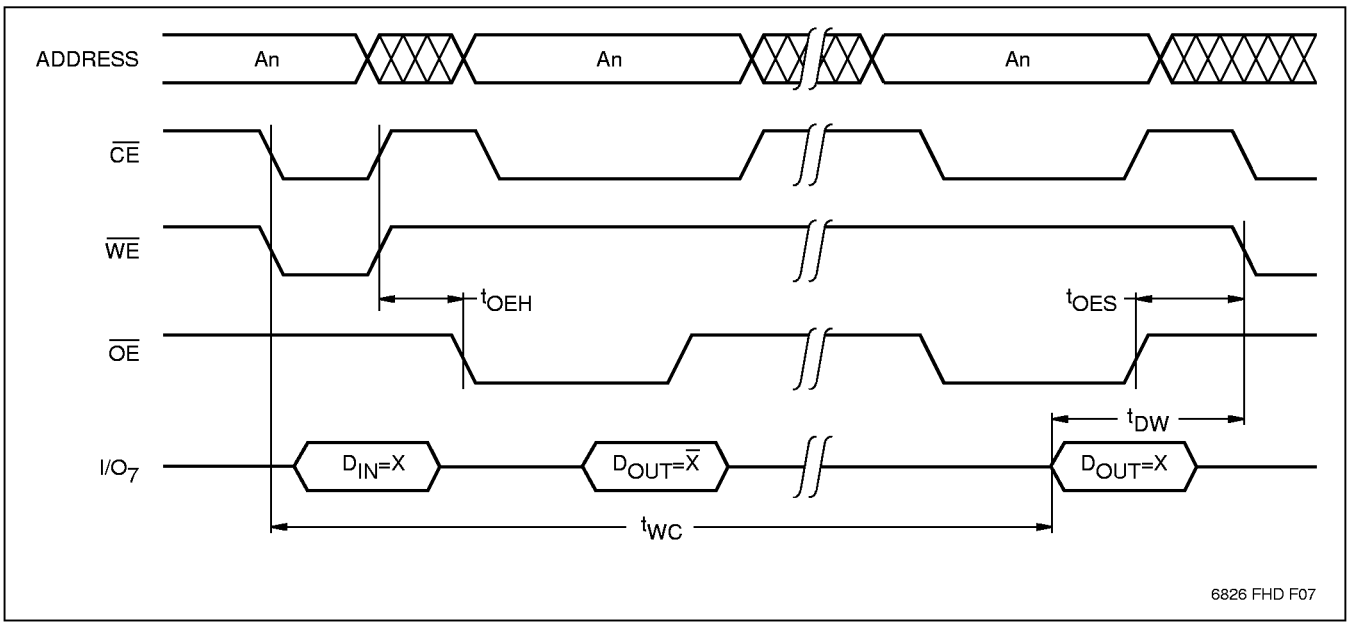
$\overline{CE}$ Controlled Write Cycle



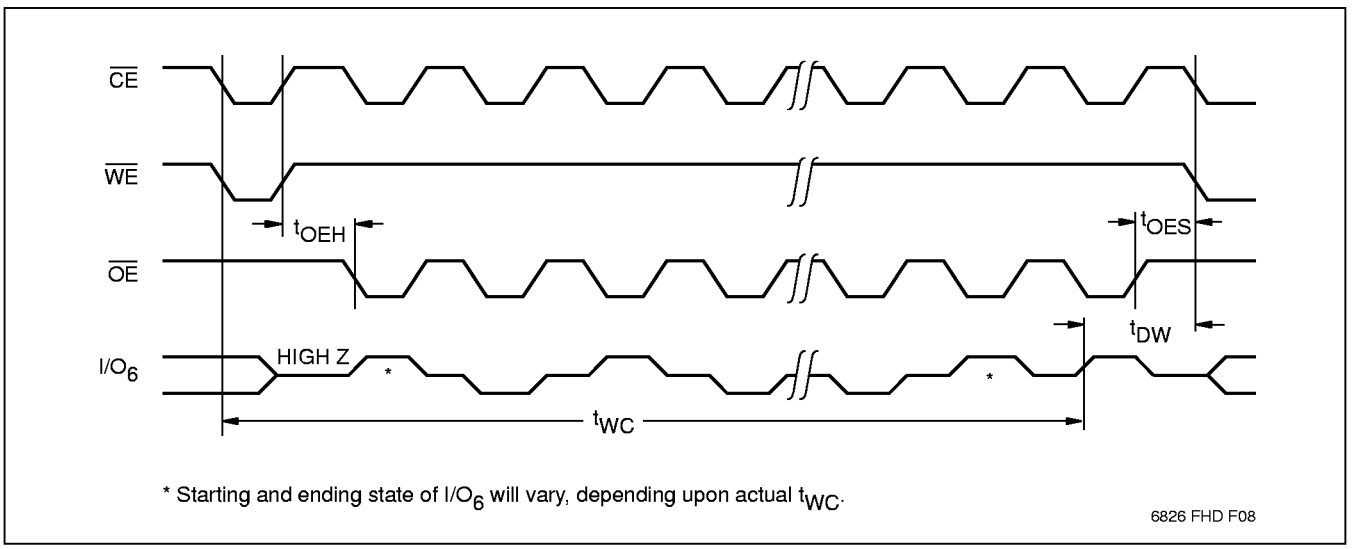
Page Write Cycle



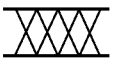
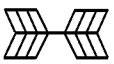
$\overline{\text{DATA}}$ Polling Timing Diagram



Toggle Bit Timing Diagram



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

1 Megabit Puma Module XM28HC010P 32K x 32 Bit

High Speed 5 Volt Byte Alterable Nonvolatile Memory Array

FEATURES

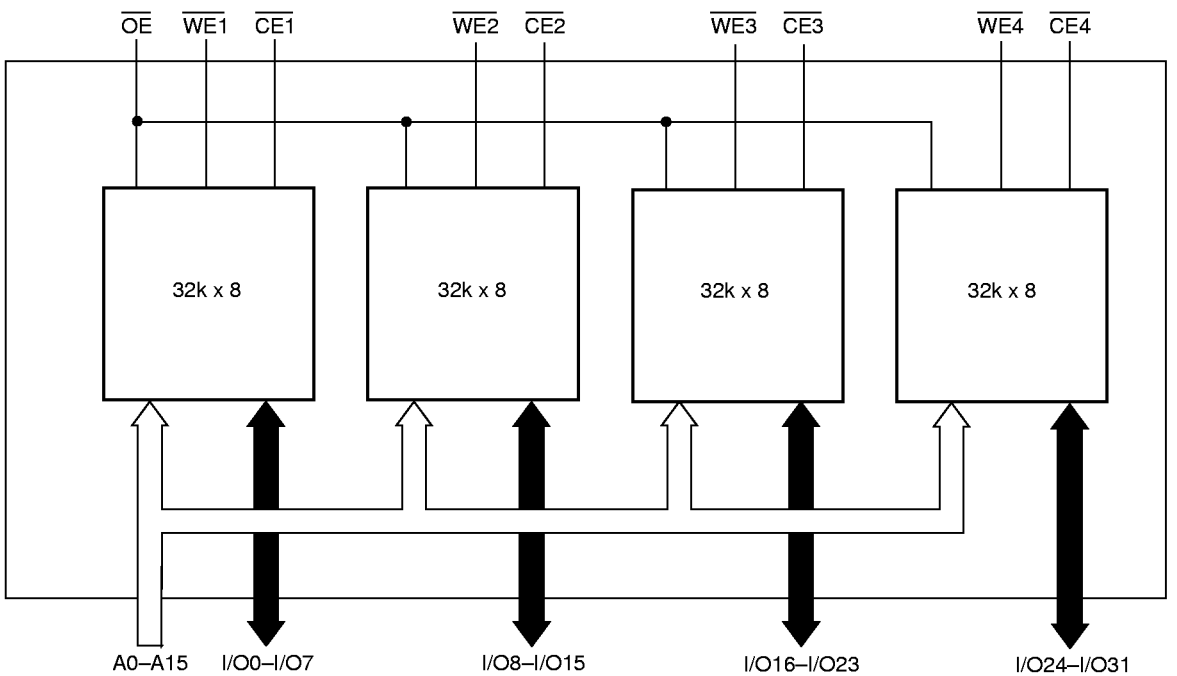
- **High Speed, High Density Memory Module**
  - **—120ns, 90ns and 70ns Access Times Available**
  - **—1 Megabit Memory in 1 square inch.**
- **Flexible Multiplane Architecture**
  - **—Four Separate Chip Selects**
  - **—32 Separate I/Os**
    - **User Configurable I/Os—x8, x16, or x32**
    - **User Configurable Page Size—64 Doublewords, 128 Words, or 256 Bytes**
  - **—Concurrent Read/Write Operations**
    - **Able to Continue Reading During a Nonvolatile Write Cycle.**
- **5 Volt Byte or Page Alterable**
  - **—No Erase Before Write**
- **Software Data Protection**
- **Early End of Write Polling**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit Polling**
- **High Reliability**
  - **—Endurance: 100,000 Cycles**
  - **—Data Retention: 100 Years**

DESCRIPTION

The XM28HC010P is a high speed, high density CMOS byte alterable nonvolatile memory array constructed on a co-fired ceramic substrate using Xicor's High Speed 32K x 8 components in 32-pad leadless chip carriers. The Substrate is a 66-pin ceramic pin grid array.

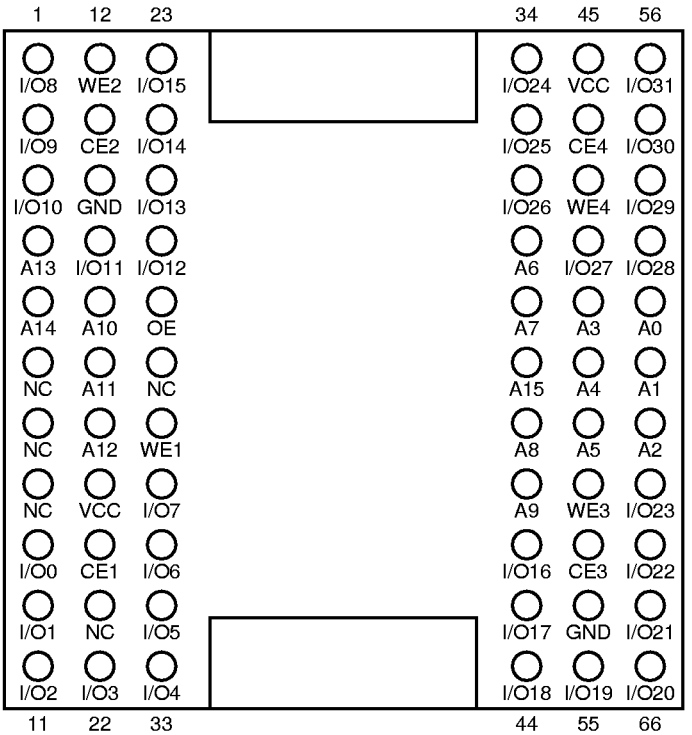
The module is configured with four separate chip enable and write enable inputs and 32 separate I/Os. This, along with the small footprint, provides the end user with a large degree of flexibility in board layout and memory configuration. In addition, with the large number of pins and the growth path being implemented, the module will be able to grow to 16 megabits.

FUNCTIONAL DIAGRAM

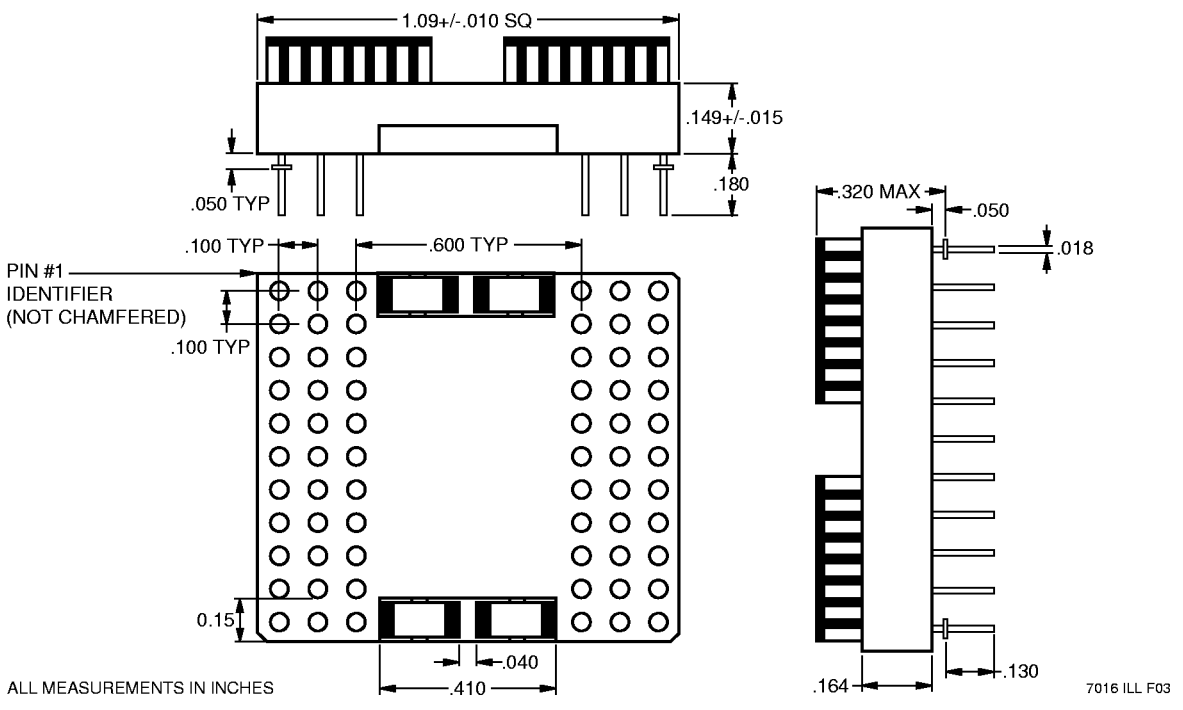


7016 ILL F01

PIN CONFIGURATION

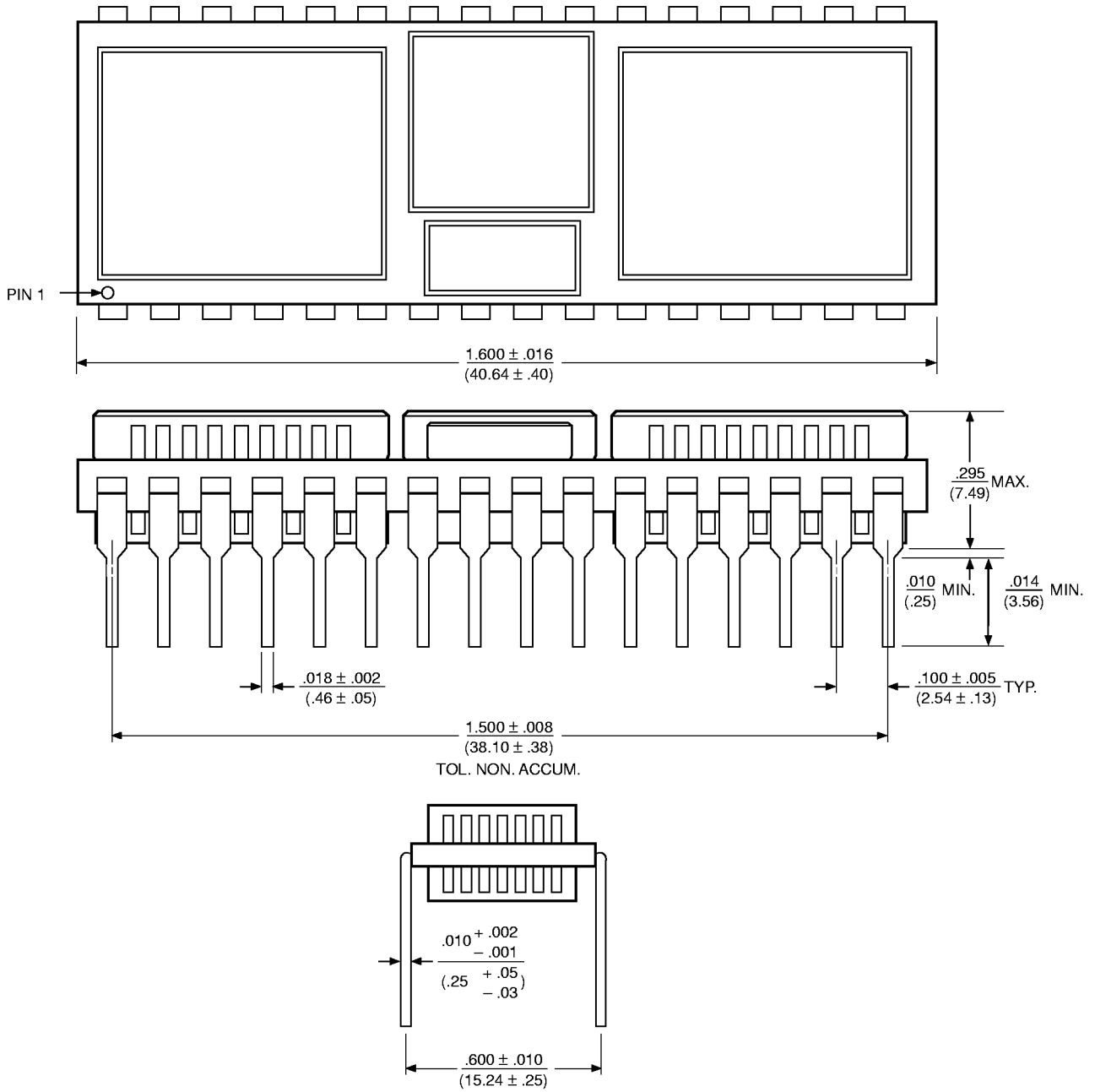


PACKAGE INFORMATION



PACKAGING INFORMATION

32-PIN DUAL-IN-LINE PACKAGE
CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE



NOTES:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY**

3926 FHD F12

ORDERING INFORMATION
1 MEGABIT E^2 MODULES