

**PowerStore 512 x 8 nvSRAM**

**Features**

- High-performance CMOS non-volatile static RAM 512 x 8 bits
- 25 and 45 ns Access Times
- 12 and 25 ns Output Enable Access Times
- I<sub>CC</sub> = 15 mA at 200 ns Cycle Time
- Unlimited Read and Write to SRAM
- Automatic STORE to EEPROM on Power Down using system capacitance
- Automatic STORE Timing
- 10<sup>5</sup> STORE cycles to EEPROM
- 10 years data retention in EEPROM
- Automatic RECALL on Power Up
- Unlimited RECALL cycles from EEPROM
- Single 5 V ± 10 % Operation
- Operating temperature ranges:  
0 to 70 °C  
-40 to 85 °C
- CECC 90000 Quality Standard
- ESD characterization according MIL STD 883C M3015.7-HBM
- Packages: PDIP24 (600 mil)  
SOP24 (300 mil)

**Description**

The U636H04 has two separate modes of operation: SRAM mode and nonvolatile mode.

In SRAM mode, the memory operates as an ordinary static RAM. In nonvolatile operation, data is transferred in parallel from SRAM to EEPROM or from EEPROM to SRAM.

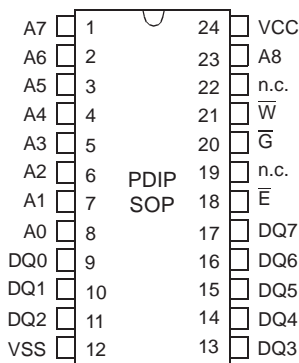
In this mode SRAM functions are disabled.

The U636H04 is a fast static RAM (25 and 45 ns), with a nonvolatile electrically erasable PROM (EEPROM) element incorporated in each static memory cell. Data transfers from the SRAM to the EEPROM (the STORE operation) take place automatically upon power down using charge stored in system capacitance. Transfers from the EEPROM to the SRAM (the RECALL operation) take place automatically on power up.

The SRAM can be read and written an unlimited number of times, while independent nonvolatile data resides in EEPROM.

The U636H04 combines the high performance and ease of use of a fast SRAM with nonvolatile data integrity.

**Pin Configuration**

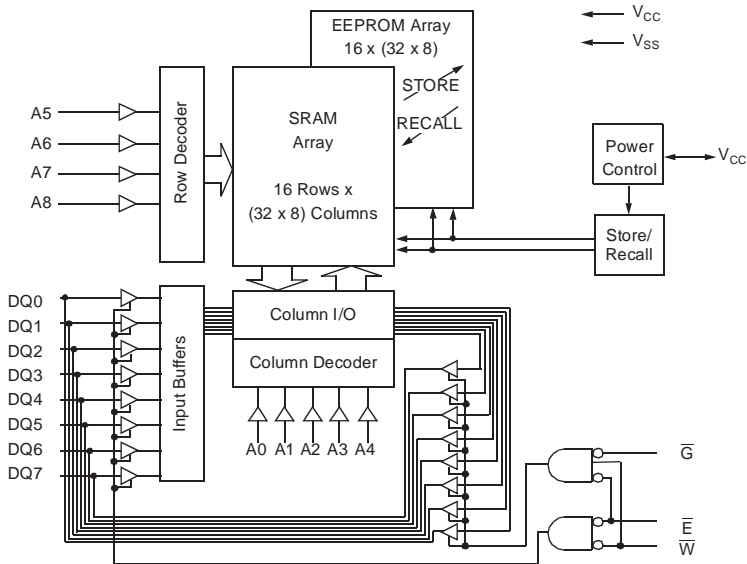


Top View

**Pin Description**

Signal Name	Signal Description
A0 - A8	Address Inputs
DQ0 - DQ7	Data In/Out
$\bar{E}$	Chip Enable
$\bar{G}$	Output Enable
$\bar{W}$	Write Enable
VCC	Power Supply Voltage
VSS	Ground

Block Diagram



Truth Table for SRAM Operations

Operating Mode	$\bar{E}$	$\bar{W}$	$\bar{G}$	DQ0 - DQ7
Standby/not selected	H	*	*	High-Z
Internal Read	L	H	H	High-Z
Read	L	H/O	L	Data Outputs Low-Z
Write	L	L	*	Data Inputs High-Z

\* H or L

Characteristics

All voltages are referenced to  $V_{SS} = 0$  V (ground).

All characteristics are valid in the power supply voltage range and in the operating temperature range specified.

Dynamic measurements are based on a rise and fall time of  $\leq 5$  ns, measured between 10 % and 90 % of  $V_I$ , as well as input levels of  $V_{IL} = 0$  V and  $V_{IH} = 3$  V. The timing reference level of all input and output signals is 1.5 V,

with the exception of the  $t_{dis}$ -times and  $t_{en}$ -times, in which cases transition is measured  $\pm 200$  mV from steady-state voltage.

Absolute Maximum Ratings <sup>a</sup>	Symbol	Min.	Max.	Unit
Power Supply Voltage	$V_{CC}$	-0.5	7	V
Input Voltage	$V_I$	-0.3	$V_{CC}+0.5$	V
Output Voltage	$V_O$	-0.3	$V_{CC}+0.5$	V
Power Dissipation	$P_D$		1	W
Operating Temperature	C-Type	$T_a$	0	$^{\circ}C$
	K-Type		-40	$^{\circ}C$
Storage Temperature	$T_{stg}$	-65	150	$^{\circ}C$

a: Stresses greater than those listed under „Absolute Maximum Ratings“ may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions	Symbol	Conditions	Min.	Max.	Unit
Power Supply Voltage	$V_{CC}$		4.5	5.5	V
Input Low Voltage	$V_{IL}$	-2 V at Pulse Width 10 ns permitted	-0.3	0.8	V
Input High Voltage	$V_{IH}$		2.2	$V_{CC} + 0.3$	V

DC Characteristics	Symbol	Conditions	C-Type		K-Type		Unit
			Min.	Max.	Min.	Max.	
Operating Supply Current <sup>b</sup>	$I_{CC1}$	$V_{CC} = 5.5\text{ V}$ $V_{IL} = 0.8\text{ V}$ $V_{IH} = 2.2\text{ V}$  $t_c = 25\text{ ns}$ $t_c = 45\text{ ns}$		90 75		95 80	mA mA
Average Supply Current during STORE <sup>c</sup>	$I_{CC2}$	$V_{CC} = 5.5\text{ V}$ $\overline{E} \leq 0.2\text{ V}$ $\overline{W} \geq V_{CC} - 0.2\text{ V}$ $V_{IL} \leq 0.2\text{ V}$ $V_{IH} \geq V_{CC} - 0.2\text{ V}$		6		7	mA
Average Supply Current during PowerStore Cycle <sup>c</sup>	$I_{CC4}$	$V_{CC} = 4.5\text{ V}$ $V_{IL} = 0.2\text{ V}$ $V_{IH} \geq V_{CC} - 0.2\text{ V}$		4		4	mA
Standby Supply Current <sup>d</sup> (Cycling TTL Input Levels)	$I_{CC(SB1)}$	$V_{CC} = 5.5\text{ V}$ $\overline{E} = V_{IH}$ $t_c = 25\text{ ns}$ $t_c = 45\text{ ns}$		30 20		34 23	mA mA
Operating Supply Current at $t_{cR} = 200\text{ ns}$ <sup>b</sup> (Cycling CMOS Input Levels)	$I_{CC3}$	$V_{CC} = 5.5\text{ V}$ $\overline{W} \geq V_{CC} - 0.2\text{ V}$ $V_{IL} \leq 0.2\text{ V}$ $V_{IH} \geq V_{CC} - 0.2\text{ V}$		15		15	mA
Standby Supply Current <sup>d</sup> (Stable CMOS Input Levels)	$I_{CC(SB)}$	$V_{CC} = 5.5\text{ V}$ $\overline{E} \geq V_{CC} - 0.2\text{ V}$ $V_{IL} \leq 0.2\text{ V}$ $V_{IH} \geq V_{CC} - 0.2\text{ V}$		3		3	mA

b:  $I_{CC1}$  and  $I_{CC3}$  are dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded. The current  $I_{CC1}$  is measured for WRITE/READ - ratio of 1/2.

c:  $I_{CC2}$  and  $I_{CC4}$  are the average currents required for the duration of the respective STORE cycles (STORE Cycle Time).

d: Bringing  $\overline{E} \geq V_{IH}$  will not produce standby current levels until any nonvolatile cycle in progress has timed out. See MODE SELECTION table. The current  $I_{CC(SB1)}$  is measured for WRITE/READ - ratio of 1/2.

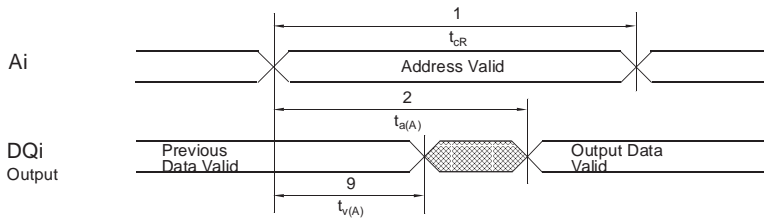
DC Characteristics	Symbol	Conditions	C-Type		K-Type		Unit
			Min.	Max.	Min.	Max.	
Output High Voltage Output Low Voltage	$V_{OH}$ $V_{OL}$	$V_{CC} = 4.5\text{ V}$ $I_{OH} = -4\text{ mA}$ $I_{OL} = 8\text{ mA}$	2.4	0.4	2.4	0.4	V V
Output High Current Output Low Current	$I_{OH}$ $I_{OL}$	$V_{CC} = 4.5\text{ V}$ $V_{OH} = 2.4\text{ V}$ $V_{OL} = 0.4\text{ V}$	8	-4	8	-4	mA mA
Input Leakage Current  High Low	$I_{IH}$ $I_{IL}$	$V_{CC} = 5.5\text{ V}$ $V_{IH} = 5.5\text{ V}$ $V_{IL} = 0\text{ V}$	-1	1	-1	1	$\mu\text{A}$ $\mu\text{A}$
Output Leakage Current  High at Three-State- Output Low at Three-State- Output	$I_{OHZ}$ $I_{OLZ}$	$V_{CC} = 5.5\text{ V}$ $V_{OH} = 5.5\text{ V}$ $V_{OL} = 0\text{ V}$	-1	1	-1	1	$\mu\text{A}$ $\mu\text{A}$

SRAM MEMORY OPERATIONS

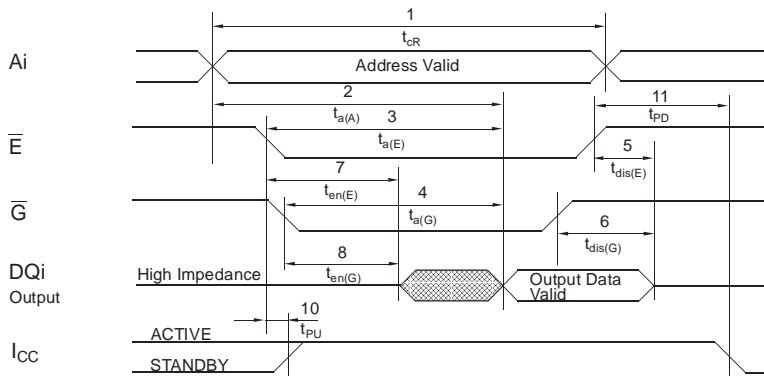
No.	Switching Characteristics Read Cycle	Symbol		25		45		Unit
		Alt.	IEC	Min.	Max.	Min.	Max.	
1	Read Cycle Time <sup>f</sup>	$t_{AVAV}$	$t_{cR}$	25		45		ns
2	Address Access Time to Data Valid <sup>g</sup>	$t_{AVQV}$	$t_{a(A)}$		25		45	ns
3	Chip Enable Access Time to Data Valid	$t_{ELQV}$	$t_{a(E)}$		25		45	ns
4	Output Enable Access Time to Data Valid	$t_{GLQV}$	$t_{a(G)}$		12		25	ns
5	$\overline{E}$ HIGH to Output in High-Z <sup>h</sup>	$t_{EHQZ}$	$t_{dis(E)}$		13		20	ns
6	$\overline{G}$ HIGH to Output in High-Z <sup>h</sup>	$t_{GHQZ}$	$t_{dis(G)}$		13		20	ns
7	$\overline{E}$ LOW to Output in Low-Z	$t_{ELQX}$	$t_{en(E)}$	5		5		ns
8	$\overline{G}$ LOW to Output in Low-Z	$t_{GLQX}$	$t_{en(G)}$	0		0		ns
9	Output Hold Time after Address Change	$t_{AXQX}$	$t_{v(A)}$	3		3		ns
10	Chip Enable to Power Active <sup>e</sup>	$t_{ELICCH}$	$t_{PU}$	0		0		ns
11	Chip Disable to Power Standby <sup>d, e</sup>	$t_{EHICCL}$	$t_{PD}$		25		45	ns

e: Parameter guaranteed but not tested.  
 f: Device is continuously selected with  $\overline{E}$  and  $\overline{G}$  both LOW.  
 g: Address valid prior to or coincident with  $\overline{E}$  transition LOW.  
 h: Measured  $\pm 200\text{ mV}$  from steady state output voltage.

Read Cycle 1: Ai-controlled (during Read cycle:  $\bar{E} = \bar{G} = V_{IL}$ ,  $\bar{W} = V_{IH}$ )<sup>f</sup>

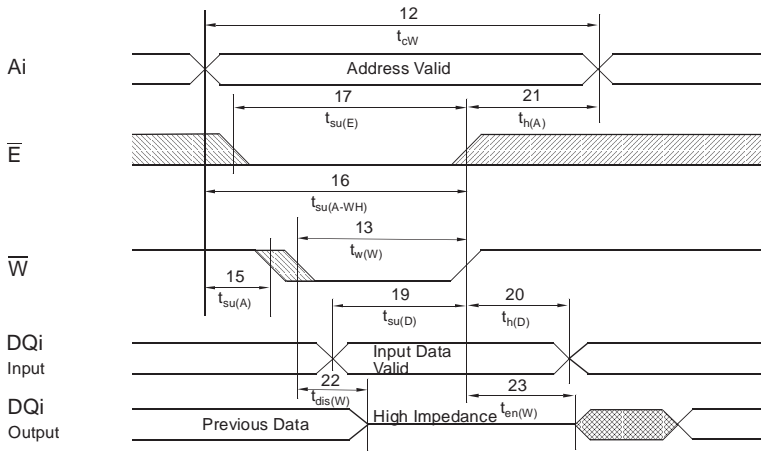


Read Cycle 2:  $\bar{G}$ -,  $\bar{E}$ -controlled (during Read cycle:  $\bar{W} = V_{IH}$ )<sup>g</sup>

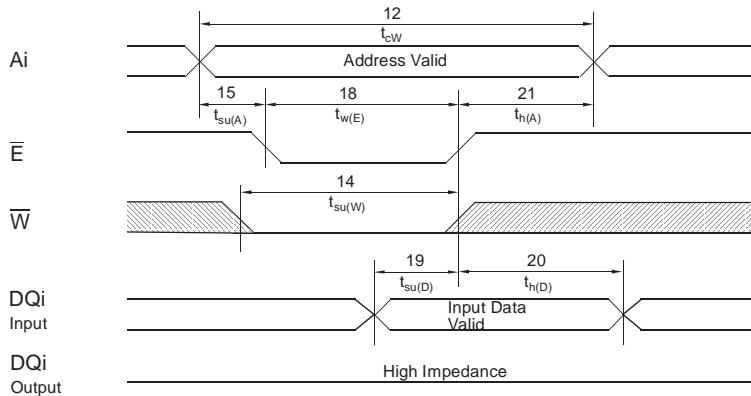


No.	Switching Characteristics Write Cycle	Symbol			25		45		Unit
		Alt. #1	Alt. #2	IEC	Min.	Max.	Min.	Max.	
12	Write Cycle Time	$t_{AVAV}$	$t_{AVAV}$	$t_{cW}$	25		45		ns
13	Write Pulse Width	$t_{WLWH}$		$t_{w(W)}$	20		35		ns
14	Write Pulse Width Setup Time		$t_{WLEH}$	$t_{su(W)}$	20		35		ns
15	Address Setup Time	$t_{AVWL}$	$t_{AVEL}$	$t_{su(A)}$	0		0		ns
16	Address Valid to End of Write	$t_{AVWH}$	$t_{AVEH}$	$t_{su(A-WH)}$	20		35		ns
17	Chip Enable Setup Time	$t_{ELWH}$		$t_{su(E)}$	20		35		ns
18	Chip Enable to End of Write		$t_{ELEH}$	$t_{w(E)}$	20		35		ns
19	Data Setup Time to End of Write	$t_{DVWH}$	$t_{DVEH}$	$t_{su(D)}$	12		20		ns
20	Data Hold Time after End of Write	$t_{WHDX}$	$t_{EHDX}$	$t_{h(D)}$	0		0		ns
21	Address Hold after End of Write	$t_{WHAX}$	$t_{EHAX}$	$t_{h(A)}$	0		0		ns
22	$\bar{W}$ LOW to Output in High-Z <sup>h,i</sup>	$t_{WLQZ}$		$t_{dis(W)}$		10		15	ns
23	$\bar{W}$ HIGH to Output in Low-Z	$t_{WHQX}$		$t_{en(w)}$	5		5		ns

Write Cycle #1:  $\overline{W}$ -controlled<sup>j</sup>



Write Cycle #2:  $\overline{E}$ -controlled<sup>j</sup>



undefined  L- to H-level  H- to L-level 

i: If  $\overline{W}$  is LOW and when  $\overline{E}$  goes LOW, the outputs remain in the high impedance state.

j:  $\overline{E}$  or  $\overline{W}$  must be  $V_{IH}$  during address transition.

## NONVOLATILE MEMORY OPERATIONS

### MODE SELECTION

$\bar{E}$	$\bar{W}$	A8 - A0 (hex)	Mode	I/O	Power	Notes
H	X	X	Not Selected	Output High Z	Standby	
L	H	X	Read SRAM	Output Data	Active	m
L	L	X	Write SRAM	Input Data	Active	

k: reserved for future development

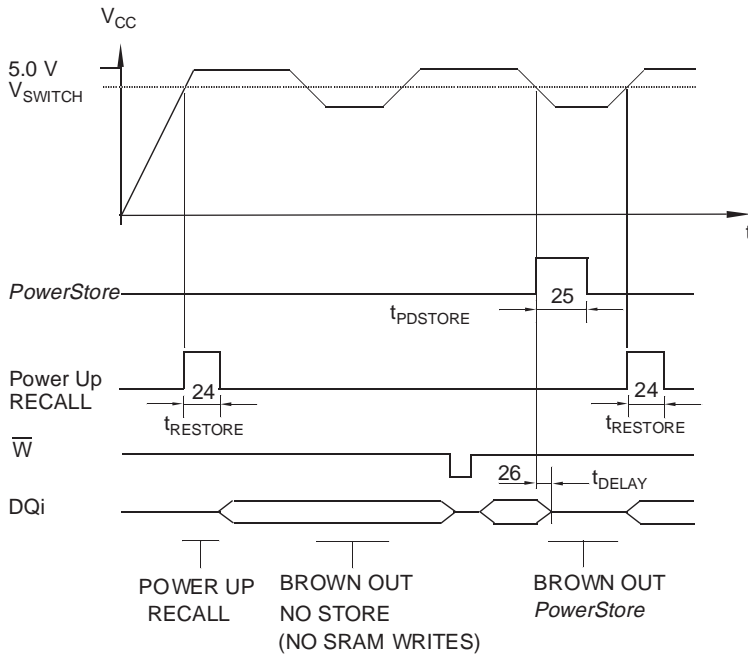
l: reserved for future development

m: I/O state assumes that  $\bar{G} \leq V_{IL}$ .

No.	PowerStore Power Up RECALL	Symbol		Conditions	Min.	Max.	Unit
		Alt.	IEC				
24	Power Up RECALL Duration <sup>n, e</sup>	$t_{RESTORE}$				650	$\mu s$
25	STORE Cycle Duration <sup>f</sup>	$t_{PDSTORE}$		the power supply voltage must stay above 3.6 V for at least 10 ms after the start of the STORE operation		10	ms
26	Time allowed to Complete SRAM Cycle <sup>f, e</sup>	$t_{DELAY}$			1		$\mu s$
	Low Voltage Trigger Level	$V_{SWITCH}$			4.0	4.5	V

n: An automatic RECALL also takes place at power up, starting when  $V_{CC}$  exceeds  $V_{SWITCH}$  and takes  $t_{RESTORE}$ .  $V_{CC}$  must not drop below  $V_{SWITCH}$  once it has been exceeded for the RECALL to function properly.

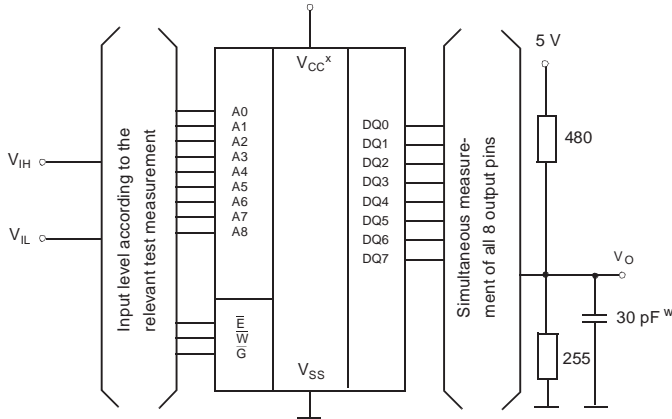
PowerStore and automatic Power Up RECALL



o ... t reserved for future development  
 u, v reserved for future development



Test Configuration for Functional Check



w: In measurement of  $t_{dis}$ -times and  $t_{en}$ -times the capacitance is 5 pF.

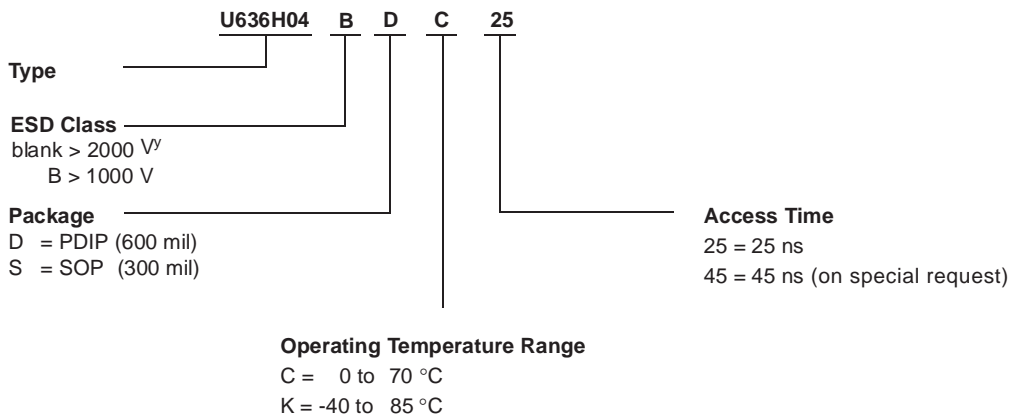
x: Between  $V_{CC}$  and  $V_{SS}$  must be connected a high frequency bypass capacitor 0.1  $\mu$ F to avoid disturbances.

Capacitance <sup>e</sup>	Conditions	Symbol	Min.	Max.	Unit
Input Capacitance	$V_{CC} = 5.0 V$ $V_I = V_{SS}$	$C_I$		8	pF
Output Capacitance	$f = 1 MHz$ $T_a = 25^\circ C$	$C_O$		7	pF

All Pins not under test must be connected with ground by capacitors.

IC Code Numbers

Example



The date of manufacture is given by the last 4 digits of the mark, the first 2 digits indicating the year, and the last 2 digits the calendar week.

y: ESD protection > 2000 V under development

## Device Operation

The U636H04 has two separate modes of operation: SRAM mode and nonvolatile mode. In SRAM mode, the memory operates as a standard fast static RAM. In nonvolatile mode, data is transferred from SRAM to EEPROM (the STORE operation) or from EEPROM to SRAM (the RECALL operation). In this mode SRAM functions are disabled.

STORE cycles may be initiated under user control via a software sequence and are also automatically initiated when the power supply voltage level of the chip falls below  $V_{SWITCH}$ . RECALL operations are automatically initiated upon power up and may occur also when  $V_{CC}$  rises above  $V_{SWITCH}$  after a low power condition.

### SRAM READ

The U636H04 performs a READ cycle whenever  $\bar{E}$  and  $\bar{G}$  are LOW and  $\bar{W}$  are HIGH. The address specified on pins A0 - A8 determines which of the 512 data bytes will be accessed. When the READ is initiated by an address transition, the outputs will be valid after a delay of  $t_{CR}$ . If the READ is initiated by  $\bar{E}$  or  $\bar{G}$ , the outputs will be valid at  $t_{a(E)}$  or at  $t_{a(G)}$ , whichever is later. The data outputs will repeatedly respond to address changes within the  $t_{CR}$  access time without the need for transition on any control input pins, and will remain valid until another address change or until  $\bar{E}$  or  $\bar{G}$  is brought HIGH or  $\bar{W}$  is brought LOW.

### SRAM WRITE

A WRITE cycle is performed whenever  $\bar{E}$  and  $\bar{W}$  are LOW. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either  $\bar{E}$  or  $\bar{W}$  goes HIGH at the end of the cycle. The data on pins DQ0 - 7 will be written into the memory if it is valid  $t_{su(D)}$  before the end of a  $\bar{W}$  controlled WRITE or  $t_{su(D)}$  before the end of an  $\bar{E}$  controlled WRITE. It is recommended that  $\bar{G}$  is kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O lines. If  $\bar{G}$  is left LOW, internal circuitry will turn off the output buffers  $t_{dis(W)}$  after  $\bar{W}$  goes LOW.

### AUTOMATIC STORE

The U636H04 uses the intrinsic system capacitance to

perform an automatic STORE on power down. As long as the system power supply take at least  $t_{PDSTORE}$  to decay from  $V_{SWITCH}$  down to 3.6 V the U636H04 will safely and automatically STORE the SRAM data in EEPROM on power down.

In order to prevent unneeded STORE operations, automatic STORE will be ignored unless at least one WRITE operation has taken place since the most recent STORE or RECALL cycle.

### AUTOMATIC RECALL

During power up an automatic RECALL takes place. After any low power condition ( $V_{CC} < V_{SWITCH}$ ) an internal RECALL request may be latched. When  $V_{CC}$  once again exceeds the sense voltage of  $V_{SWITCH}$ , a requested RECALL cycle will automatically be initiated and will take  $t_{RESTORE}$  to complete.

If the U636H04 is in a WRITE state at the end of a power up RECALL, the SRAM data will be corrupted. To help avoid this situation, a 10 K $\Omega$  resistor should be connected between  $\bar{W}$  and system  $V_{CC}$ .

### HARDWARE PROTECTION

The U636H04 offers hardware protection against inadvertent STORE operation through  $V_{CC}$  Sense. When  $V_{CC} < V_{SWITCH}$  all software controlled STORE operations will be inhibited.

### LOW AVERAGE ACTIVE POWER

The U636H04 has been designed to draw significantly less power when  $\bar{E}$  is LOW (chip enabled) but the access cycle time is longer than 55 ns.

When  $\bar{E}$  is HIGH the chip consumes only standby current.

The overall average current drawn by the part depends on the following items:

1. CMOS or TTL input levels
2. the time during which the chip is disabled ( $\bar{E}$  HIGH)
3. the cycle time for accesses ( $\bar{E}$  LOW)
4. the ratio of READs to WRITEs
5. the operating temperature
6. the  $V_{CC}$  level



## **Memory Products 1998**

### ***PowerStore 512 x 8 nvSRAM U636H04***

#### **LIFE SUPPORT POLICY**

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The information describes the type of component and shall not be considered as assured characteristics.

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