ZiLOG

PRODUCT SPECIFICATION

Z86C30

CMOS Z8® 8-BIT MICROCONTROLLER

FEATURES

- 8-bit CMOS microcontroller, 28-pin DIP
- Low cost
- 3.0 to 5.5 volt operating range
- Low power consumption - 50 mW (Typical)
- Fast instruction pointer - 1.0 microsecond @ 12 MHz
- Two standby modes (STOP and HALT)
- 24 input/output lines (two with comparator inputs)
- All digital inputs CMOS levels, Schmitt-triggered
- 4 Kbytes of ROM
- 236 bytes of RAM
- Two Expanded Register File control registers
- Two programmable 8-bit Counter/Timers
- 6-bit programmable prescaler on each Counter/Timer
- Six vectored, priority interrupts from six different sources
- Clock speeds 8 and 12 MHz
- "Brown-Out" protection
- Watchdog/Power-On Reset Timer
- Two comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC or external clock drive.
- ROM and RAM protect

GENERAL DESCRIPTION

The Z86C30 CCP™ Consumer Controller Processor introduces a new level of sophistication to single-chip architecture. The Z86C30 is a member of the Z8 single-chip microcontroller family with 4 Kbytes of ROM and 236 bytes of RAM. The device is housed in a 28-pin DIP, and is manufactured in CMOS technology. Zilog's CMOS microcontroller offers fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C30 architecture is characterized by Zilog's 8-bit microcontroller core with an Expanded Register File to allow easy access to register mapped peripheral and I/O circuits. The CCP offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many industrial, automotive, and advanced scientific applications.

The device applications demand powerful I/O capabilities. The CCP fulfills this with 24 pins dedicated to input and output. These lines are grouped into three ports, eight lines per port, and are configurable under software control to provide timing, status signals, and parallel I/O with or without handshake.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Register File, and Expanded Register File. The Register File is composed of 236 bytes of general purpose registers, three I/O port registers and 15 control and status registers. The Expanded Register File consists of two Control registers.

GENERAL DESCRIPTION (Continued)

To unburden the program from coping with the real-time problems such as counting/timing and input/output data communication, the Z86C30 offers two on-chip counter/timers with a large number of user selectable modes, and on-board comparators to process analog signals with a common reference voltage (Figure 1).

Note: All Signals with a preceding front slash, "/", are active Low, e.g.: B//W (WORD is active Low); /B/W (BYTE is active Low, only); /N//S (NORMAL and SYSTEM are both active Low).

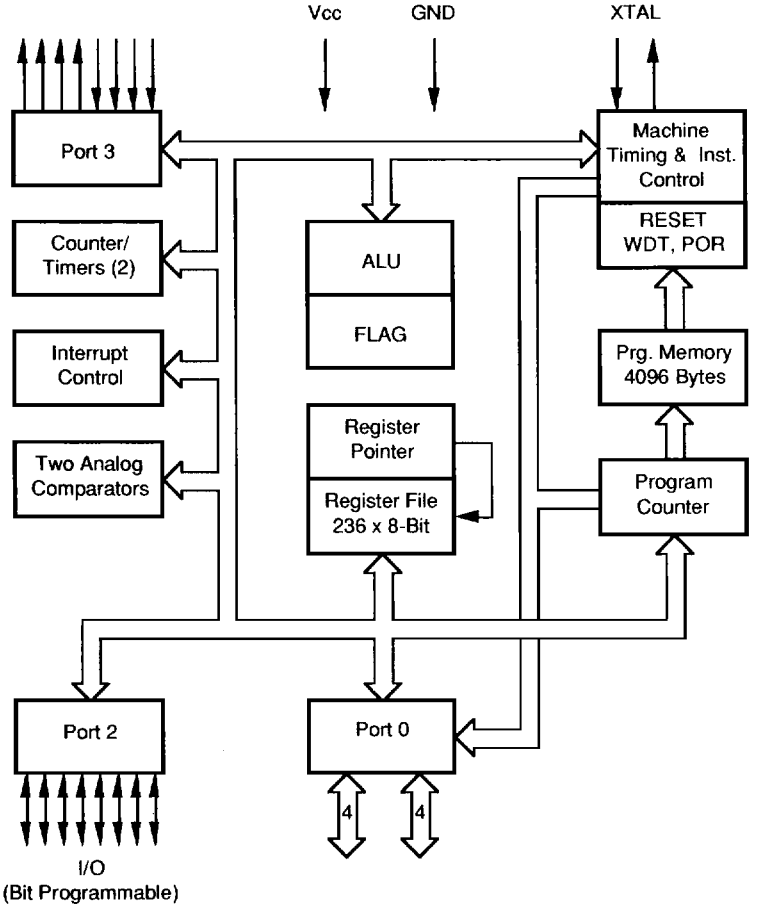


Figure 1. Functional Block Diagram

PIN DESCRIPTION

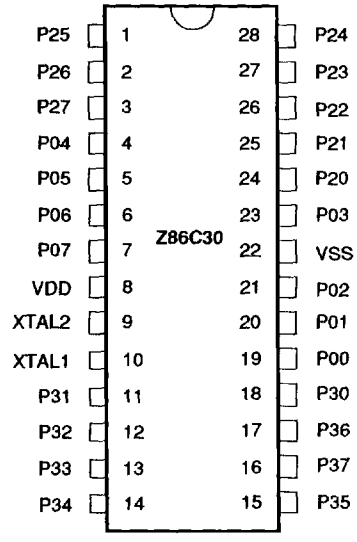


Figure 2. Pin Configuration

Table 1. Pin Identification

Pin #	Symbol	Function	Direction
1-3	P25-7	Port 2 pin 5,6,7	In/Output
4-7	P04-7	Port 0 pin 4,5,6,7	In/Output
8	V_{CC}	Power Supply	Input
9	XTAL2	Crystal Oscillator	Output
10	XTAL1	Crystal Oscillator	Input
11-13	P31-3	Port 3 pin 1,2,3	Fixed Input
14-15	P34-5	Port 3 pin 4,5	Fixed Output
16	P37	Port 3 pin 7	Fixed Output
17	P36	Port 3 pin 6	Fixed Output
18	P30	Port 3 pin 0	Fixed Input
19-21	P00-2	Port 0 pin 0,1,2	In/Output
22	GND	Ground, V_{SS}	Input
23	P03	Port 0 pin 3	In/Output
24-28	P20-4	Port 2 pin 0,1,2,3,4	In/Output

Note: Power connections follow Conventional descriptions below

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

XTAL1. *Crystal 1* (time-based input). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network or external single-phase clock to the on-chip oscillator input.

XTAL2. *Crystal 2* (time-based output). This pin connects a parallel-resonant crystal, ceramic resonator, LC or RC network to the on-chip oscillator output.

Port 0 P00-P07. Port 0 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be nibble programmed as P00-P03 input/output and P04-P07 input/output, separately. All input buffers are Schmitt-triggered and output drivers are push-pull. It can also be used as a handshake I/O port.

Port 3 lines P32 and P35 are used as handshake control lines. The handshake direction is determined by the configuration (input or output) assigned to port 0's upper nibble. The lower nibble must have the same direction as the upper nibble (Figure 3).

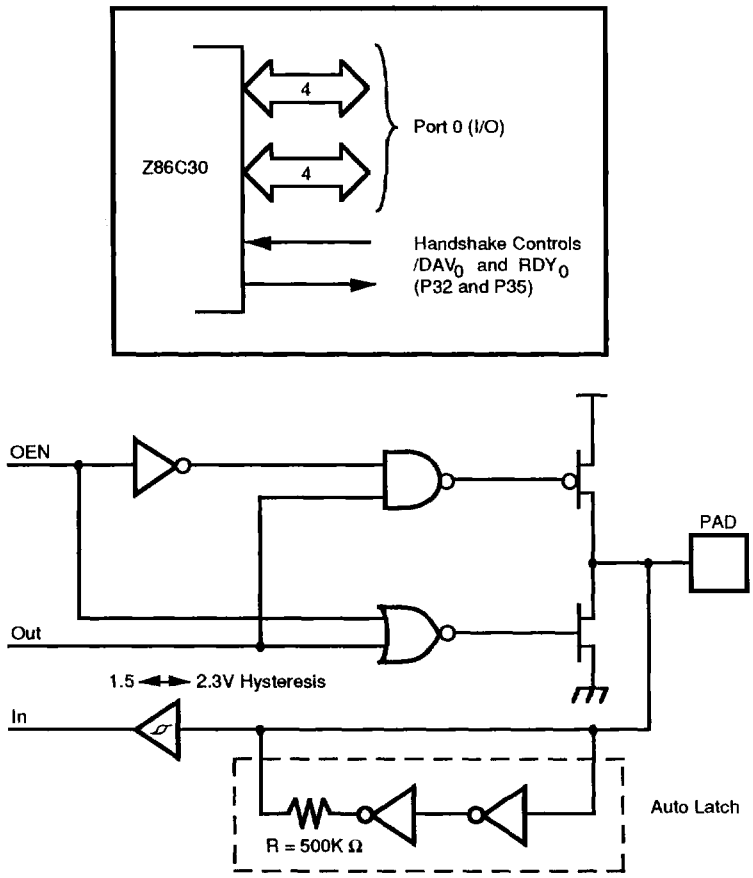


Figure 3. Port 0 Configuration

Port 2 P20-P27. Port 2 is an 8-bit, bidirectional, CMOS compatible I/O port. These eight I/O lines can be configured under software control as an input or output, independently. Input buffers are Schmitt-triggered. Bits programmed as outputs may be globally programmed as either push-pull or open drain. When used as an I/O port, Port 2 may be placed under handshake control. In this configuration, Port 3 lines P31 and P36 are used as the handshake control lines. The handshake signal assignment for Port 3 lines P31 and P36 is dictated by the direction (input or output) assigned to bit 7, Port 2 (Figure 4).

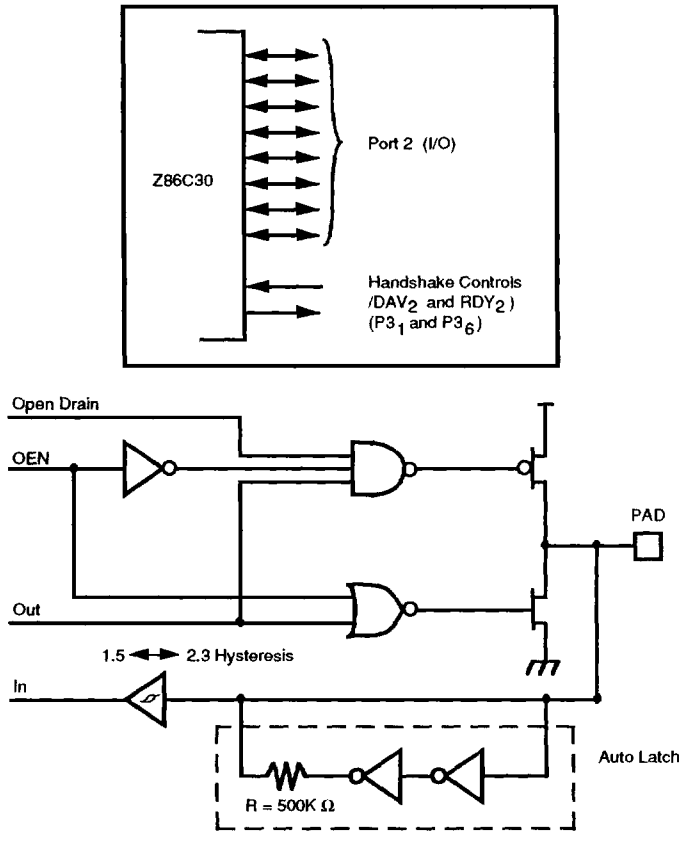


Figure 4. Port 2 Configuration

PIN DESCRIPTION (Continued)

Auto-Latch. The Auto-Latch puts valid CMOS levels on all CMOS inputs that are not externally driven. This reduces excessive supply current flow in the input buffer when not being driven by any source (Figure 46).

Port 3 P30-P37. Port 3 is an 8-bit, CMOS compatible port with four fixed input and four fixed output. Port 3 consists of four fixed inputs (P30-P33) and four fixed outputs (P34-P37), and can be configured under software for interrupt and port handshake functions. Port 3, pin 0 input is Schmitt-triggered. Pins P31, P32 and P33 are standard CMOS inputs and the outputs are push-pull. Two on-board comparators can process analog signals on P31 and P32 with reference to the voltage on P33. The analog function is enabled by programming the Port 3 Mode Register (bit 1). P30 and P33 are falling edge interrupt inputs. P31 and P32 are programmable as falling, rising, or both edge triggered interrupts (IRQ register bits 6 and 7). P33 is the comparator reference voltage input.

Access to Counter/Timer 1 is made through P31 (T_{IN} and P36 (T_{OUT}). Handshake lines for Ports 0 and 2 are available on P3 pin 1 through 6 (Figure 5).

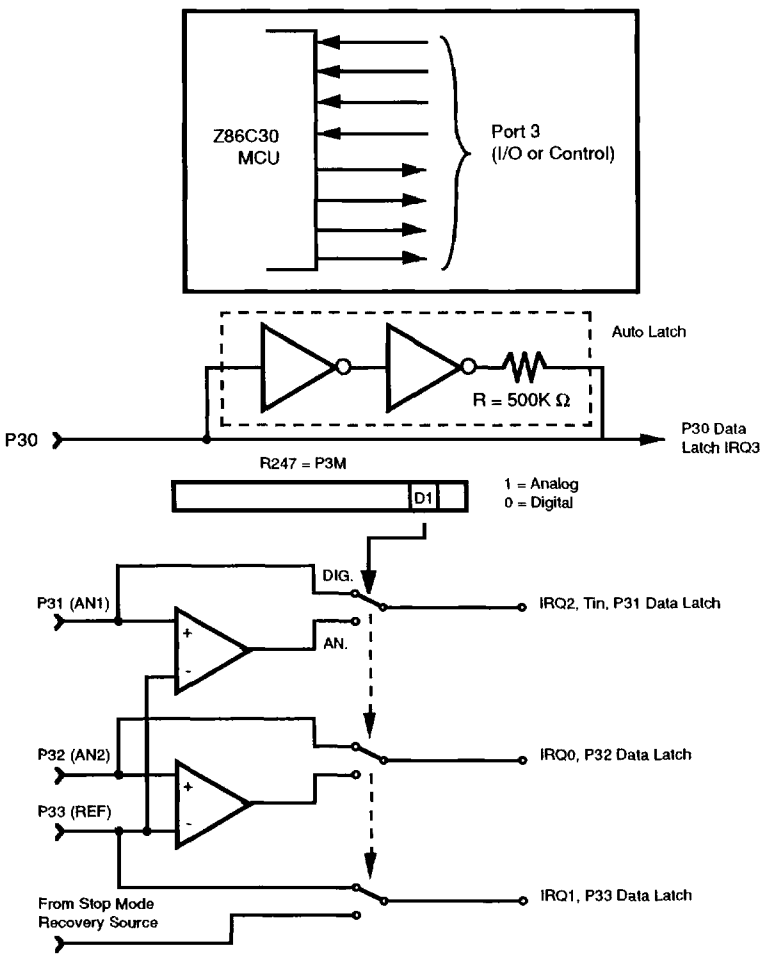


Figure 5. Port 3 Configuration

Table 2. Pin Assignments

Pin	I/O	CTC1	AN In	Int.	P0 HS	P2 HS
P30	IN			IRQ3		
P31	IN	Tin	AN1	IRQ2		D/R
P32	IN		AN2	IRQ0	D/R	
P33	IN		REF	IRQ1		
P34	OUT					
P35	OUT				R/D	
P36	OUT	Tout				R/D
P37	OUT					

Notes:
HS = Handshake Signals
D = DAV
R = RDY

Comparator Inputs. Port 3 Pin P31 and P32 each have a comparator front end. The comparator reference voltage Pin P33 is common to both comparators. In analog mode, the P31 and P32 are the positive inputs to the comparators and P33 is the reference voltage supplied to both comparators. In digital mode, pin P33 can be used as a P33 register input or IRQ1 source.

FUNCTIONAL DESCRIPTION

The Z8 CCP incorporates special functions to enhance the Z8's application in industrial, scientific research and advanced technologies applications.

Reset. The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- STOP Mode Recovery Source
- Brown-Out Recovery

The Z86C30 does not re-initialize WDTMR, SMR, P2M, and P3M registers to their reset values on a STOP Mode Recovery operation.

Program Memory. The Z86C30 can address up to 4K bytes of internal program memory (Figure 6). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain six, 16-bit vectors that correspond to the six available interrupts. Byte 13 to byte 4095 consists of on-chip mask programmed ROM.

The 4K bytes of program memory is mask programmable. **A ROM protect feature prevents "dumping" of the ROM contents by inhibiting execution of LDC and LDCI instructions to program memory in ALL modes.**

The ROM protect option is mask-programmable, and is selected by the customer when the ROM code is submitted.

Expanded Register File. The register file has been expanded to allow for additional system control registers, mapping of additional peripheral devices and input/output ports into the register address area. The Z8 register address space R0 through R15 is implemented as 16 groups of 16 registers per group (Figure 7). These register groups are known as the ERF (Expanded Register File).

Bits 3:0 of the Register Pointer (RP) select the active ERF group. Bits 7:4 of register RP select the working register group (Figure 8). Two system configuration registers reside in the Expanded Register File at bank F. The rest of the Expanded Register is not physically implemented and is open for future expansion.

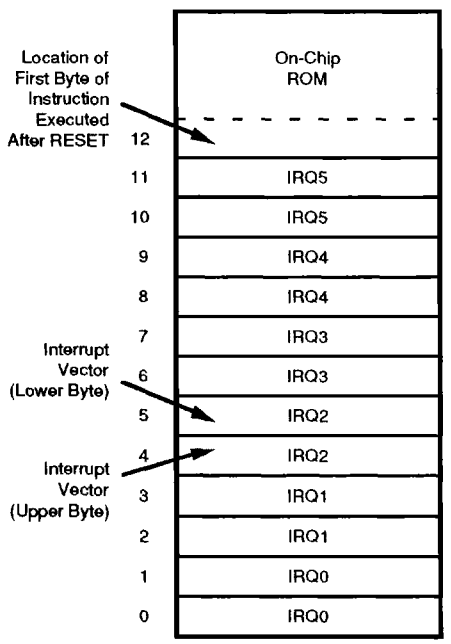


Figure 6. Program Memory Map

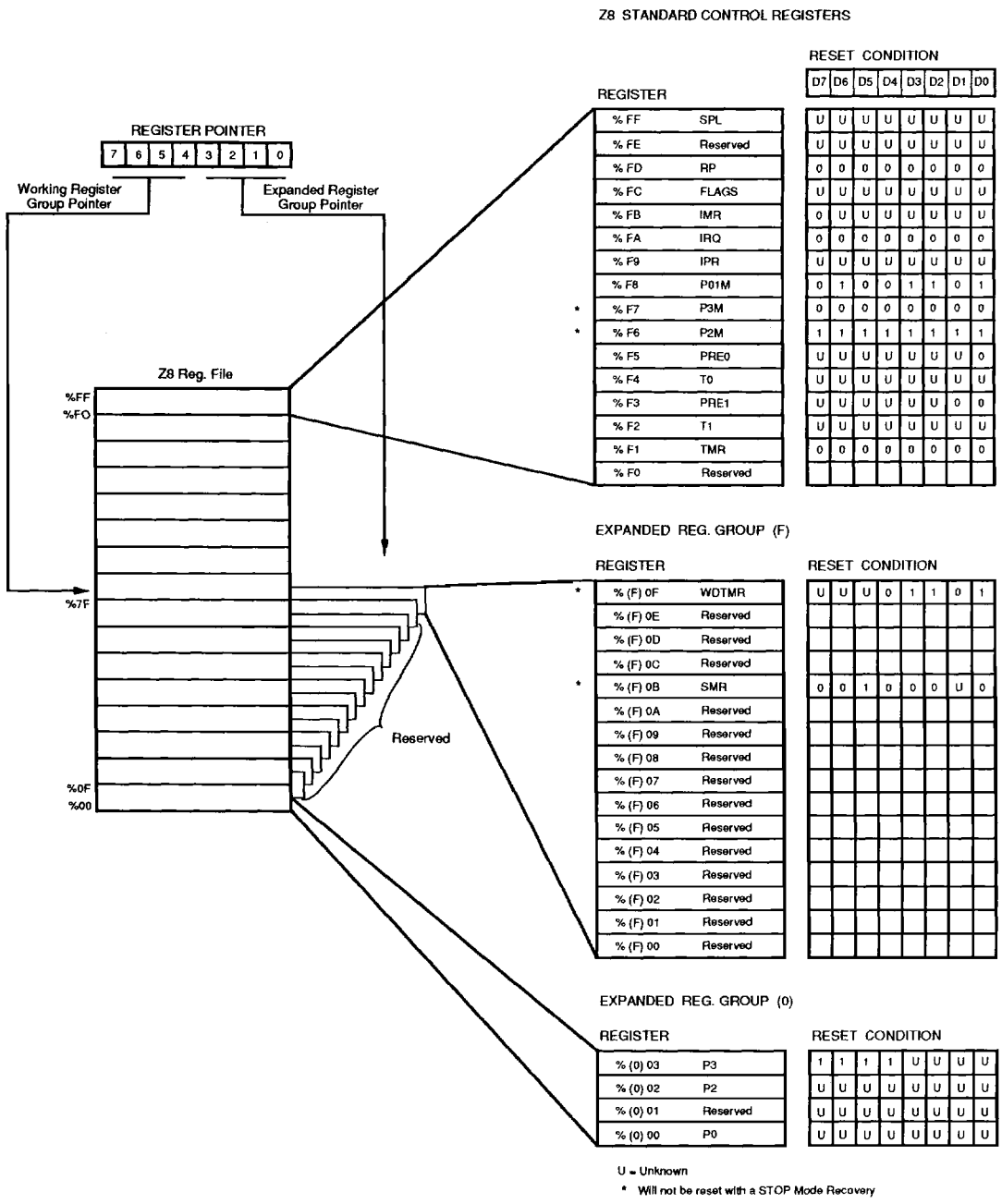


Figure 7. Expanded Register File Architecture

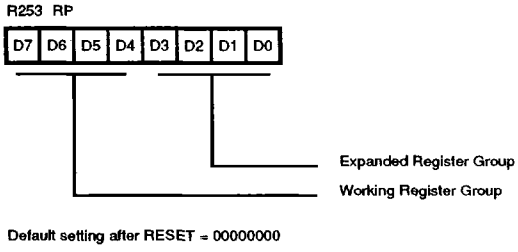


Figure 8. Register Pointer Register

Register File. The register file consists of three I/O port registers, 236 general purpose registers and 15 control and status registers (R0-R3, R4-239 and R240-R255, respectively), and two system configuration registers in the expanded register group (See Figure 7). The instructions can access registers directly or indirectly via an 8-bit address field. This allows a short 4-bit register address using the Register Pointer (Figure 9). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The Register Pointer addresses the starting location of the active working register group.

Note: Register Bank E0-FF can only be accessed through working register and indirect addressing modes.

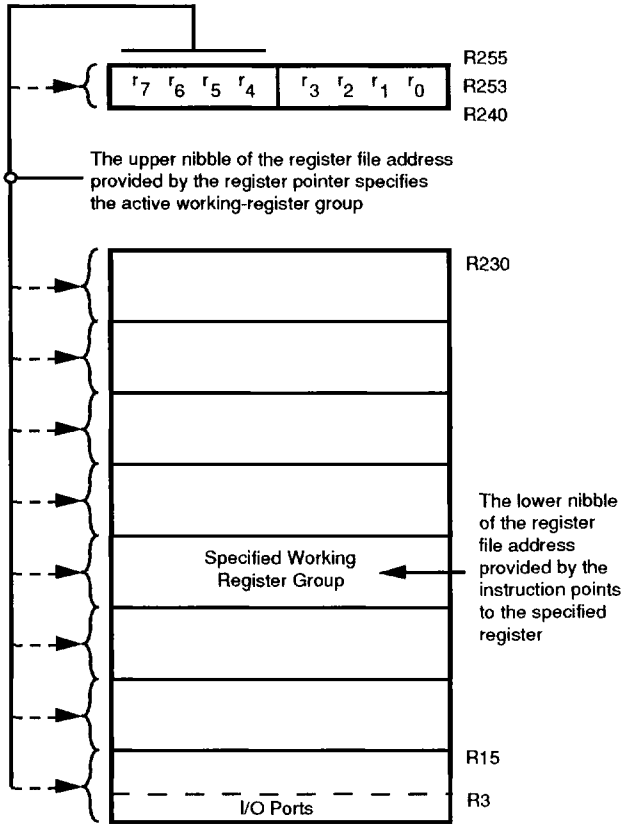


Figure 9. Register Pointer

RAM Protect. The upper portion of the RAM's address spaces %7F to %EF (excluding the control registers) can be protected from reading and writing. The RAM Protect bit option is mask-programmable and is selected by the customer when the ROM code is submitted. After the mask option is selected, the user can activate from the internal ROM code to turn off/on the RAM Protect by loading a bit D6 in the IMR register to either a 0 or a 1, respectively. A 1 in D6 indicates RAM Protect enabled.

Stack. An 8-bit Stack Pointer (R255) is used for the internal stack that resides within the 256 general purpose registers.

Counter/Timers. There are two 8-bit programmable counter/timers (T0-T1), each driven by its own 6-bit programmable prescaler. The T1 prescaler can be driven by internal or external clock sources; however, the T0 prescaler is driven by the internal clock only (Figure 10).

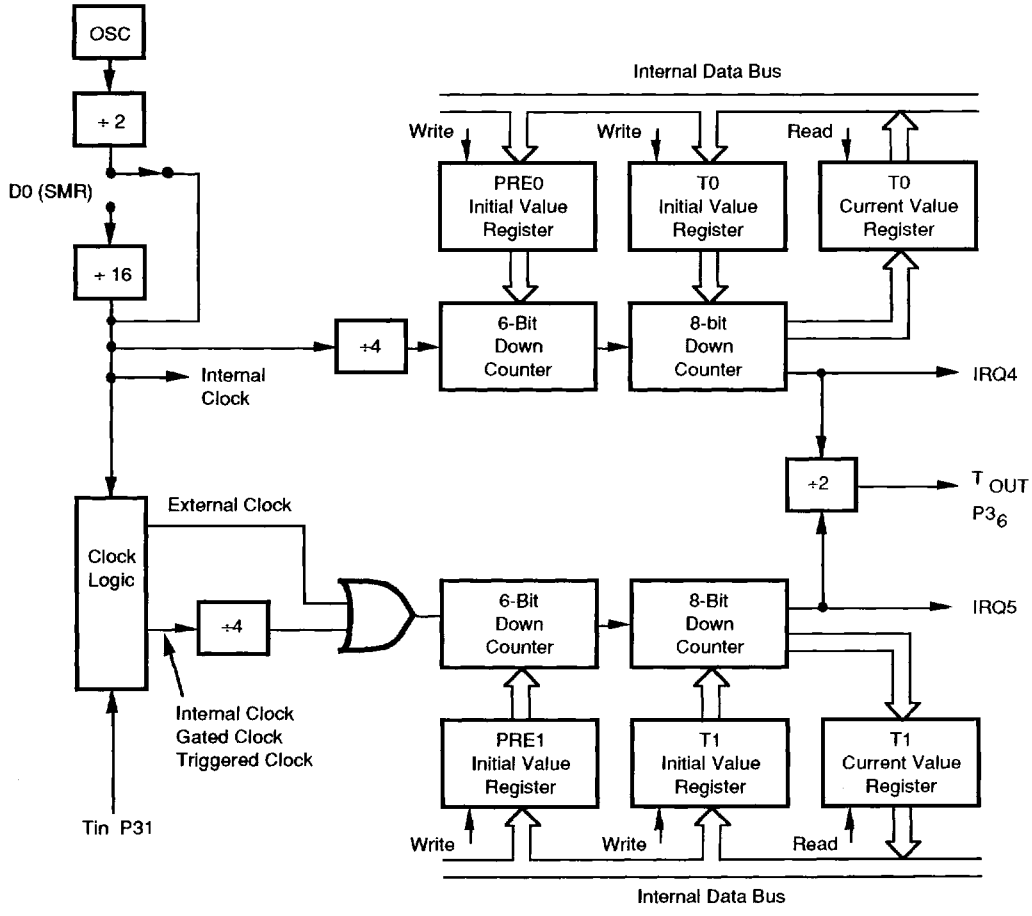


Figure 10. Counter/Timer Block Diagram

The 6-bit prescalers can divide the input frequency of the clock source by any integer number from 1 to 64. Each prescaler drives its counter, which decrements the value (1 to 256) that has been loaded into the counter. When the counter reaches the end of count, a timer interrupt request-IRQ4 (T0) or IRQ5 (T1) is generated.

The counters can be programmed to start, stop, restart to continue, or restart from the initial value. The counters can also be programmed to stop upon reaching zero (single pass mode) or to automatically reload the initial value and continue counting (modulo-n continuous mode).

The counters, but not the prescalers, can be read at any time without disturbing their value or count mode. The clock source for T1 is user-definable and can be either the internal microprocessor clock divided-by-four, or an external signal input via Port 3. The Timer Mode register configures the external timer input (P31) as an external clock; a trigger input that can be retriggerable or not-retriggerable; or as a gate input for the internal clock. Port 3 line P36 serves as a timer output (Tout) through which T0, T1 or the internal clock are output. The counter/timers can be cascaded by connecting the T0 output to the input of T1.

Interrupts. The Z86C30 has six different interrupts from six different sources. The interrupts are maskable and prioritized (Figure 11). The six sources are divided as follows; four sources are claimed by Port 3 lines P30-P33 and two in counter/timers. The Interrupt Mask Register globally or individually enables or disables the six interrupt requests (Table 3).

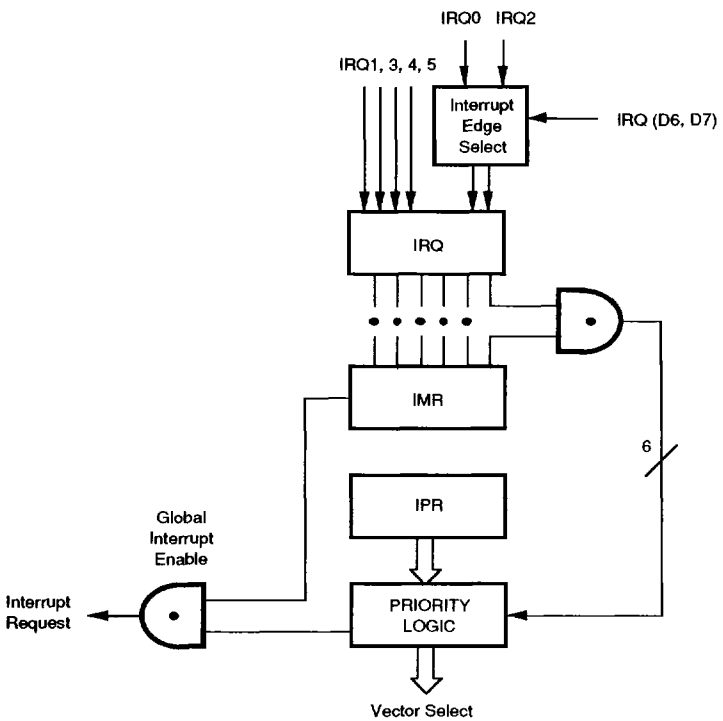


Figure 11. Interrupt Block Diagram

Table 3. Interrupt Types, Sources, and Vectors

Name	Source	Vector Location	Comments
IRQ 0	/DAV 0, IRQ 0	0, 1	External (P32), Rising/Falling Edge Triggered
IRQ 1,	IRQ 1	2, 3	External (P33), Falling Edge Triggered
IRQ 2	/DAV 2, IRQ 2, TIN	4, 5	External (P31), Rising/Falling Edge Triggered
IRQ 3	IRQ3	6, 7	External (P30), Falling Edge Triggered
IRQ 4	T0	8, 9	Internal
IRQ 5	T1	10, 11	Internal

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder that is controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. Thus, disabling all subsequent interrupts saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86C30 interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit starting address of the interrupt service routine for that particular interrupt request.

To accommodate polled interrupt systems, interrupt inputs are masked and the interrupt request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 may be rising, falling or both edge triggered, and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is shown in Table 4.

Table 4. IRQ Register

IRQ		Interrupt Edge	
D7	D6	P31	P32
0	0	F	F
0	1	F	R
1	0	R	F
1	1	R/F	R/F

Notes:
F = Falling Edge
R = Rising Edge

Clock. The Z86C30 on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, RC, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal should be AT cut, 10 KHz to 12 MHz max., with a series resistance (RS) less than, or equal to, 100 Ohms.

The crystal should be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance is more than or equal to 22pf) from each pin to ground. The RC oscillator option is mask-programmable, to be selected by the customer at the time ROM code is submitted. The RC oscillator configuration must be an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (Figure 12). The RC value vs. Frequency curves are shown in Figures 46 to 48. **(Note: The RC option is not available in the 12 MHz part.)**

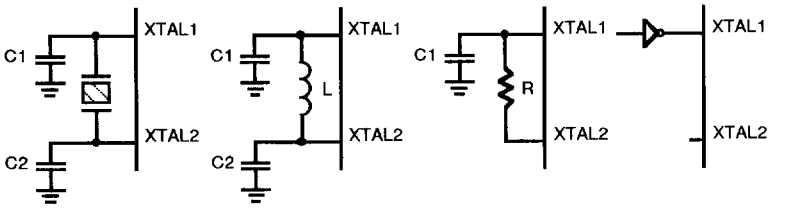
Power-On Reset (POR). A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR timer allows V_{cc} and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

1. Power-fail to Power-OK status
2. STOP mode recovery (if D5 of SMR=1)
3. WDT timeout

The POR time is a nominal 5 mS. Bit 5 of the Stop Mode register determines whether the POR timer is bypassed after STOP mode recovery (typical for external clock, and RC/LC oscillators with fast start up time).

HALT. Turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupt IRQ0, IRQ1, and IRQ2, remain active. The device may be recovered by interrupts, either external or internal generated.



Ceramic Resonator or Crystal	LC	RC	External Clock
C1, C2 = 47 pf TYP *	C1, C2 = 22 pf	@ 5V VCC (TYP)	
F = 8 MHz	L = 130 uH *	C1 = 33 pf *	
	F = 3 MHz *	R = 1K *	
		F = 9.5 MHz *	

* Preliminary Value Including Pin Parasitics

Figure 12. Oscillator Configuration

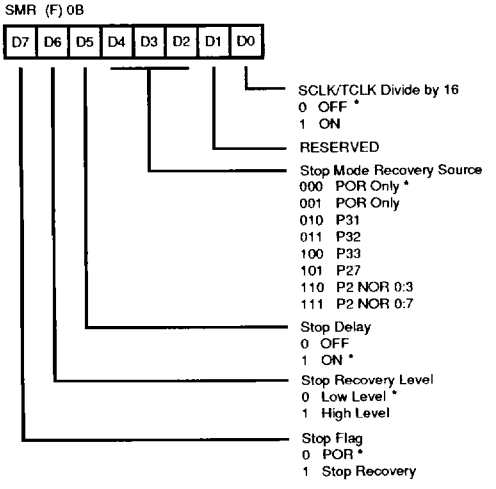
STOP. This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10 microamps or less. The Stop mode is terminated by a RESET only, either by WDT timeout, POR, or SMR recovery. This causes the processor to restart the application program at address 000C (HEX). In order to enter STOP (or HALT) mode, it is necessary to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, the user must execute a NOP (opcode=FFH) immediately before the appropriate sleep instruction, i.e.:

```
FF    NOP     ; clear the pipeline
6F    STOP    ; enter STOP mode
        or
FF    NOP     ; clear the pipeline
7F    HALT    ; enter HALT mode
```

Stop Mode Recovery Register (SMR). This register selects the clock divide value and determines the mode of STOP mode recovery (Figure 13). All bits are Write only, except Bit 7 which is a Read only. Bit 7 is a flag bit that is hardware set on the condition of STOP Recovery and reset by a power-on cycle. Bit 6 controls whether a low level or high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits 2, 3, and 4 of the SMR register specify the source of the STOP Mode Recovery signal. Bits 0 and 1 determine the timeout period of the WDT (Table 6). The SMR is located in bank F of the Expanded Register Group at address OBH.

SCLK/TCLK Divide-by-16 Select (D0). D0 of the SMR controls a divide-by-16 prescaler of SCLK/TCLK. The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT mode (TCLK sources, counter/timers, and interrupt logic).

STOP Mode Recovery Source (D2, D3, and D4). These three bits of the SMR specify the wake up source of the STOP Mode recovery (Figure 14).



* Default setting after RESET

Figure 13. STOP Mode Recovery Register

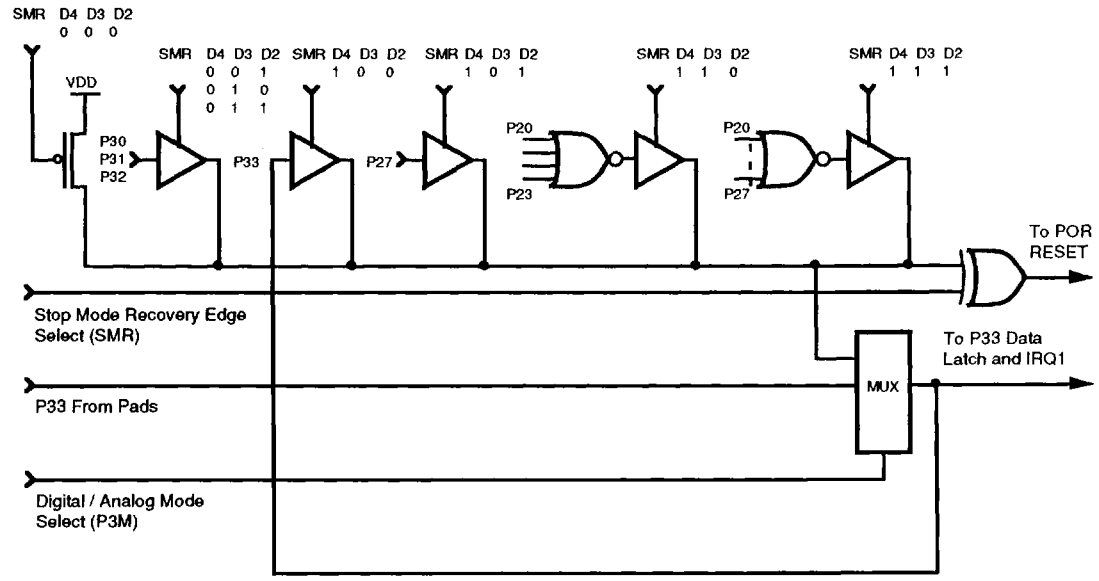


Figure 14. STOP Mode Recovery Source

Table 5. Stop Mode Recovery Source

SMR D4	SMR D3	SMR D2	Operation Description of action
0	0	0	POR recovery only
0	0	1	P30 transition
0	1	0	P31 transition
0	1	1	P32 transition
1	0	0	P33 transition
1	0	1	P27 transition
1	1	0	Logical NOR of Port 2 bits 0:3
1	1	1	Logical NOR of Port 2 bits 0:7

STOP Mode Recovery Delay Select (D5). This bit disables the 5 mS RESET delay after STOP Mode Recovery. The default condition of this bit is 1. If the "fast" wake up is selected, the STOP Mode Recovery source needs to be kept active for at least 5 TpC.

STOP Mode Recovery Level Select (D6). A 1 in this bit position indicates that a high level on any one of the recovery sources wakes the Z86C30 from STOP Mode. A 0 indicates low level recovery. The default is 0 on POR (Figure 14).

Cold or Warm Start (D7). This bit is set by the device upon entering STOP Mode. A 0 in this bit (cold) indicates that the device will be reset by POR RESET. A 1 in this bit (warm) indicates that the device awakens by a SMR source.

Watch Dog Timer Mode Register (WDTMR). The WDT is a retriggerable one-shot timer that will reset the Z8 if it reaches its terminal count. The WDT is initially enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT cannot be disabled after it has been initially enabled. The WDT circuit is driven by an on-board RC oscillator or external oscillator from XTAL1 pin. The POR clock source is selected with bit 4 of the WDT register.

WDT Time Select (D0, D1). Bits 0 and 1 control a tap circuit that determines the timeout period. Table 6 shows the different values that can be obtained. The default value of D0 and D1 are 1 and 0, respectively.

FUNCTIONAL DESCRIPTION (Continued)

Table 6. Timeout Period of the WDT

D1	D0	Timeout of Internal RC OSC	Timeout of XTAL clock
0	0	5 ms min	256 TpC
0	1	15 ms min	512 TpC
1	0	25 ms min	1024 TpC
1	1	100 ms min	4096 TpC

Notes:
TpC = XTAL clock cycle
The default on reset is 15 ms.
See Figures 50 to 53 for details.

WDT During HALT (D2). This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

WDT During STOP (D3). This bit determines whether or not the WDT is active during STOP mode. A 1 indicates active during STOP. A 0 will disable the WDT during STOP mode. Since the on-board OSC is stopped during STOP mode, the WDT clock source has to select the on-board RC OSC for the WDT to recover from STOP mode. The default is 1.

Clock source for WDT (D4). This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator.

Bits 5 through 7 are reserved. The WDTMR register is accessible only during the first 64 processor cycles (128 XTAL clock cycles) from the execution of the first instruction after Power-On Reset, watch dog reset or a STOP mode recovery. After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in bank F of the Expanded Register Group at address location 0FH (Figure 15).

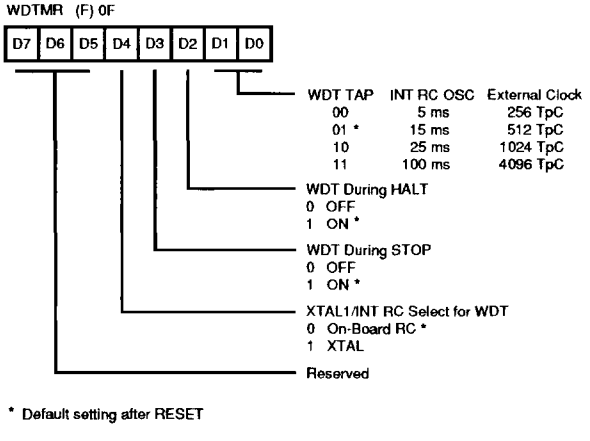


Figure 15. Watchdog Timer Mode Register

Brown Out Protection. An on-board Voltage Comparator checks that V_{CC} is at the required level to ensure correct operation of the device. Reset is globally driven if V_{CC} is below the referenced voltage (Brown Out Voltage). The minimum operating voltage varies with temperature and operating frequency, while the brown out voltage (V_{BO}) varies with temperature only.

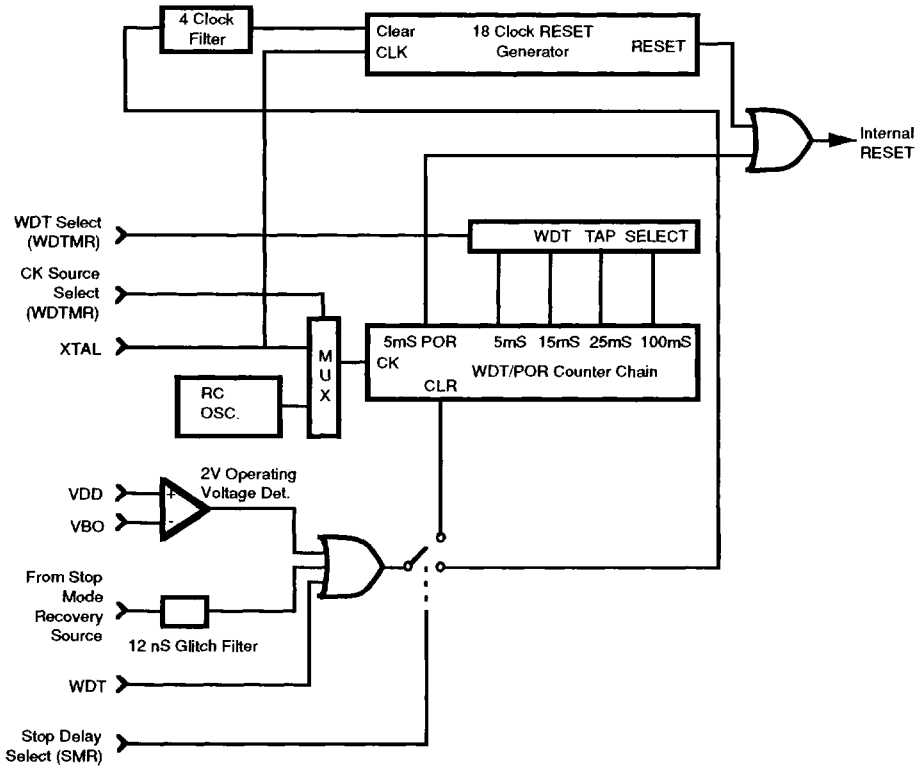


Figure 16. Resets and WDT

The brown-out trip voltage (V_{BO}) is less than 3 volts and above 1.4 volts under the following conditions.

Maximum (V_{BO}) Conditions:

Case1 T_A = -40°C to +105°C, Internal Clock Frequency equal or less than 1 MHz

Case 2 T_A = -40°C to + 85°C, Internal Clock Frequency equal or less than 2 MHz

Note: The internal clock frequency runs at half the external clock frequency.

The device functions normally at or above 3.0V under all conditions. Below 3.0V, the device is guaranteed to function normally until the Brown-Out Protection trip point (V_{BO}) is reached for the temperatures and operating frequencies in case 1 and case 2 above. The actual brown-out trip point is a function of temperature and process parameters (Figure 17).

ROM Protect. ROM protect is mask-programmable. It is selected by the customer at the time the ROM code is submitted. **The selection of ROM protect will disable the LDC and LDCI instructions in ALL modes.**

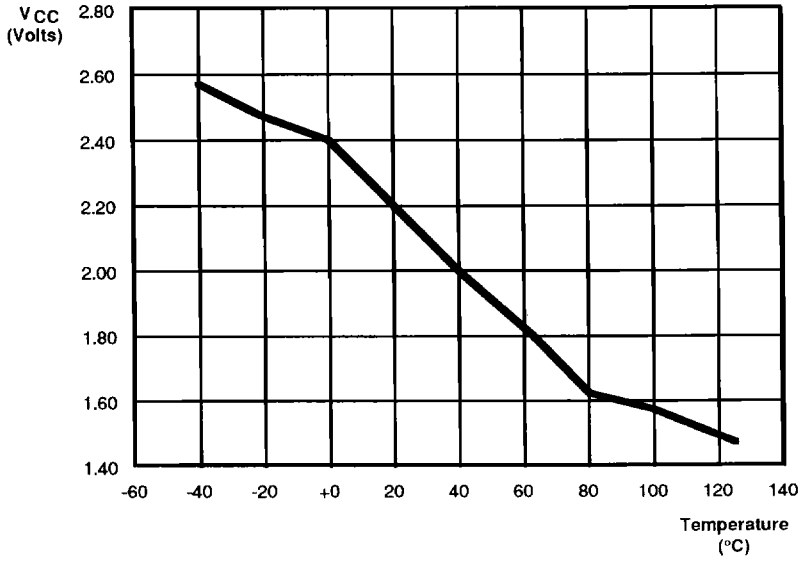


Figure 17. Typical Z86C30 V_{BO} Voltage vs Temperature

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions, as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Figure 18).

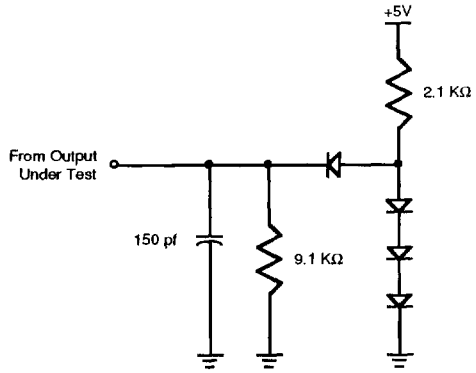


Figure 18. Test Load Configuration

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
Vcc	Supply Voltage (*)	-0.3	+7.0	V
TSTG	Storage Temp	-65	+150	C
T_A	Oper Ambient Temp		†	C
	Power Dissipation		2.2	W

Notes:
* Voltage on all pins with respect to GND.
† See Ordering Information.

Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended period may affect device reliability.

CAPACITANCE

T_A = 25°C, V_{CC} = GND = 0V, f = 1.0 MHz, Unmeasured pins to GND.

Parameter	Max
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

DC ELECTRICAL CHARACTERISTICS
Z86C30

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40°C to 105°C Min	Max	Typical at 25°C	Units	Conditions	Notes
	Max Input Voltage	3.3V		7		7		V	I_{IN} 250µA	
		5.0V		7		7		V	I_{IN} 250µA	
V_{CH}	Clock Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V	Driven by External Clock Generator	
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V	Driven by External Clock Generator	
V_{CL}	Clock Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	0.7	V	Driven by External Clock Generator	
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.5	V	Driven by External Clock Generator	
V_{IH}	Input High Voltage	3.3V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	1.3	V		
		5.0V	0.7 V_{CC}	V_{CC}+0.3	0.7 V_{CC}	V_{CC}+0.3	2.5	V		
V_{IL}	Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	0.7	V		
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.5	V		
V_{OH}	Output High Voltage	3.3V	V_{CC}-0.4		V_{CC}-0.4		3.1	V	I_{OL} = -2.0 mA	
		5.0V	V_{CC}-0.4		V_{CC}-0.4		4.8	V	I_{OL} = -2.0 mA	
$V_{OL}1$	Output Low Voltage	3.3V		0.6		0.6	0.2	V	I_{OL} = +4.0 mA	
		5.0V		0.4		0.4	0.1	V	I_{OL} = +4.0 mA	
$V_{OL}2$	Output Low Voltage	3.3V		1.2		1.2	0.3	V	I_{OL} = +6 mA, 3 Pin Max	
		5.0V		1.2		1.2	0.3	V	I_{OL} = +12 mA, 3 Pin Max	
V_{RH}	Reset Input High Voltage	3.3V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	1.5	V		
		5.0V	.8 V_{CC}	V_{CC}	.8 V_{CC}	V_{CC}	2.1	V		
V_{RI}	Reset Input Low Voltage	3.3V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.1			
		5.0V	V_{SS}-0.3	0.2 V_{CC}	V_{SS}-0.3	0.2 V_{CC}	1.7			
V_{OFFSET}	Comparator Input Offset Voltage	3.3V		25		25	10	mV		
		5.0V		25		25	10	mV		
I_{IL}	Input Leakage	3.3V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{OL}	Output Leakage	3.3V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
		5.0V	-1	1	-1	2	<1	µA	V_{IN} = 0V, V_{CC}	
I_{IR}	Reset Input Current	3.3V		-45		-60	-20	µA		
		5.0V		-55		-70	-30	µA		
I_{CC}	Supply Current	3.3V		10		10	4	mA	@ 8 MHz	[4,5]
		5.0V		15		15	10	mA	@ 8 MHz	[4,5]
		3.3V		15		15	5	mA	@ 12 MHz	[4,5]
		5.0V		20		20	15	mA	@ 12 MHz	[4,5]

DC ELECTRICAL CHARACTERISTICS (Continued)
Z86C30

Symbol	Parameter	V_{CC} Note [3]	T_A = 0°C to 70°C Min	Max	T_A = -40°C to 105°C Min	Max	Typical at 25°C	Units	Conditions	Notes
$I_{CC}1$	Standby Current	3.3V		3		3	1	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		5.0V		5		5	2.4	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 8 MHz	[4,5]
		3.3V		4		4	1.5	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		5.0V		6		6	3.2	mA	HALT Mode V_{IN} = 0V, V_{CC} @ 12 MHz	[4,5]
		3.3V		2		2	0.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		5.0V		4		4	1.8	mA	Clock Divide by 16 @ 8 MHz	[4,5]
		3.3V		3		3	1.2	mA	Clock Divide by 16 @ 12 MHz	[4,5]
		5.0V		5		5	2.5	mA	Clock Divide by 16 @ 12 MHz	[4,5]
$I_{CC}2$	Standby Current	3.3V		8		15	1	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		5.0V		10		20	2	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is not Running	[6]
		3.3V		500		600	310	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6]
		5.0V		800		1000	600	µA	STOP Mode V_{IN} = 0V, V_{CC} WDT is Running	[6]
I_{ALL}	Auto Latch Low Current	3.3V		8		10	5	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		15		20	11	µA	$0V < V_{IN} < V_{CC}$	
I_{ALH}	Auto Latch High Current	3.3V		-5		-7	-3	µA	$0V < V_{IN} < V_{CC}$	
		5.0V		-8		-10	-6	µA	$0V < V_{IN} < V_{CC}$	
T_{POR}	Power On Reset	3.3V	7	24	8	25	13	mS		
		5.0V	3	13	4	14	7	mS		
V_{BO}	V_{CC} Brown Out Voltage		1.5	2.65	1.2	2.95	2.1	V	2 MHz max Ext. CLK Freq.	[3]

Notes:

[1]

ICC1	Type	Max	Unit	Freq
Clock Driven on Crystal	3.0 mA	5	mA	8 MHz
or XTAL Resonator	0.3 mA	50	mA	8 MHz

[2] V_{SS}=0V=GND.
[3] 5.0V ± 0.5V, 3.3 V ± 0.3V. The V_{BO} increases as the temperature decreases.
[4] All outputs unloaded, I/O pins floating, inputs at rail.
[5] C_L1=C_L2=100 pF.
[6] Same as note [4] except inputs at V_{CC}.

AC ELECTRICAL CHARACTERISTICS
Additional Timing Diagram

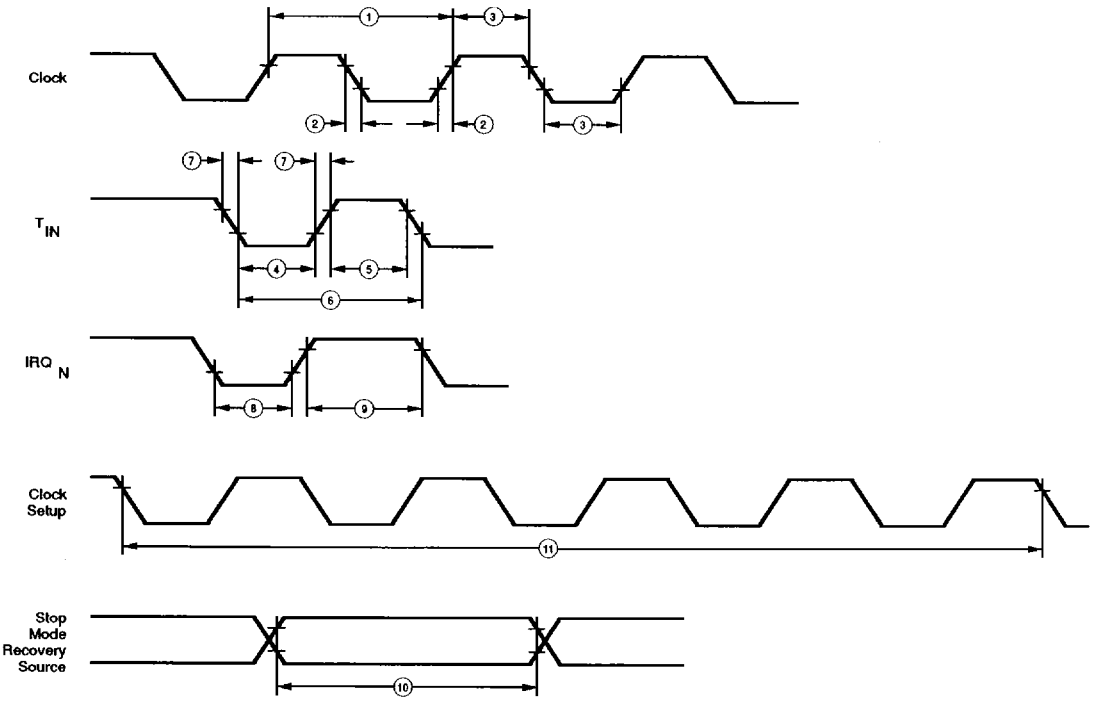


Figure 19. Additional Timing

AC ELECTRICAL CHARACTERISTICS

Additional Timing Table

No	Symbol	Parameter	V_{CC} Note[6]	T_A = 0°C to 70°C				T_A = -40°C to 105°C				Units	Notes
				8 MHz		12 MHz		8 MHz		12 MHz			
				Min	Max	Min	Max	Min	Max	Min	Max		
1	TpC	Input Clock Period	3.3V	125	100000	83	100000	125	100000	83	100000	ns	[1]
			5.0V	125	100000	83	100000	125	100000	83	100000	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times	3.3V		25		15		25		15	ns	[1]
			5.0V		25		15		25		15	ns	[1]
3	TwC	Input Clock Width	3.3V	37		26		37		26		ns	[1]
			5.0V	37		26		37		26		ns	[1]
4	TwTinL	Timer Input Low Width	3.3V	100		100		100		100		ns	[1]
			5.0V	70		70		70		70		ns	[1]
5	TwTinH	Timer Input High Width	3.3V	3TpC		3TpC		3TpC		3TpC			[1]
6	TpTin	Timer Input Period	3.3V	8TpC		8TpC		8TpC		8TpC			[1]
			5.0V	8TpC		8TpC		8TpC		8TpC			[1]
7	TrTin	Timer Input Rise & Fall Timers	3.3V		100		100		100		100	ns	[1]
			5.0V		100		100		100		100	ns	[1]
8A	TwIL	Int. Request Low Time	3.3V	100		100		100		100		ns	[1,2]
			5.0V	70		70		70		70		ns	[1,2]
8B	TwIL	Int. Request Low Time	3.3V	3TpC		3TpC		3TpC		3TpC			[1,3]
			5.0V	3TpC		3TpC		3TpC		3TpC			[1,3]
9	TwIH	Int. Request Input High Time	3.3V	3TpC		3TpC		3TpC		3TpC			[1,2]
			5.0V	3TpC		3TpC		3TpC		3TpC			[1,2]
10	Twsm	STOP Mode Recovery Width Spec	3.3V	12		12		12		12		ns	
			5.0V	12		12		12		12		ns	
			3.3V	5TpC									Reg. SMR - D5=0 No Delay
			5.0V	5TpC									Reg. SMR - D5=1 with Delay
11	Tost	Oscillator Startup Time	3.3V		5TpC		5TpC		5TpC		5TpC		[4]
			5.0V		5TpC		5TpC		5TpC		5TpC		[4]
12	Twdt	Watchdog Timer Delay Time	3.3V	10		10		10		10		ms	D0 = 0 [5]
			5.0V	5		5		5		5		ms	D1 = 0 [5]
			3.3V	30		30		30		30		ms	D0 = 1 [5]
			5.0V	15		15		15		15		ms	D1 = 0 [5]
			3.3V	50		50		50		50		ms	D0 = 0 [5]
			5.0V	25		25		25		25		ms	D1 = 1 [5]
			3.3V	200		200		200		200		ms	D0 = 1 [5]
			5.0V	100		100		100		100		ms	D1 = 1 [5]

Notes:

[1] Timing Reference uses 0.9 V_{CC} for a logic "1" and 0.1 V_{CC} for a logic "0".
[2] Interrupt request via Port 3 (P31-P33).
[3] Interrupt request via Port 3 (P30).
[4] SMR-D5 = 0.
[5] Reg. WDTMR.
[6] 5.0V ± 0.5V, 3.3V ± 0.3V.

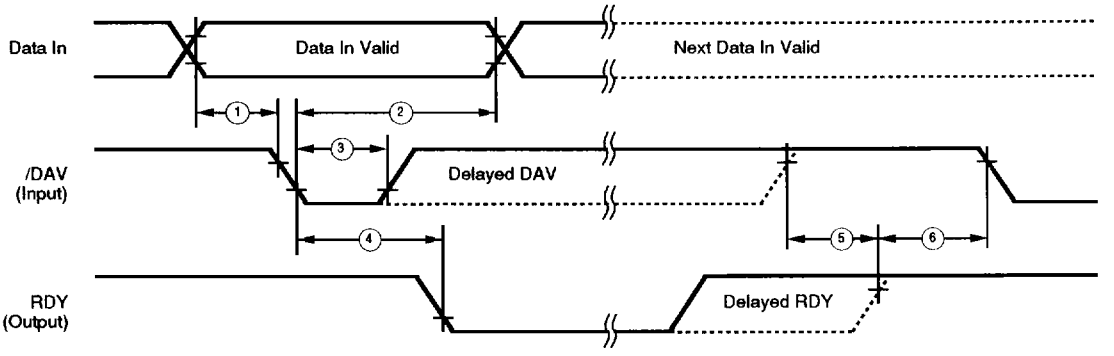


Figure 20. Input Handshake Timing

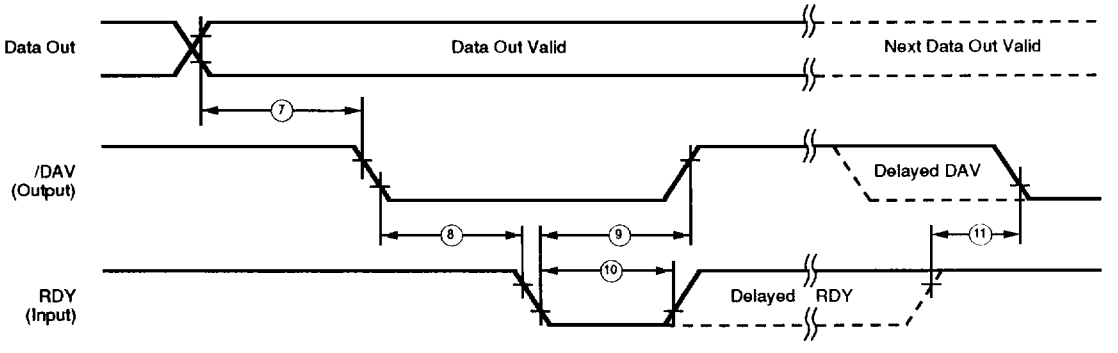


Figure 21. Output Handshake Timing

AC ELECTRICAL CHARACTERISTICS (Continued)
Handshake Timing Table

No	Symbol	Parameter	V_{cc} Note[1]	T_A = 0°C to 70°C				T_A = -40°C to 105°C				Notes
				8 MHz		12 MHz		8 MHz		12 MHz		
				Min	Max	Min	Max	Min	Max	Min	Max	
1	TsDI(DAV)	Data In Setup Time	3.3V	0		0		0		0		IN
			5.0V	0		0		0		0		IN
2	ThDI(DAV)	Data In Hold Time	3.3V	160		160		160		160		IN
			5.0V	115		115		115		115		IN
3	TwDAV	Data Available Width	3.3V	155		155		155		155		IN
			5.0V	110		110		110		110		IN
4	TdDAVI(RDY)	DAV Fall to RDY Fall Delay	3.3V		160		160		160		160	IN
			5.0V		115		115		115		115	IN
5	TdDAVId(RDY)	DAV Rise to RDY Rise Delay	3.3V		120		120		120		120	IN
			5.0V		80		80		80		80	IN
6	TdDO(DAV)	RDY Rise to DAV Fall Delay	3.3V	0		0		0		0		IN
			5.0V	0		0		0		0		IN
7	TcLDAV0(RDY)	Data Out to	3.3V	63		42		63		42		OUT
		DAV Fall Delay	5.0V	63		42		63		42		OUT
8	TcLDAV0(RDY)	DAV Fall to RDY Fall Delay	3.3V	0		0		0		0		OUT
			5.0V	0		0		0		0		OUT
9	TdRDY0(DAV)	RDY Fall to DAV Rise Delay	3.3V		160		160		160		160	OUT
			5.0V		115		115		115		115	OUT
10	TwRDY	RDY Width	3.3V	110		110		110		110		OUT
			5.0V	80		80		80		80		OUT
11	TdRDY0d(DAV)	RDY Rise to DAV Fall Delay	3.3V		110		110		110		110	OUT
			5.0V		80		80		80		80	OUT

Note:
[1] 5.0 V ± 0.5V, 3.3V ± 0.3V.

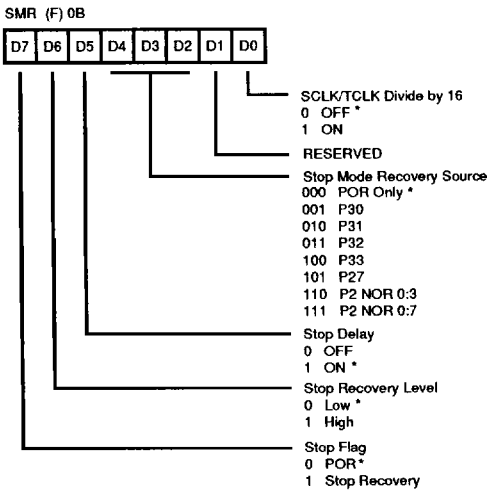


Figure 22. Stop Mode Recovery Register

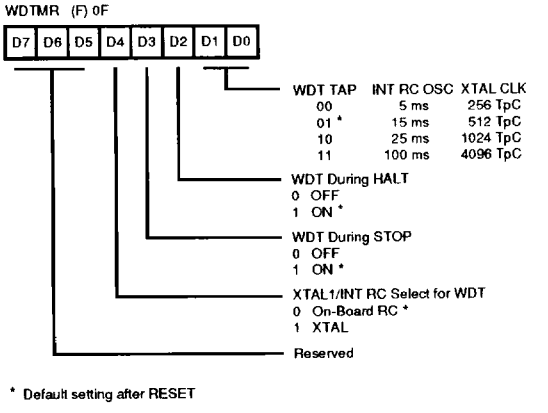


Figure 23. Watchdog Timer Mode Register

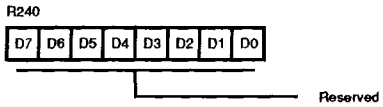


Figure 24. Reserved

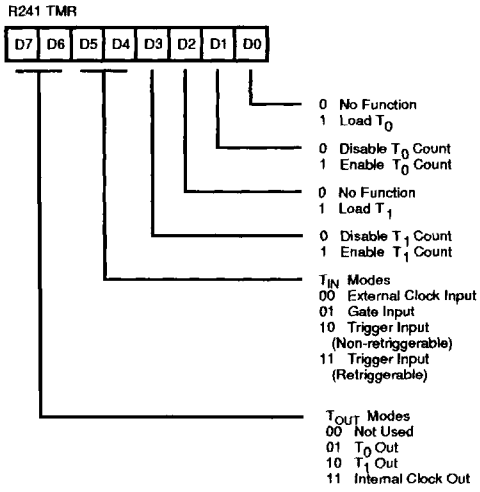


Figure 25. Timer Mode Register
(F1H: Read/Write)

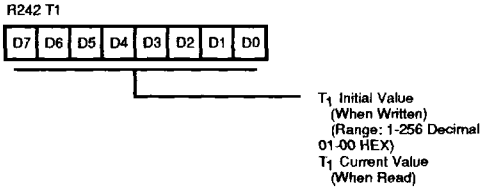


Figure 26. Counter Timer 1 Register
(F2H: Read/Write)

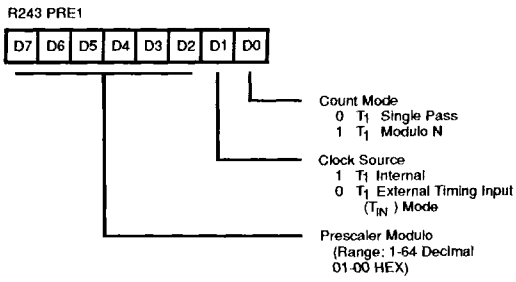


Figure 27. Prescaler 1 Register
(F3H: Write Only)

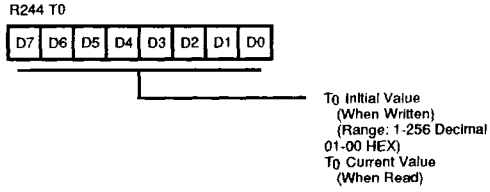


Figure 28. Counter/Timer 0 Register
(F4H: Read/Write)

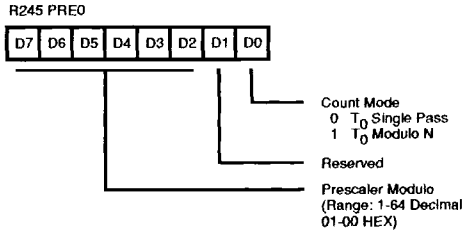


Figure 29. Prescaler 0 Register
(F5H: Write Only)

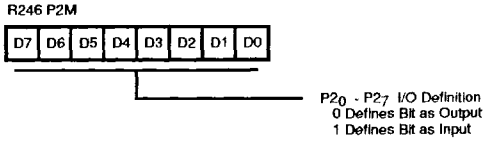


Figure 30. Port 2 Mode Register
(F6H: Write Only)

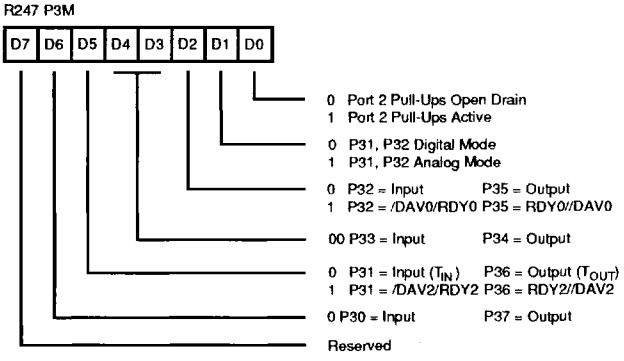


Figure 31. Port 3 Mode Register (F7H: Write Only)

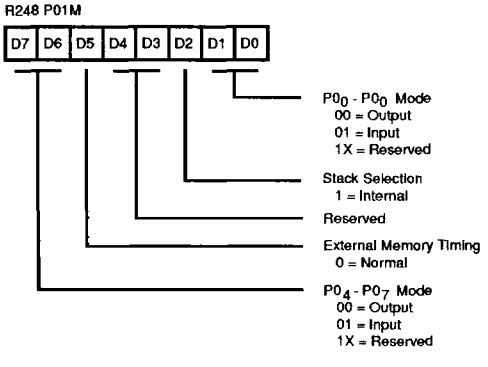


Figure 32. Port 0 and 1 Mode Register (F8H: Write Only)

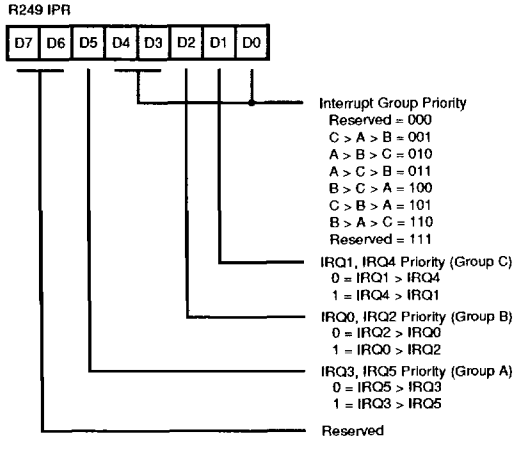


Figure 33. Interrupt Priority Register (F9H: Write Only)

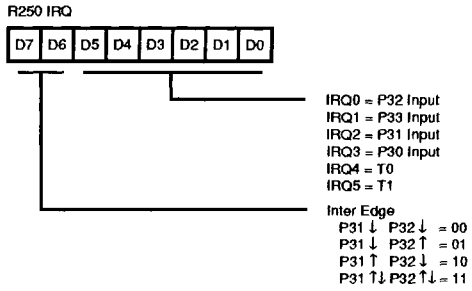


Figure 34. Interrupt Request Register (FAH: Read/Write)

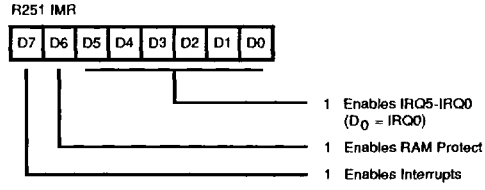


Figure 35. Interrupt Mask Register (FBH: Read/Write)

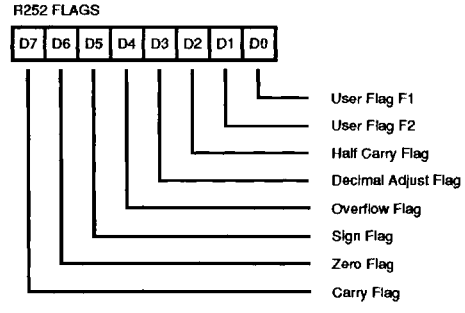


Figure 36. Flag Register (FCH: Read/Write)

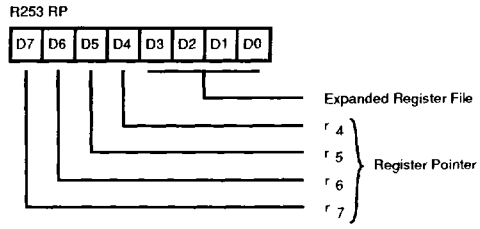


Figure 37. Register Pointer (FDH: Read/Write)

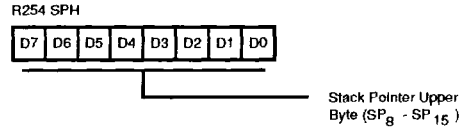


Figure 38. Reserved

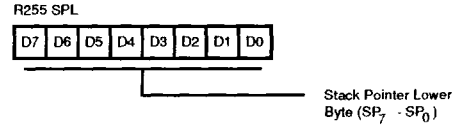


Figure 39. Stack Pointer (FFH: Read/Write)

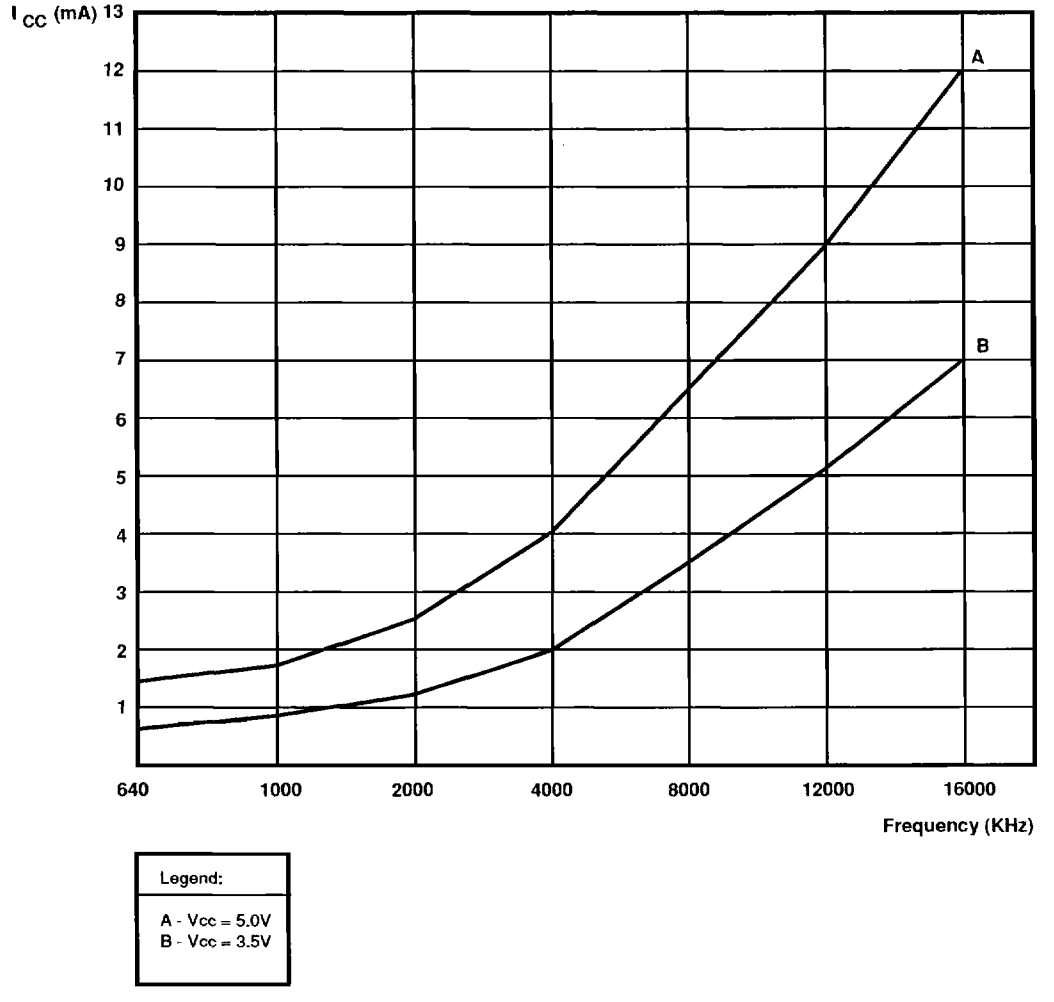


Figure 40. Typical I_{cc} vs Frequency

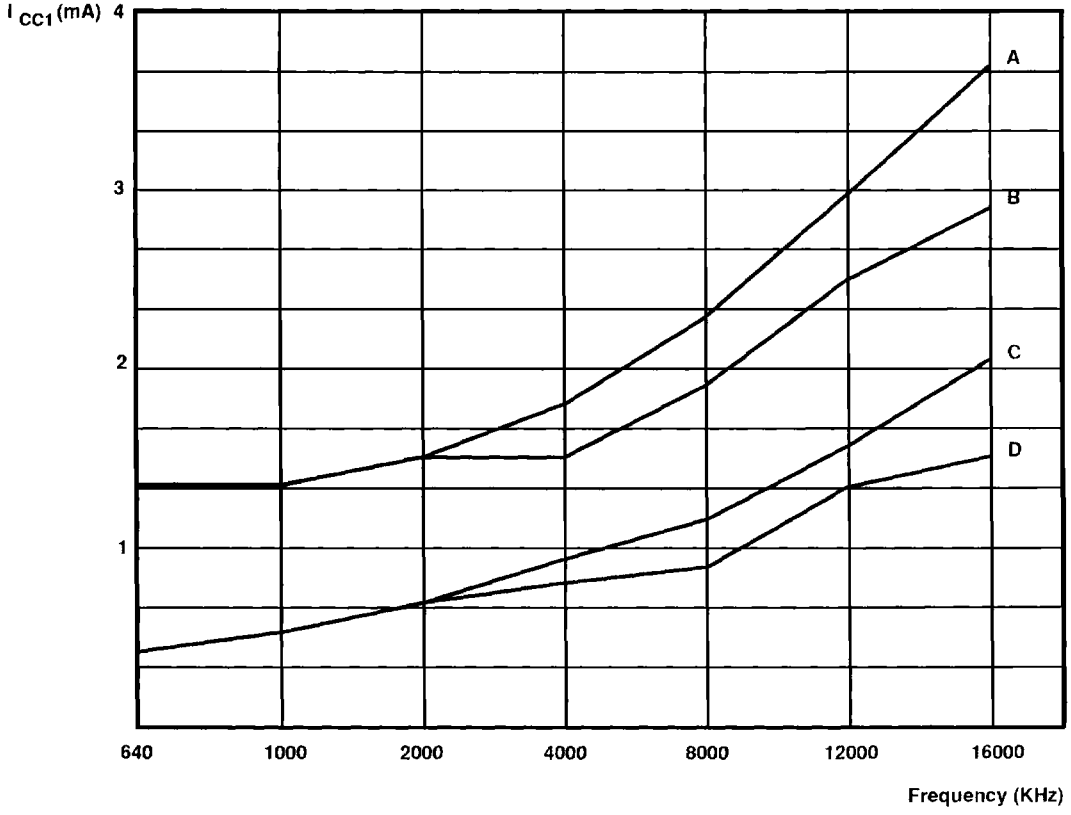
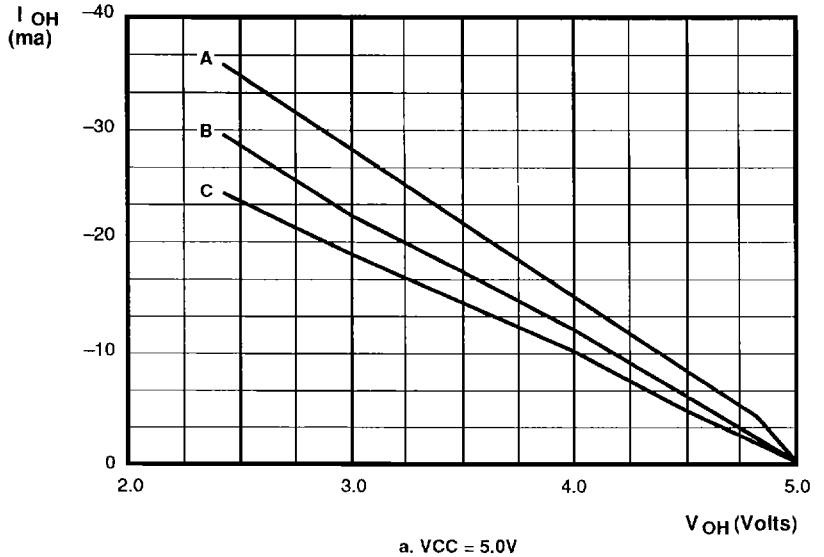
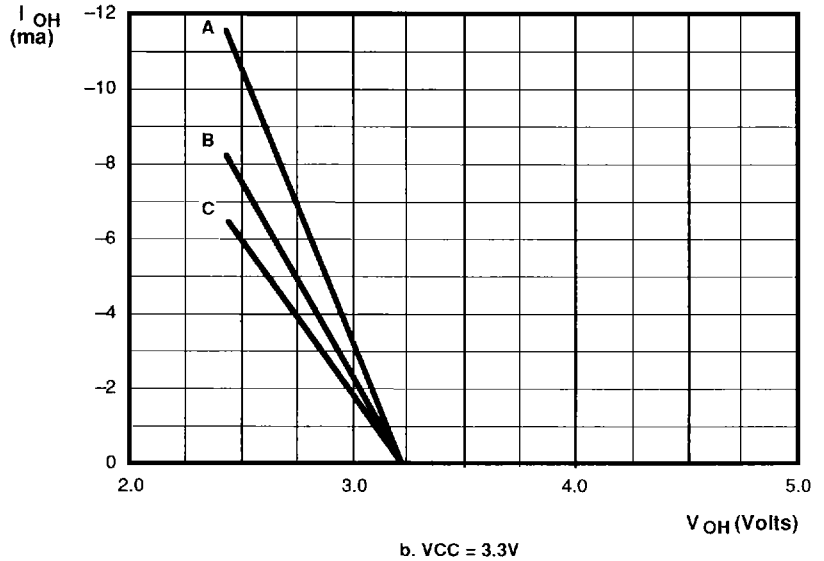


Figure 41. Typical I_{CC1} vs Frequency



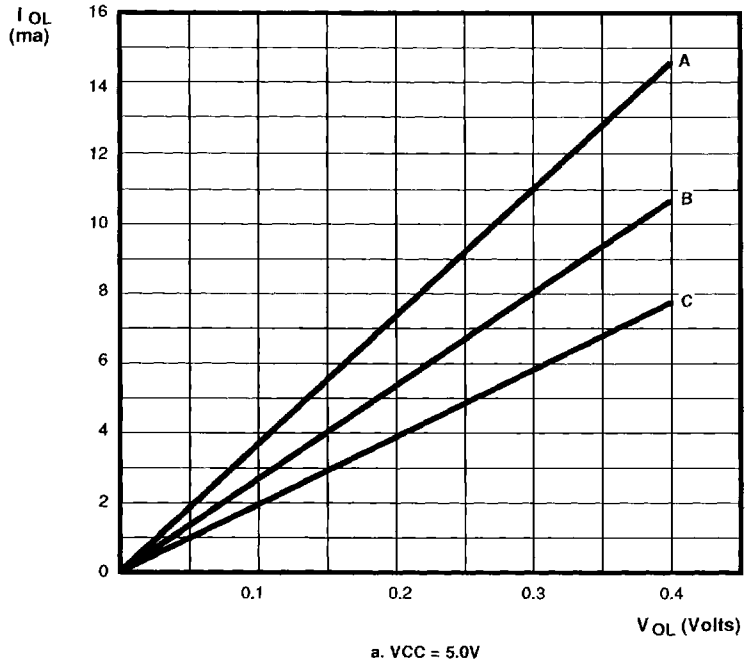
a. VCC = 5.0V



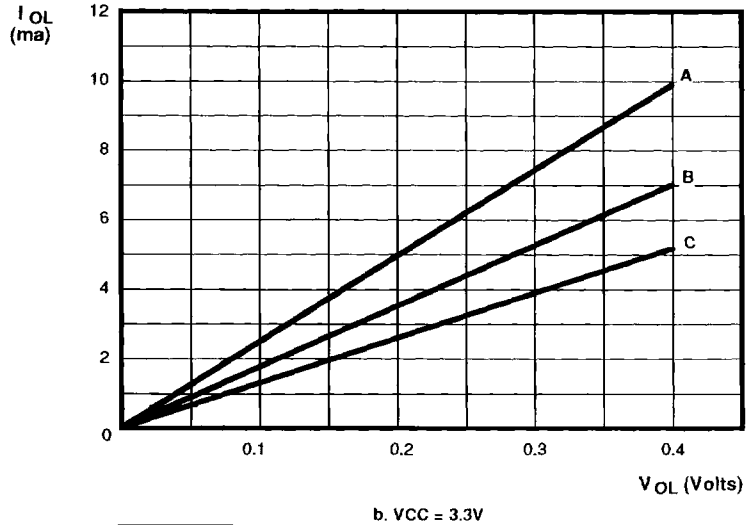
b. VCC = 3.3V

Legend:
A = –55°C B = 25°C C = 125°C

Figure 42. Typical I_{OH} vs V_{OH} Over Temperature



a. VCC = 5.0V



b. VCC = 3.3V

Legend:
A = –55°C B = 25°C C = 125°C

Figure 43. Typical I_{OL} vs V_{OL} Over Temperature

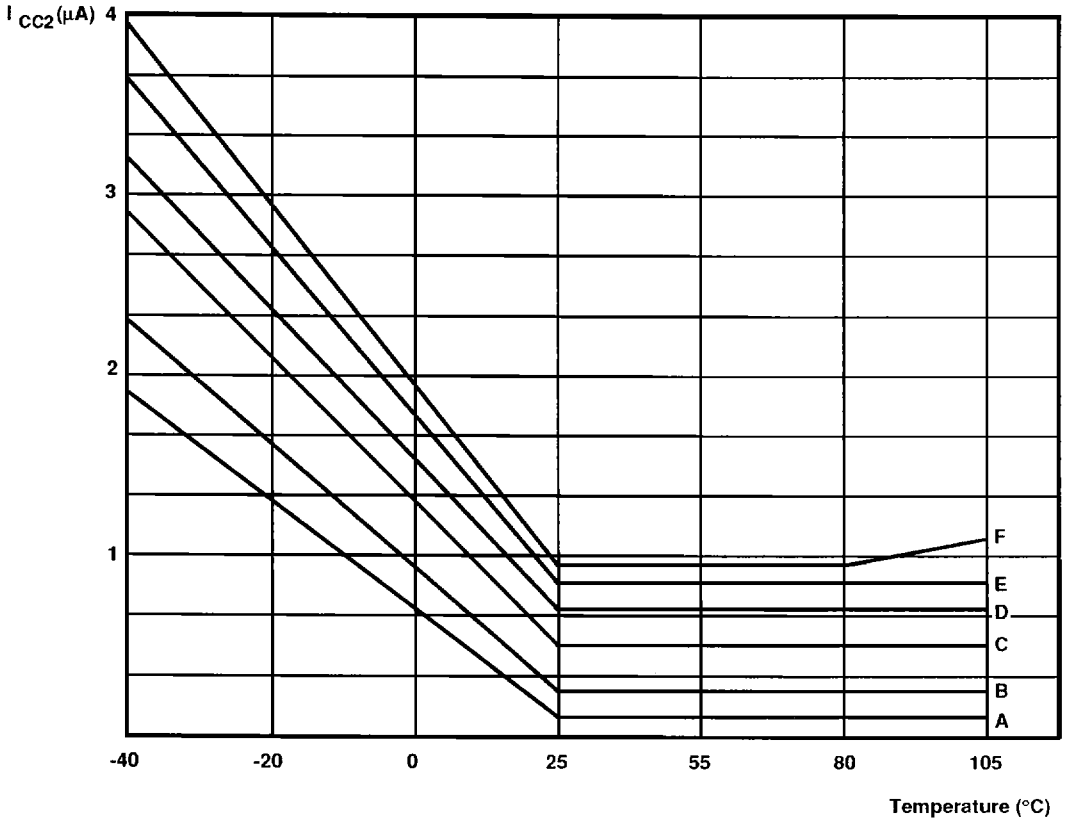


Figure 44. Typical I_{CC2} vs Temperature

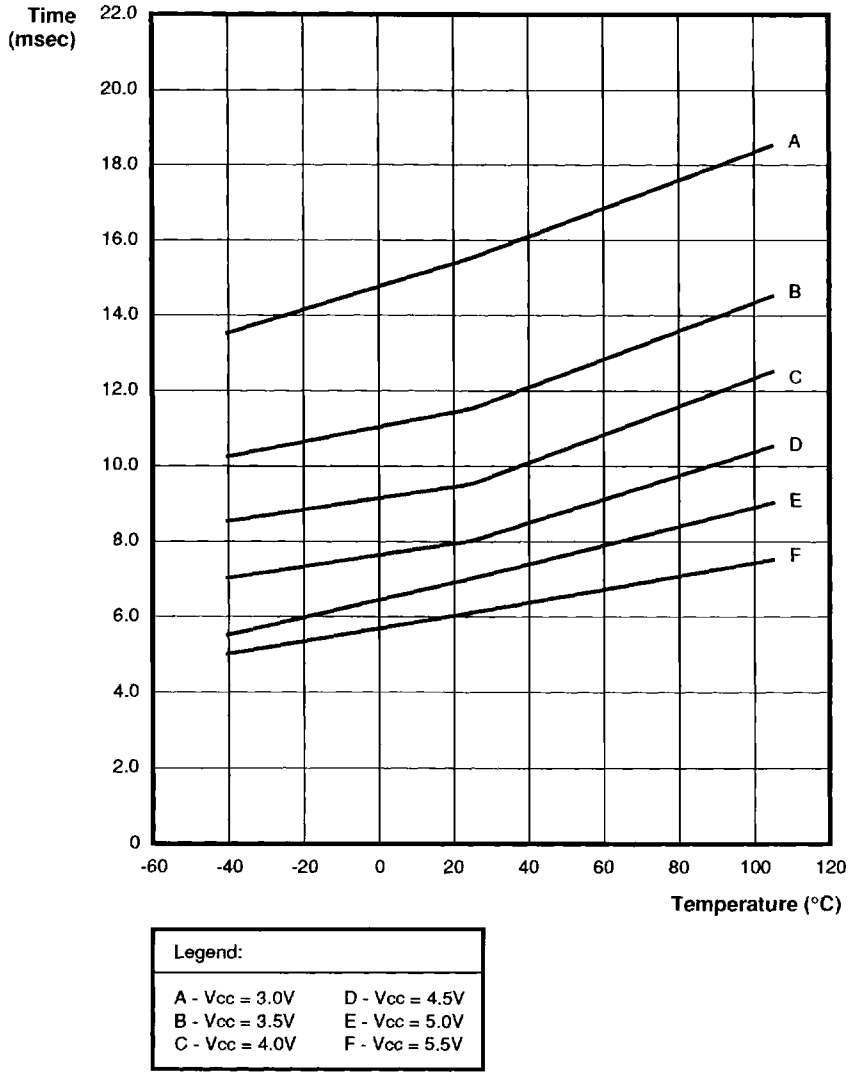
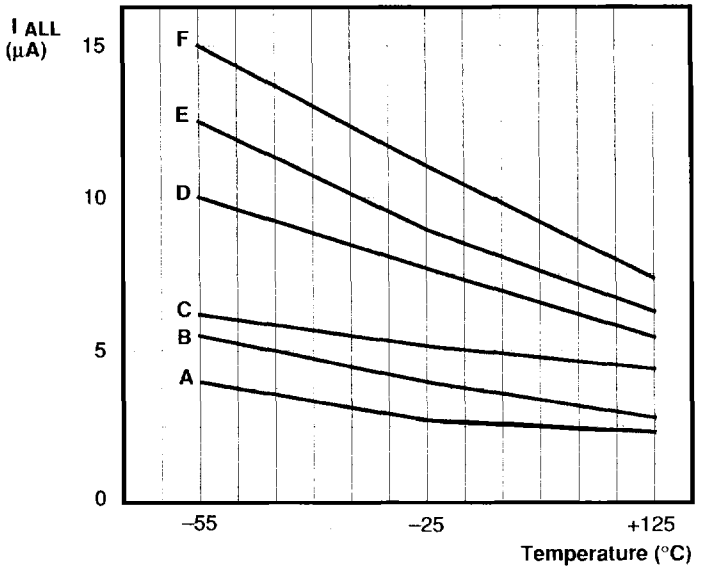
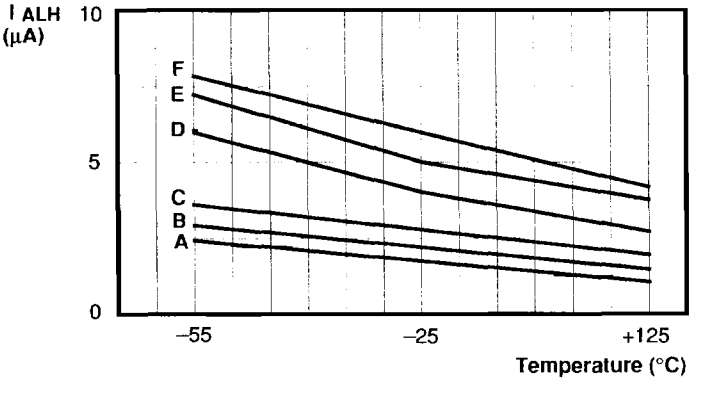


Figure 45. Typical Power-On Reset Time vs Temperature



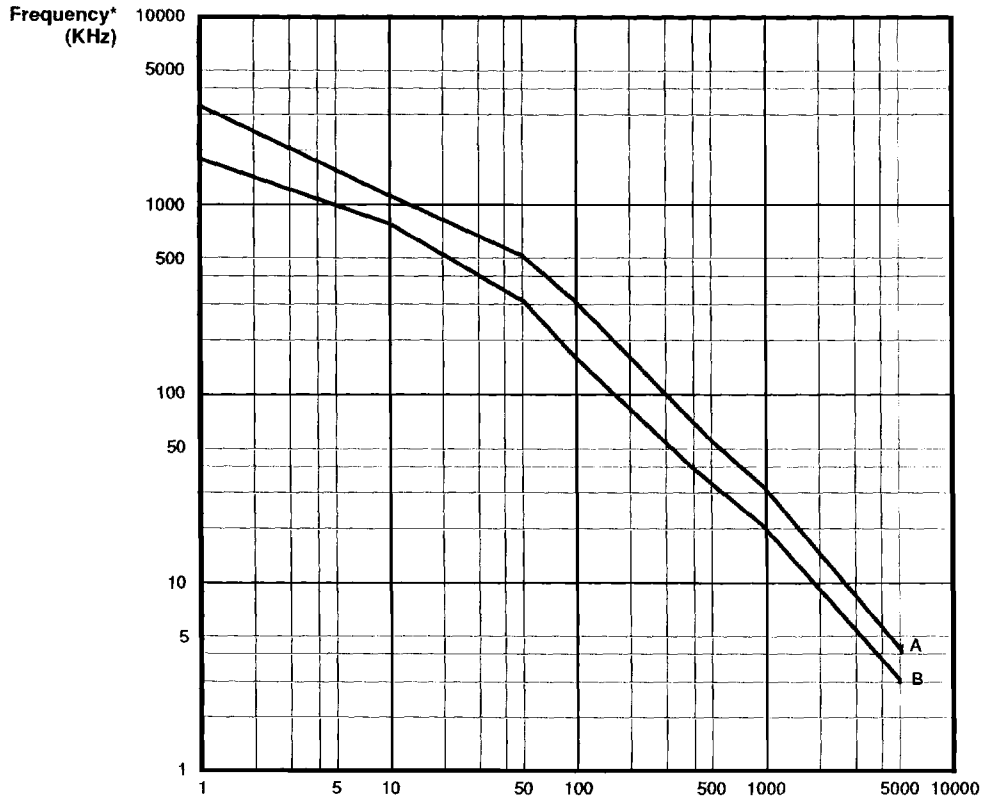
a. Typical Auto Latch Low Current vs Temperature



b. Typical Auto Latch High Current vs Temperature

Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.3V	E - Vcc = 5.0V
C - Vcc = 3.6V	F - Vcc = 5.5V

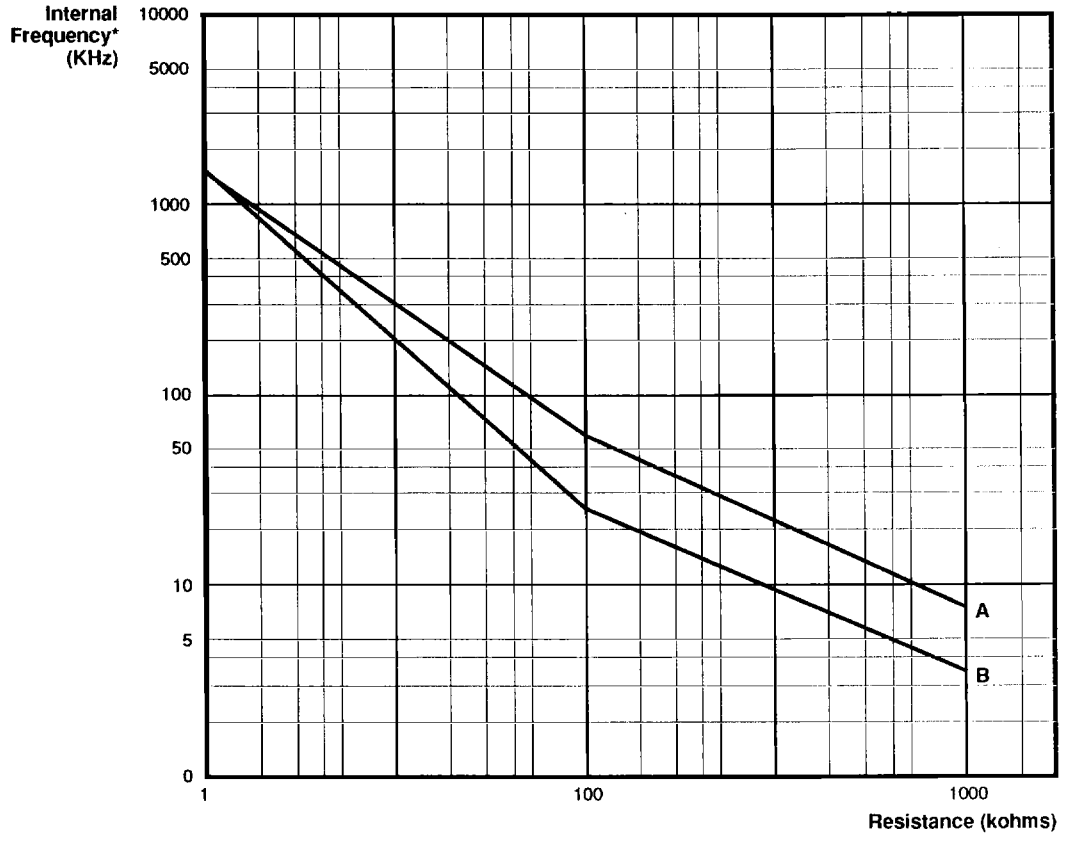
Figure 46. Typical Auto-Latch Current vs Temperature



Legend:
A - Vcc = 5.0V C = 33 pF B - Vcc = 3.3V C = 33 pF

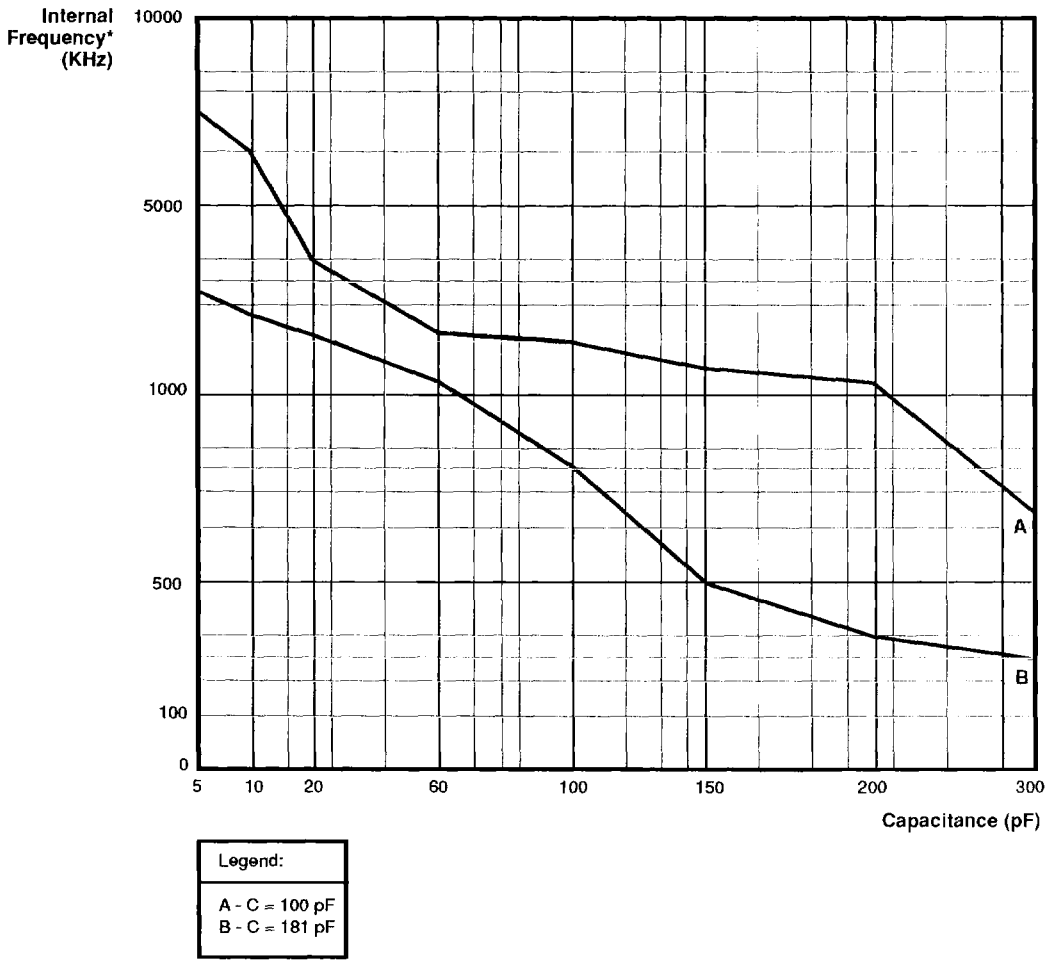
Note: * The internal clock frequency is one half the external clock frequency.
This chart for reference only. Each process will have a different characteristc curve.

Figure 47. Typical Internal Frequency vs RC Resistance



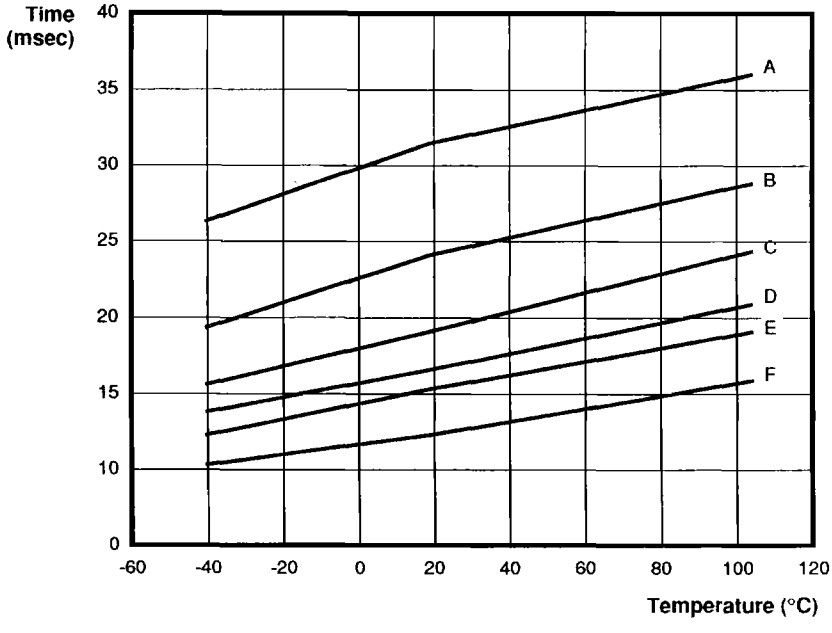
Note: * The internal clock frequency is one half the external clock frequency.
This chart for reference only. Each process will have a different characteristc curve.

Figure 48. Typical Internal Frequency vs Resistance



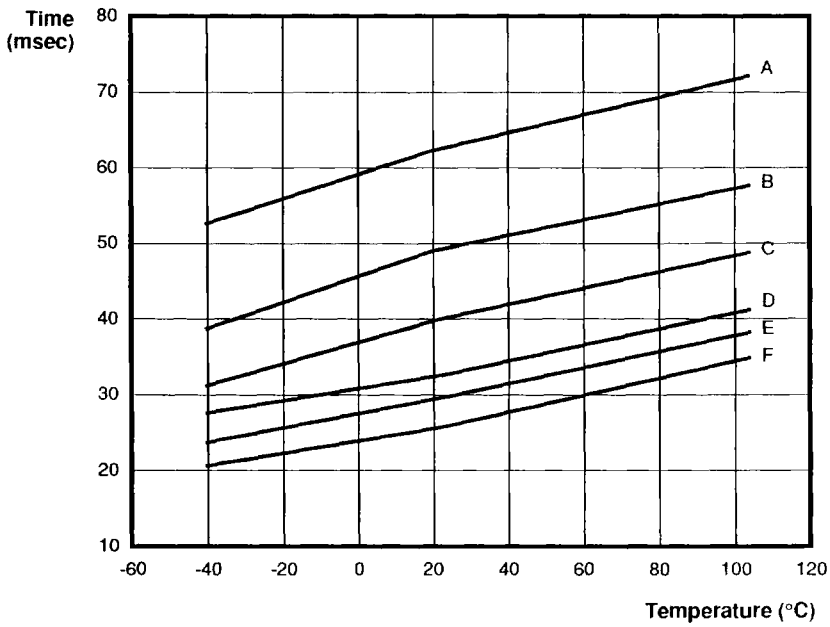
Note: * The internal clock frequency is one half the external clock frequency.
This chart for reference only. Each process will have a different characteristc curve.
R = 1 kohm

Figure 49. Typical Internal Frequency vs RC Capacitance



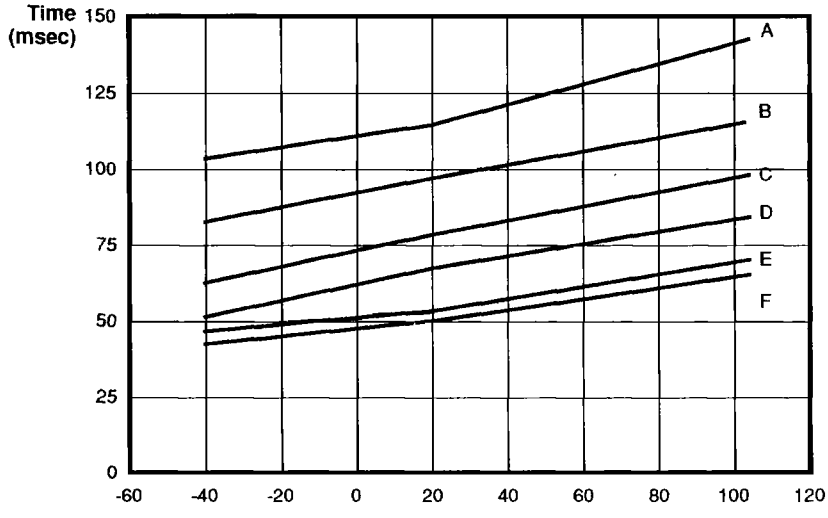
Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 50. Typical 5 ms WDT Setting vs Temperature



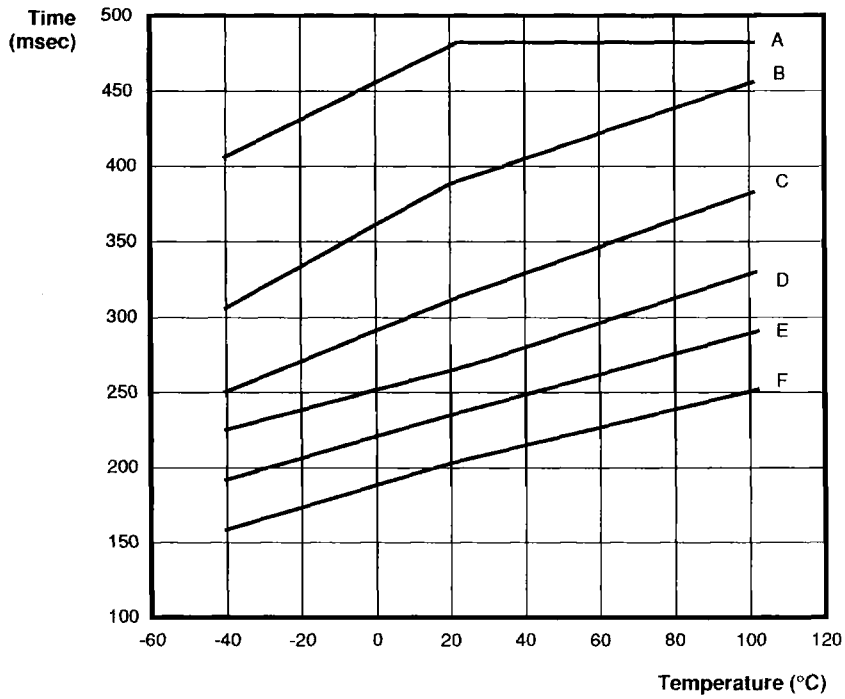
Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 51. Typical 15 ms WDT Setting vs Temperature



Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 52. Typical 25 ms WDT Setting vs Temperature



Legend:	
A - Vcc = 3.0V	D - Vcc = 4.5V
B - Vcc = 3.5V	E - Vcc = 5.0V
C - Vcc = 4.0V	F - Vcc = 5.5V

Figure 53. Typical 100 ms WDT Setting vs Temperature

INSTRUCTION SET NOTATION

Addressing Modes. The following notation is used to describe the addressing modes and instruction operations as shown in the instruction summary.

Symbol	Meaning
IRR	Indirect register pair or indirect working-register pair address
Irr	Indirect working-register pair only
X	Indexed address
DA	Direct address
RA	Relative address
IM	Immediate
R	Register or working-register address
r	Working-register address only
IR	Indirect-register or indirect working-register address
Ir	Indirect working-register address only
RR	Register pair or working register pair address

Symbols. The following symbols are used in describing the instruction set.

Symbol	Meaning
dst	Destination location or contents
src	Source location or contents
cc	Condition code
@	Indirect address prefix
SP	Stack Pointer
PC	Program Counter
FLAGS	Flag register (Control Register 252)
RP	Register Pointer (R253)
IMR	Interrupt mask register (R251)

Flags. Control register (R252) contains the following six flags:

Symbol	Meaning
C	Carry flag
Z	Zero flag
S	Sign flag
V	Overflow flag
D	Decimal-adjust flag
H	Half-carry flag

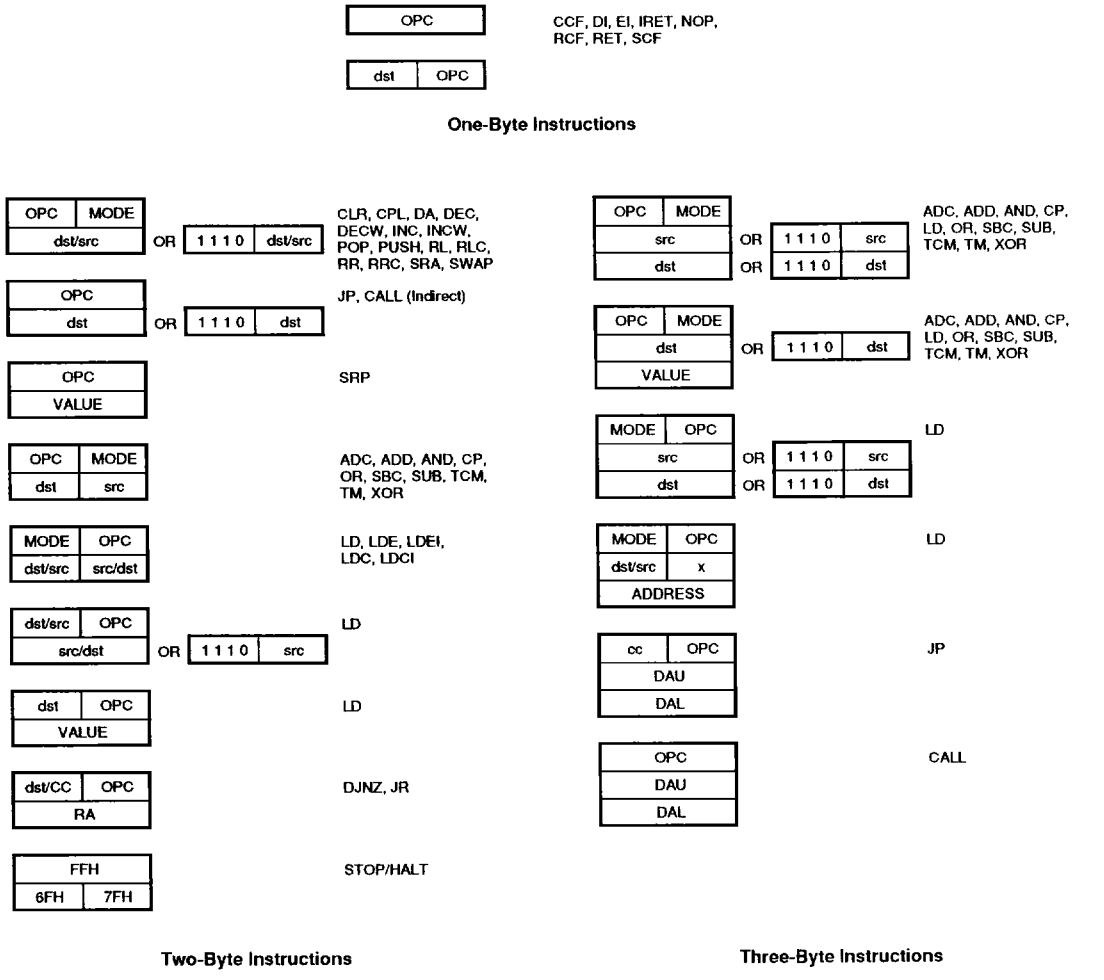
Affected flages are indicated by:

0	Clear to zero
1	Set to one
*	Set to clear according to operation
-	Unaffected
x	Undefined

CONDITION CODES

Value	Mnemonic	Meaning	Flags Set
1000		Always True	
0111	C	Carry	C = 1
1111	NC	No Carry	C = 0
0110	Z	Zero	Z = 1
1110	NZ	Not Zero	Z = 0
1101	PL	Plus	S = 0
0101	MI	Minus	S = 1
0100	OV	Overflow	V = 1
1100	NOV	No Overflow	V = 0
0110	EQ	Equal	Z = 1
1110	NE	Not Equal	Z = 0
1001	GE	Greater Than or Equal	(S XOR V) = 0
0001	LT	Less than	(S XOR V) = 1
1010	GT	Greater Than	[Z OR (S XOR V)] = 0
0010	LE	Less Than or Equal	[Z OR (S XOR V)] = 1
1111	UGE	Unsigned Greater Than or Equal	C = 0
0111	ULT	Unsigned Less Than	C = 1
1011	UGT	Unsigned Greater Than	(C = 0 AND Z = 0) = 1
0011	ULE	Unsigned Less Than or Equal	(C OR Z) = 1
0000		Never True	

INSTRUCTION FORMATS



INSTRUCTION SUMMARY

Note: Assignment of a value is indicated by the symbol " ← ". For example:

dst ← dst + src

indicates that the source data is added to the destination data and the result is stored in the destination location.

The notation "addr (n)" is used to refer to bit (n) of a given operand location. For example:

dst (7)

refers to bit 7 of the destination operand.

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
ADC dst, src dst←dst + src +C	†		1[ ]	*	*	*	*	0	*
ADD dst, src dst←dst + src	†		0[ ]	*	*	*	*	0	*
AND dst, src dst←dst AND src	†		5[ ]	-	*	*	0	-	-
CALL dst SP←SP - 2 @SP←PC, PC←dst	DA IRR		D6 D4	-	-	-	-	-	-
CCF C←NOT C			EF	*	-	-	-	-	-
CLR dst dst←0	R IR		B0 B1	-	-	-	-	-	-
COM dst dst←NOT dst	R IR		60 61	-	*	*	0	-	-
CP dst, src dst - src	†		A[ ]	*	*	*	*	-	-
DA dst dst←DA dst	R IR		40 41	*	*	*	X	-	-
DEC dst dst←dst - 1	R IR		00 01	-	*	*	*	-	-
DECW dst dst←dst - 1	RR IR		80 81	-	*	*	*	-	-
DI IMR(7)←0			8F	-	-	-	-	-	-
DJNZr, dst r←r - 1 if r ≠ 0 PC←PC + dst Range: +127, -128	RA		rA r = 0 - F	-	-	-	-	-	-
EI IMR(7)←1			9F	-	-	-	-	-	-
HALT			7F	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
INC dst dst←dst + 1	r		rE r = 0 - F	-	*	*	*	-	-
	R		20						
	IR		21						
INCW dst dst←dst + 1	RR IR		A0 A1	-	*	*	*	-	-
IRET FLAGS←@SP; SP←SP + 1 PC←@SP; SP←SP + 2; IMR(7)←1			BF	*	*	*	*	*	*
JP cc, dst if cc is true PC←dst	DA IRR		cD c = 0 - F 30	-	-	-	-	-	-
JR cc, dst if cc is true, PC←PC + dst Range: +127, -128	RA		cB c = 0 - F	-	-	-	-	-	-
LD dst, src dst←src	r	Im	rC	-	-	-	-	-	-
	r	R	r8						
	R	r	r9						
			r = 0 - F						
	r	X	C7						
	X	r	D7						
	r	Ir	E3						
	Ir	r	F3						
	R	R	E4						
	R	IR	E5						
	R	IM	E6						
	IR	IM	E7						
	IR	R	F5						
LDC dst, src	r	Irr	C2	-	-	-	-	-	-
LDCI dst, src dst←src r←r +1; rr←rr + 1	Ir	Irr	C3	-	-	-	-	-	-

INSTRUCTION SUMMARY (Continued)

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
NOP			FF	-	-	-	-	-	-
OR dst, src dst←dst OR src	†		4[ ]	-	*	*	0	-	-
POP dst dst←@SP; SP←SP + 1	R IR		50 51	-	-	-	-	-	-
PUSH src SP←SP - 1; @SP←src		R IR	70 71	-	-	-	-	-	-
RCF C←0			CF	0	-	-	-	-	-
RET PC←@SP; SP←SP + 2			AF	-	-	-	-	-	-
RL dst	R IR		90 91	*	*	*	*	-	-
RLC dst	R IR		10 11	*	*	*	*	-	-
RR dst	R IR		E0 E1	*	*	*	*	-	-
RRC dst	R IR		C0 C1	*	*	*	*	-	-
SBC dst, src dst←dst←src←C	†		3[ ]	*	*	*	*	1	*
SCF C←1			DF	1	-	-	-	-	-
SRA dst	R IR		D0 D1	*	*	*	0	-	-
SRP src RP←src		Im	31	-	-	-	-	-	-

Instruction and Operation	Address Mode dst	Address Mode src	Opcode Byte (Hex)	Flags Affected C	Z	S	V	D	H
STOP			6F	-	-	-	-	-	-
SUB dst, src dst←dst←src	†		2[ ]	*	*	*	*	1	*
SWAP dst	R IR		F0 F1	X	*	*	X	-	-
TCM dst, src (NOT dst) AND src	†		6[ ]	-	*	*	0	-	-
TM dst, src dst AND src	†		7[ ]	-	*	*	0	-	-
XOR dst, src dst←dst XOR src	†		B[ ]	-	*	*	0	-	-

† These instructions have an identical set of addressing modes, which are encoded for brevity. The first opcode nibble is found in the instruction set table above. The second nibble is expressed symbolically by a '[ ]' in this table, and its value is found in the following table to the left of the applicable addressing mode pair.

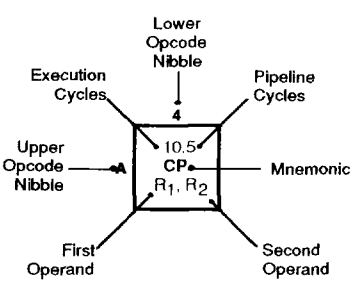
For example, the opcode of an ADC instruction using the addressing modes r (destination) and Ir (source) is 13.

Address Mode dst	Address Mode src	Lower Opcode Nibble
r	r	[2]
r	Ir	[3]
R	R	[4]
R	IR	[5]
R	IM	[6]
IR	IM	[7]

OPCODE MAP

Lower Nibble (Hex)

Upper Nibble (Hex)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	6.5 **DEC** R1	6.5 **DEC** IR1	6.5 **ADD** r1, r2	6.5 **ADD** r1, Ir2	10.5 **ADD** R2, R1	10.5 **ADD** IR2, R1	10.5 **ADD** R1, IM	10.5 **ADD** IR1, IM	6.5 **LD** r1, R2	6.5 **LD** r2, R1	12/10.5 **DJNZ** r1, RA	12/10.0 **JR** cc, RA	6.5 **LD** r1, IM	12.10.0 **JP** cc, DA	6.5 **INC** r1	
1	6.5 **RLC** R1	6.5 **RLC** IR1	6.5 **ADC** r1, r2	6.5 **ADC** r1, Ir2	10.5 **ADC** R2, R1	10.5 **ADC** IR2, R1	10.5 **ADC** R1, IM	10.5 **ADC** IR1, IM								
2	6.5 **INC** R1	6.5 **INC** IR1	6.5 **SUB** r1, r2	6.5 **SUB** r1, Ir2	10.5 **SUB** R2, R1	10.5 **SUB** IR2, R1	10.5 **SUB** R1, IM	10.5 **SUB** IR1, IM								
3	8.0 **JP** IRR1	6.1 **SRP** IM	6.5 **SBC** r1, r2	6.5 **SBC** r1, Ir2	10.5 **SBC** R2, R1	10.5 **SBC** IR2, R1	10.5 **SBC** R1, IM	10.5 **SBC** IR1, IM								
4	8.5 **DA** R1	8.5 **DA** IR1	6.5 **OR** r1, r2	6.5 **OR** r1, Ir2	10.5 **OR** R2, R1	10.5 **OR** IR2, R1	10.5 **OR** R1, IM	10.5 **OR** IR1, IM								6.0 **WHD**
5	10.5 **POP** R1	10.5 **POP** IR1	6.5 **AND** r1, r2	6.5 **AND** r1, Ir2	10.5 **AND** R2, R1	10.5 **AND** IR2, R1	10.5 **AND** R1, IM	10.5 **AND** IR1, IM								6.0 **WDT**
6	6.5 **COM** R1	6.5 **COM** IR1	6.5 **TCM** r1, r2	6.5 **TCM** r1, Ir2	10.5 **TCM** R2, R1	10.5 **TCM** IR2, R1	10.5 **TCM** R1, IM	10.5 **TCM** IR1, IM								6.0 **STOP**
7	10/12.1 **PUSH** R2	12/14.1 **PUSH** IR2	6.5 **TM** r1, r2	6.5 **TM** r1, Ir2	10.5 **TM** R2, R1	10.5 **TM** IR2, R1	10.5 **TM** R1, IM	10.5 **TM** IR1, IM								7.0 **HALT**
8	10.5 **DECW** RR1	10.5 **DECW** IR1														6.1 **DI**
9	6.5 **RL** R1	6.5 **RL** IR1														6.1 **EI**
A	10.5 **INCW** RR1	10.5 **INCW** IR1	6.5 **CP** r1, r2	6.5 **CP** r1, Ir2	10.5 **CP** R2, R1	10.5 **CP** IR2, R1	10.5 **CP** R1, IM	10.5 **CP** IR1, IM								14.0 **RET**
B	6.5 **CLR** R1	6.5 **CLR** IR1	6.5 **XOR** r1, r2	6.5 **XOR** r1, Ir2	10.5 **XOR** R2, R1	10.5 **XOR** IR2, R1	10.5 **XOR** R1, IM	10.5 **XOR** IR1, IM								16.0 **IRET**
C	6.5 **RRC** R1	6.5 **RRC** IR1	12.0 **LDC** r1, Irr2	18.0 **LDCI** Ir1, Irr2				10.5 **LD** r1,x,R2								6.5 **RCF**
D	6.5 **SRA** R1	6.5 **SRA** IR1			20.0 **CALL*** IRR1		20.0 **CALL** DA	10.5 **LD** r2,x,R1								6.5 **SCF**
E	6.5 **RR** R1	6.5 **RR** IR1		6.5 **LD** r1, IR2	10.5 **LD** R2, R1	10.5 **LD** IR2, R1	10.5 **LD** R1, IM	10.5 **LD** IR1, IM								6.5 **CCF**
F	8.5 **SWAP** R1	8.5 **SWAP** IR1		6.5 **LD** Ir1, r2		10.5 **LD** R2, IR1										6.0 **NOP**
Bytes per Instruction	2			3					2					3	1	



Legend:
R = 8-bit address
r = 4-bit address
R_1 or r_2 = Dst address
R_1 or r_2 = Src address

Sequence:
Opcode, First Operand, Second Operand

Note: The blank are not defined.

* 2-byte instruction appears as a 3-byte instruction