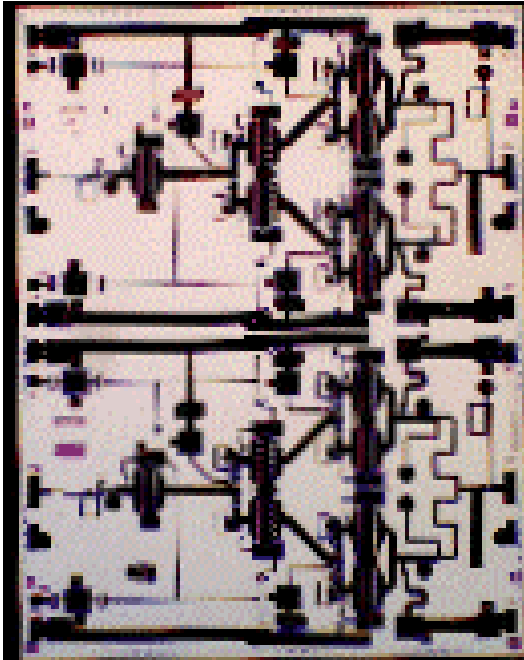


**6 - 18 GHz High Power Amplifier**

**TGA9092-SCC**



Chip Dimensions 5.739 mm x 4.318 mm x 0.1016 mm

**Product Description**

The TriQuint TGA9092-SCC is a dual channel, three-stage wide band HPA MMIC designed using TriQuint's proven 0.25  $\mu$ m Power pHEMT process to support a variety of high performance applications including military EW programs, VSAT, and other applications requiring wideband high power performance.

Each amplifier channel consists of one 1200  $\mu$ m input device driving a 2400  $\mu$ m intermediate stage which drives a 4800  $\mu$ m output stage.

The TGA9092-SCC provides a nominal 34 dBm of output power at 2dB gain compression across the 6-18 GHz range per channel . Power combined, nominal output power of 36.5 dBm can be expected with low loss external couplers. Typical per channel small signal gain is 24 dB. Typical single-ended Input/Output RL is 6-8 dB across the band.

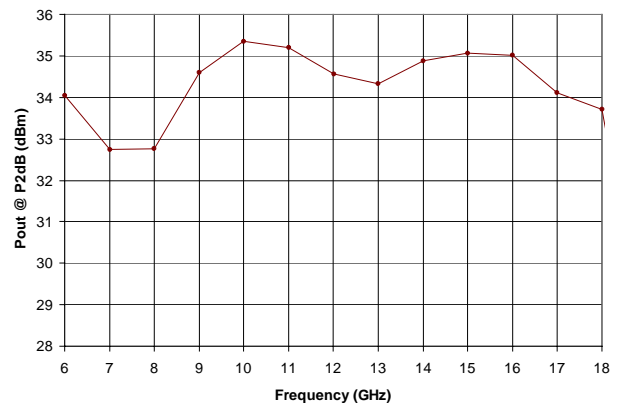
The TGA9092-SCC is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in chip form.

**Key Features and Performance**

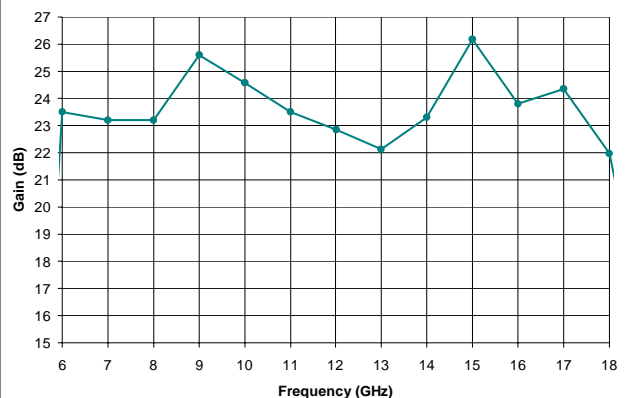
- Dual Channel Power Amplifier
- 0.25 $\mu$ m pHEMT Technology
- 6-18 GHz Frequency Range
- 2.8 W/Channel Midband Pout
- 5.6 W Pout Combined
- 24 dB Nominal Gain
- Balanced In/Out for Low VSWR
- 8V @ 1.2A per Channel Bias

**Primary Applications**

- X-Ku band High Power
- VSAT



Typical Measured Pout (RF Probe)



Typical Measured Small Signal Gain

TABLE I  
MAXIMUM RATINGS

Symbol	Parameter <u>5/</u>	Value	Notes
V <sup>+</sup>	Positive Supply Voltage	9 V	<u>4/</u>
V <sup>-</sup>	Negative Supply Voltage Range	-5V TO 0V	
I <sup>+</sup>	Positive Supply Current (Quiescent)	3.5 A	<u>4/</u>
I <sub>G</sub>	Gate Supply Current	84.48 mA	
P <sub>IN</sub>	Input Continuous Wave Power	26 dBm	<u>4/</u>
P <sub>D</sub>	Power Dissipation	28.8 W	<u>3/ 4/</u>
T <sub>CH</sub>	Operating Channel Temperature	150 °C	<u>1/ 2/</u>
T <sub>M</sub>	Mounting Temperature (30 Seconds)	320 °C	
T <sub>STG</sub>	Storage Temperature	-65 to 150 °C	

- 1/ These ratings apply to each individual FET.
- 2/ Junction operating temperature will directly affect the device median time to failure (T<sub>M</sub>). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 3/ When operated at this bias condition with a base plate temperature of 70 °C, the median life is reduced from 1.6 E+6 to 5.4 E+4 hours.
- 4/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P<sub>D</sub>.
- 5/ These ratings represent the maximum operable values for this two-channel device.

TABLE II  
DC PROBE TEST  
(TA = 25 °C ± 5 °C)

Symbol	Parameter	Minimum	Maximum	Unit
I <sub>max(Q1)</sub>	Maximum Current	400	800	mA
G <sub>m (Q1)</sub>	Transconductance	200	600	mS
V <sub>P</sub>	Pinch-off Voltage	-1.5	-0.5	V
BVGS	Breakdown Voltage Gate-Source	-30	-13	V
BVGD	Breakdown Voltage Gate-Drain	-30	-13	V

TABLE III  
AUTOPROBE FET PARAMETER MEASUREMENT CONDITONS

FET Parameters	Test Conditions
G <sub>m</sub> : Transconductance; $\frac{(I_{DSS} - I_{DS1})}{V_{G1}}$	For all material types, V <sub>DS</sub> is swept between 0.5 V and VDSP in search of the maximum value of I <sub>ds</sub> . This maximum I <sub>DS</sub> is recorded as IDS1. For Intermediate and Power material, IDS1 is measured at V <sub>GS</sub> = V <sub>G1</sub> = -0.5 V. For Low Noise, HFET and pHEMT material, V <sub>GS</sub> = V <sub>G1</sub> = -0.25 V. For LNBECOLC, use V <sub>GS</sub> = V <sub>G1</sub> = -0.10 V.
V <sub>P</sub> : Pinch-Off Voltage; V <sub>GS</sub> for I <sub>DS</sub> = 0.5 mA/mm of gate width.	V <sub>DS</sub> fixed at 2.0 V, V <sub>GS</sub> is swept to bring I <sub>DS</sub> to 0.5 mA/mm.
V <sub>BVGD</sub> : Breakdown Voltage, Gate-to-Drain; gate-to-drain breakdown current (I <sub>BD</sub> ) = 1.0 mA/mm of gate width.	Drain fixed at ground, source not connected (floating), 1.0 mA/mm forced into gate, gate-to-drain voltage (V <sub>GD</sub> ) measured is V <sub>BDGD</sub> and recorded as BVGD; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
V <sub>BVGS</sub> : Breakdown Voltage, Gate-to-Source; gate-to-source breakdown current (I <sub>BS</sub> ) = 1.0 mA/mm of gate width.	Source fixed at ground, drain not connected (floating), 1.0 mA/mm forced into gate, gate-to-source voltage (V <sub>GS</sub> ) measured is V <sub>BDGS</sub> and recorded as BVGS; this cannot be measured if there are other DC connections between gate-drain, gate-source or drain-source.
I <sub>MAX</sub> : Maximum I <sub>DS</sub> .	Positive voltage is applied to the gate to saturate the device. V <sub>DS</sub> is stepped between 0.5 V up to a maximum of 3.5 V, searching for the maximum value of I <sub>DS</sub> .

TABLE IV  
RF WAFER CHARACTERIZATION TEST\*  
( $T_A = 25^\circ\text{C} \pm 5^\circ\text{C}$ )  
( $V_d = 8\text{V}$ ,  $I_d = 1.2\text{A} \pm 5\%$ )

Parameter	Test Condition	Limit			Units
		Min	Nom	Max	
Small-signal Power Gain	F = 6 to 17 GHz F = 18 GHz	20 18	24	-	dB
Input Return Loss	F = 6 to 18 GHz		6		dB
Output Return Loss	F = 6 to 18 GHz		8		dB
Output Power @ 2dB gain compression	F = 6 to 8 GHz F = 9 to 18 GHz	32 32.5	34.5	- -	dBm
Power Added Efficiency	F = 6 to 18 GHz	12	25	-	%

Note: RF probe data taken at 1 GHz steps

\* This information is based on the per-channel device.

TABLE V  
THERMAL INFORMATION\*

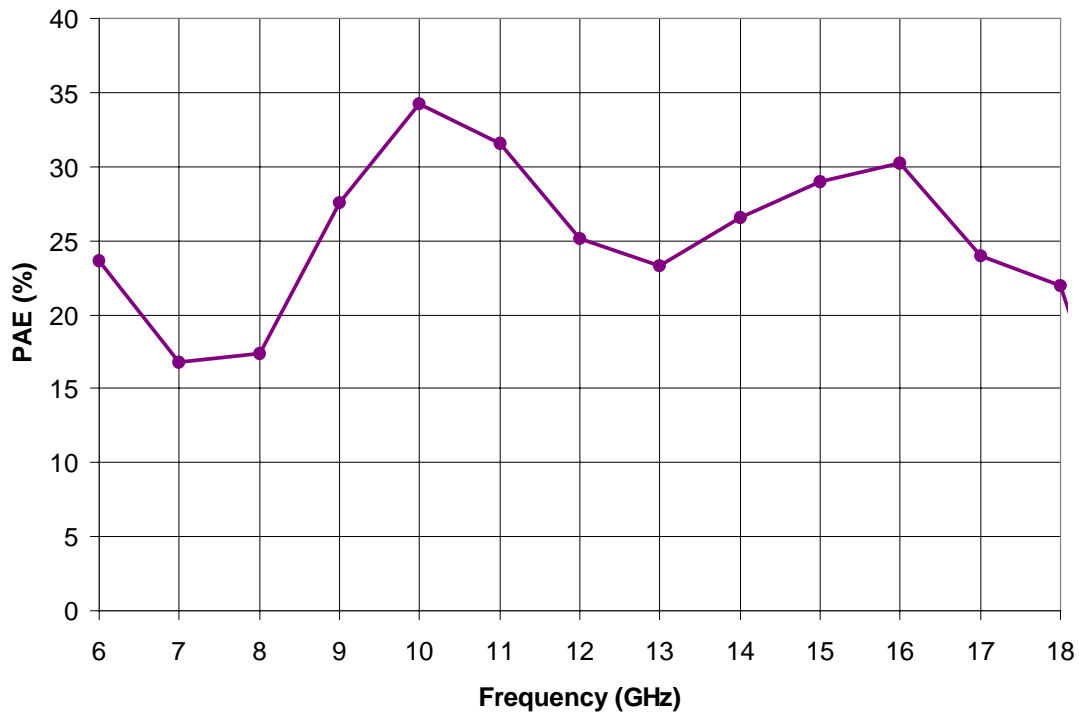
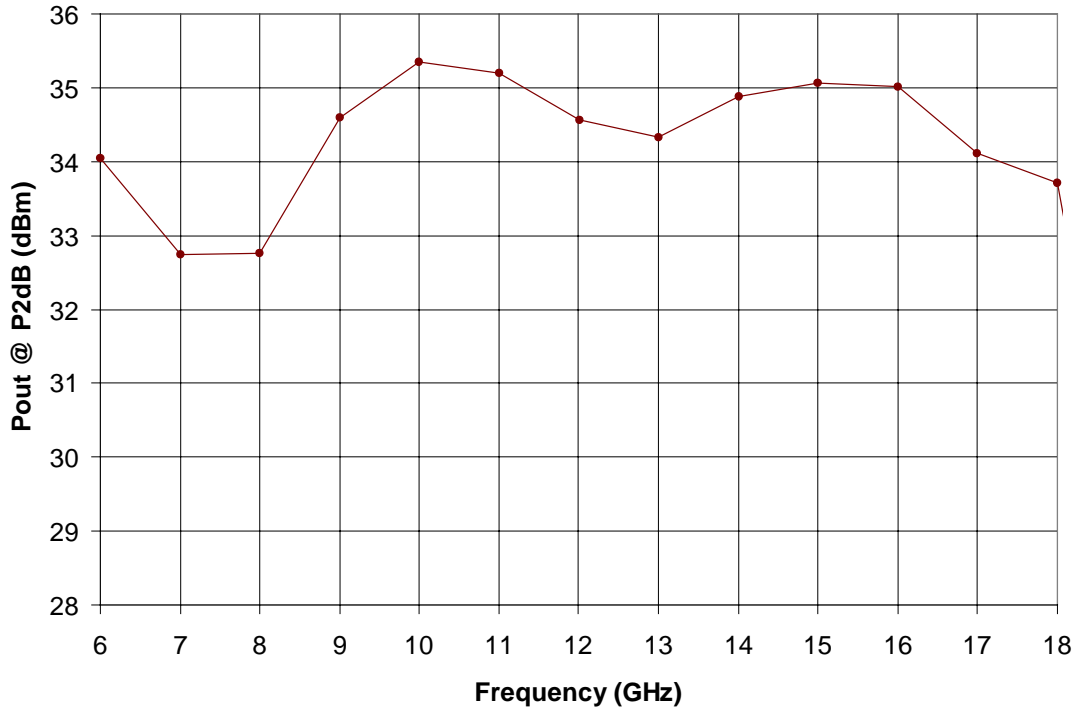
Parameter	Test Conditions	$T_{CH}$ (°C)	$R_{\theta JC}$ (°C/W)	$T_M$ (HRS)
$R_{\theta JC}$ Thermal Resistance (channel to backside of carrier)	$V_d = 8\text{V}$ $I_D = 2.4\text{A}$ $P_{diss} = 19.2\text{W}$	144.56	3.88	1.6 E+6

Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated.

\* This information is a result of a thermal model analysis based on the entire two-channel device.

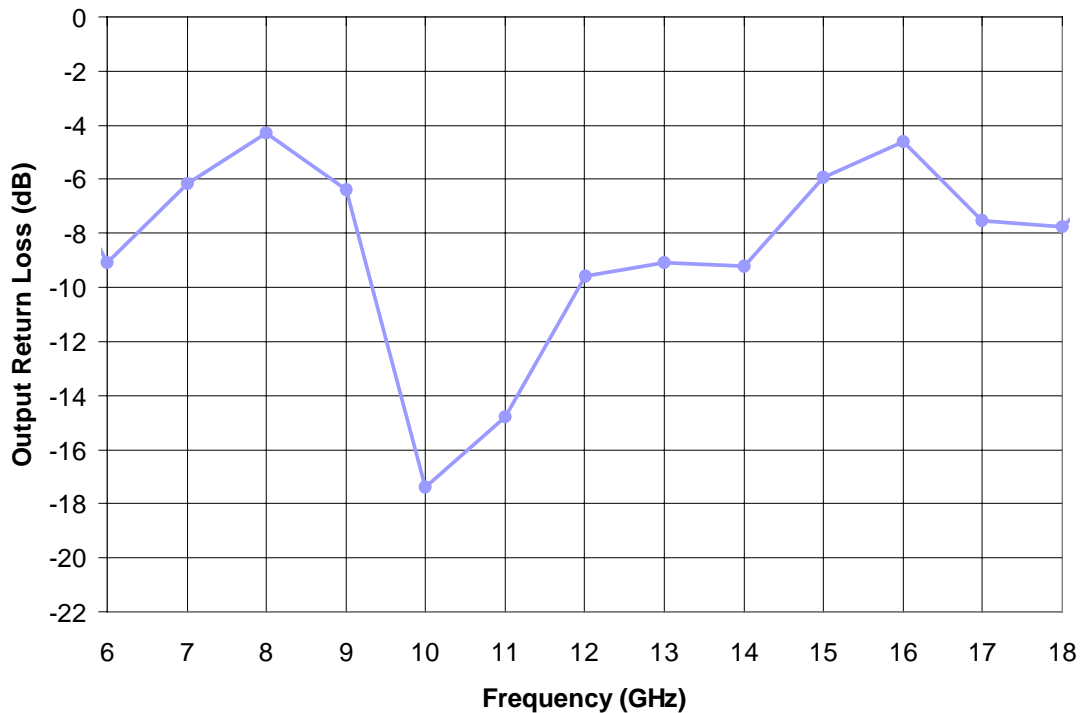
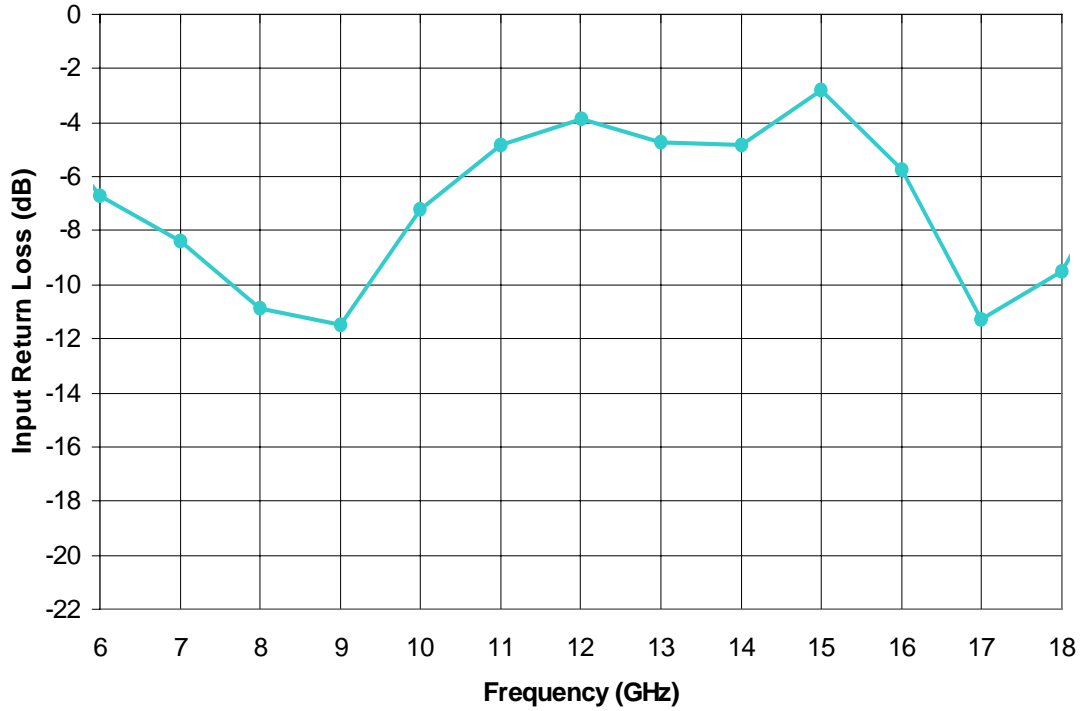
**Data Based on the 50th Percentile On-Wafer RF  
Probe Test Results, Sample Size = 3370 Devices**

**Bias Conditions:  $V_d = 8\text{ V}$ ,  $I_d = 1.2\text{ A}$**



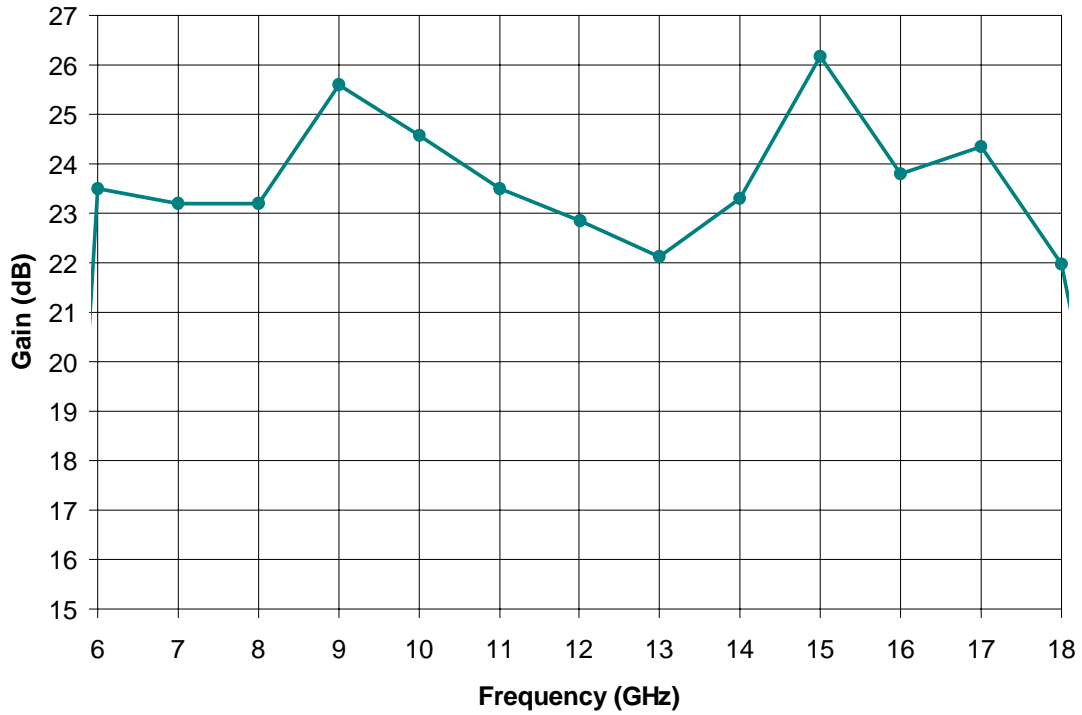
**Data Based on the 50th Percentile On-Wafer RF  
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**Bias Conditions:  $V_d = 8\text{ V}$ ,  $I_d = 1.2\text{ A}$**

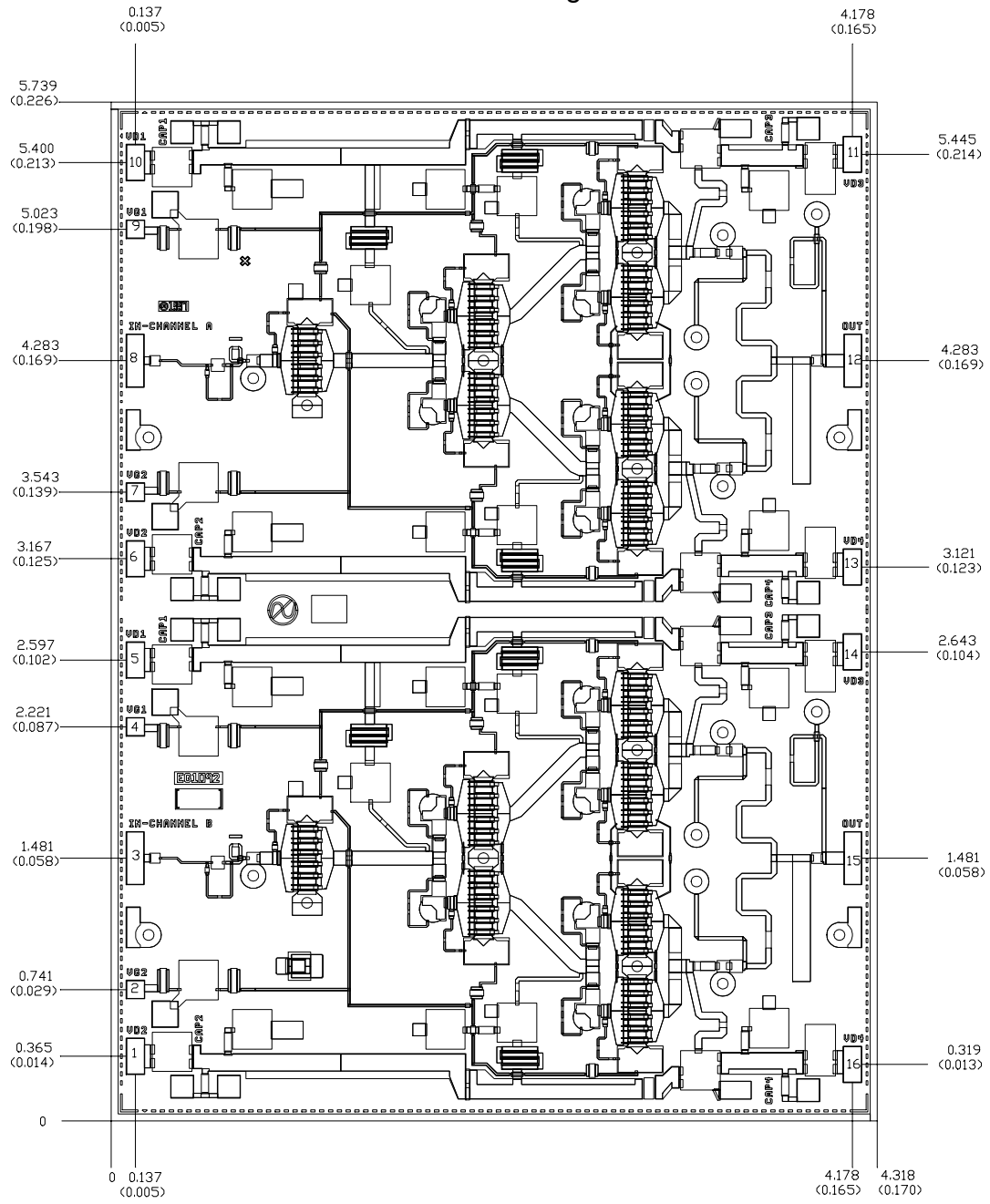


**Data Based on the 50th Percentile On-Wafer RF  
Probe Test Results, Sample Size = 3370 Devices**

**Bias Conditions:  $V_d = 8\text{ V}$ ,  $I_d = 1.2\text{ A}$**



**Mechanical Drawing**

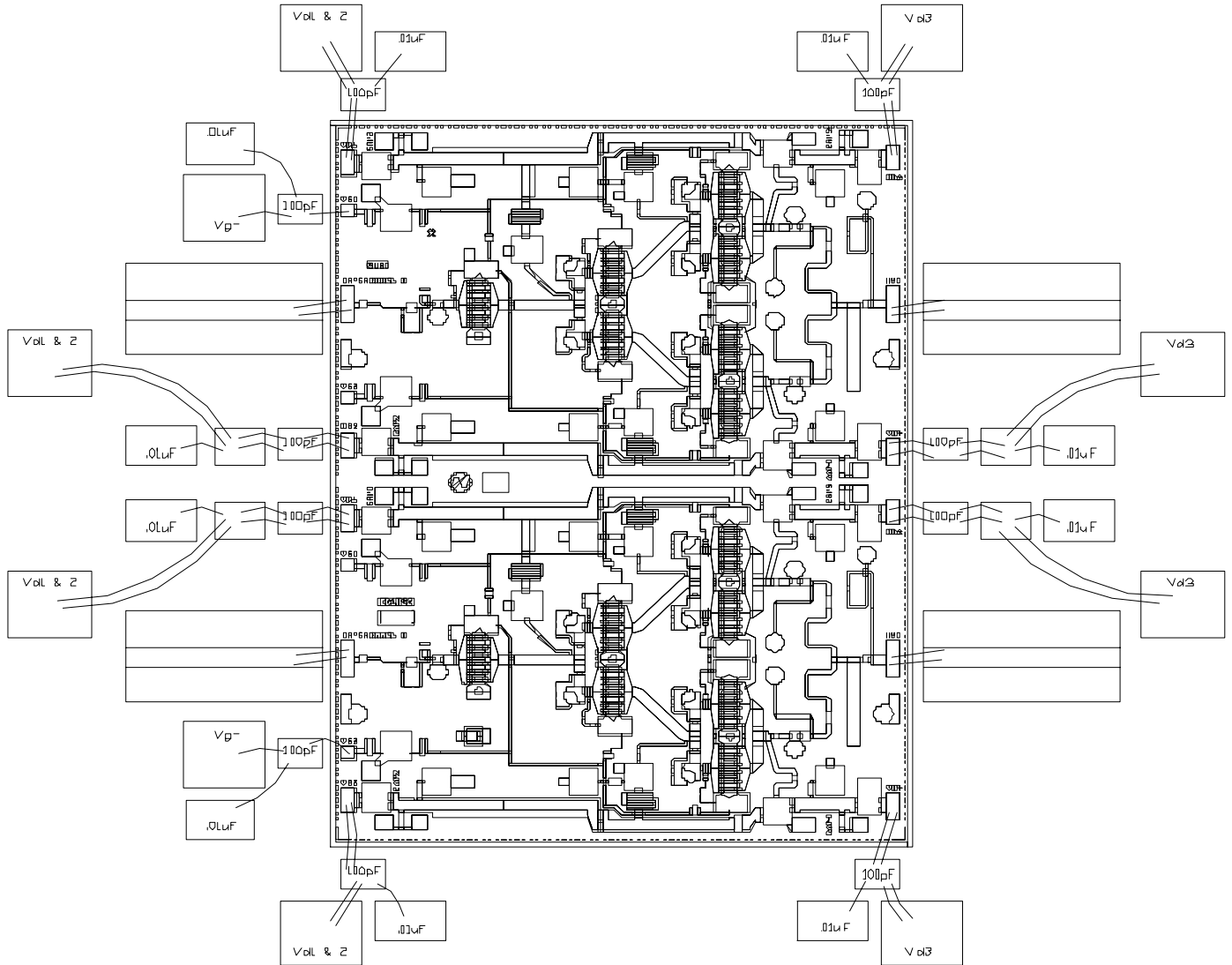


Units: millimeters (inches)  
 Thickness: 0.1016 (0.004) (reference only)  
 Chip edge to bond pad dimensions are shown to center of Bond pads.  
 Chip size tolerance: +/- 0.0508 (0.002)

Bond Pad #1,5,6,10 (Vd1&Vd2)	0.100 x 0.200	<0.004 x 0.008)
Bond Pad #11,13,14,16 (Vd3)	0.100 x 0.200	<0.004 x 0.008)
Bond Pad #2,4,7,9 (Vg)	0.100 x 0.100	<0.004 x 0.004)
Bond Pad #3,8 (RF Input)	0.100 x 0.300	<0.004 x 0.012)
Bond Pad #12,15 (RF Output)	0.100 x 0.300	<0.004 x 0.012)



Chip Assembly and Bonding Diagram



Note: All Vd's may be connected external to the MMIC.

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

## **Assembly Process Notes**

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300°C.
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire.
- Maximum stage temperature is 200°C.

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***