



# A23L3616/A23L36161 Series

**Preliminary**

**8M X 16 / 16M X 8 BIT CMOS MASK ROM**

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## **Document Title**

**8M X 16 / 16M X 8 BIT CMOS MASK ROM**

## **Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
0.0	Initial issue	November 3, 2003	Preliminary
0.1	Add A23L36161 (flash type)	August 27, 2004	
0.2	Modify A23L36161V pin configuration: pin 1 from A22 to A16 pin 48 from A16 to A22	November 24, 2004	



# A23L3616/A23L36161 Series

**Preliminary**

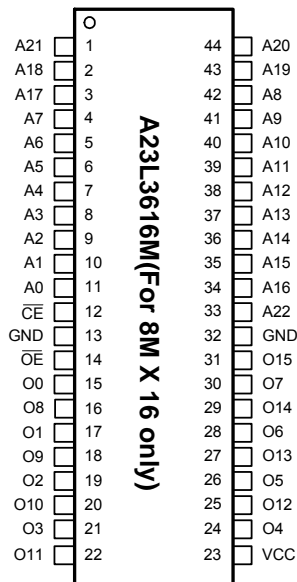
**8M X 16 / 16M X 8 BIT CMOS MASK ROM**

## Features

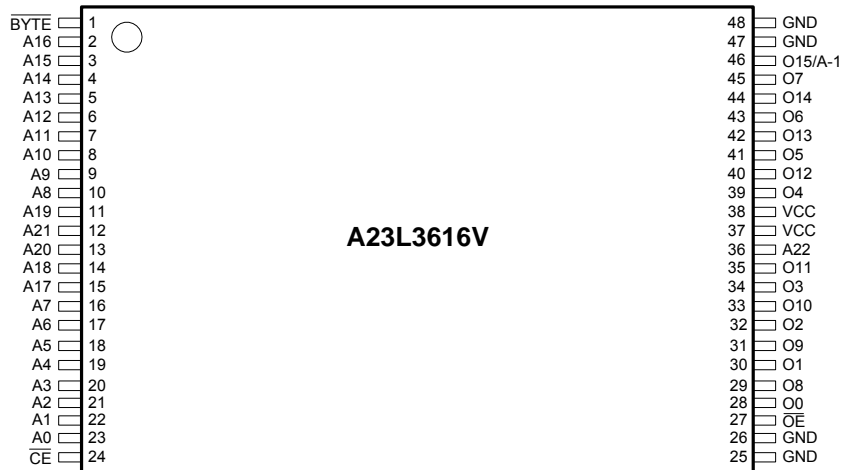
- 8M x 16 bit or 16M x 8 bit organization
- Supply voltage range: 2.7V~3.6V
- Access time: 100ns (max.)/3.0V~3.6V  
120ns (max.)/2.7V~3.6V
- Current: Operating: 40mA (typ.)/3.3V  
Standby: 10μA (typ.)/3.3V
- Three-state outputs for wired-OR expansion
- Full static operation
- All inputs and outputs are directly TTL-compatible
- Available in 44-pin SOP, 48-pin TSOP (forward, reverse type and flash memory's pinouts compatible)
- Pinout compatible with flash type (A23L36161)

## Pin Configurations

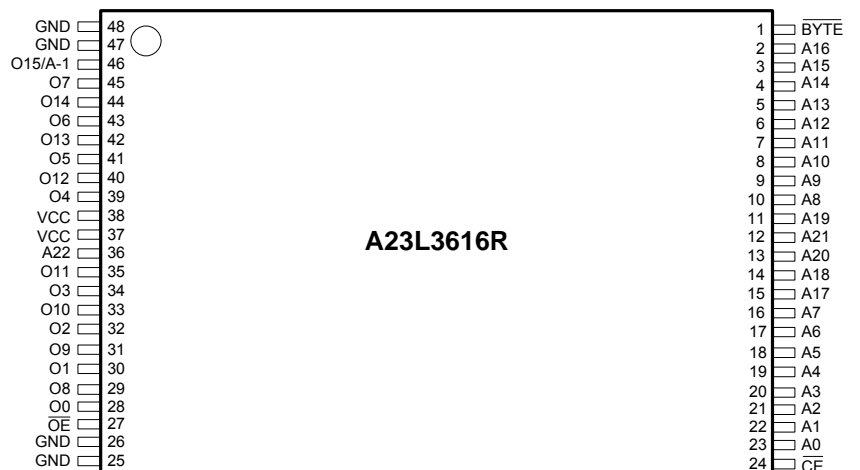
### ■ SOP

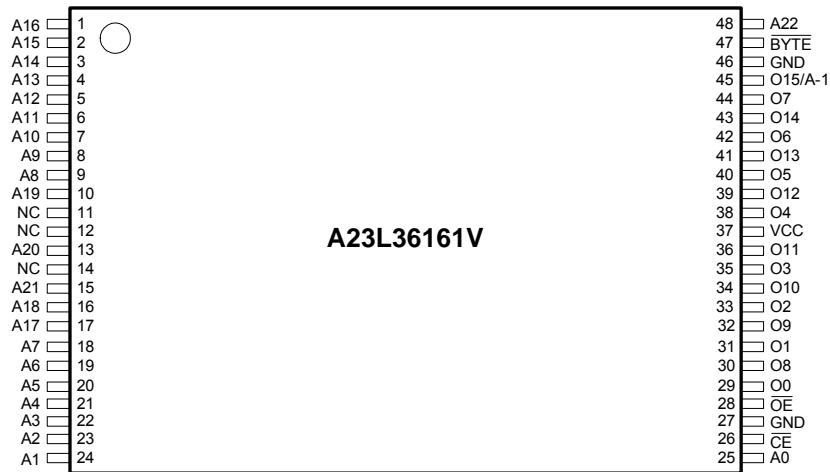
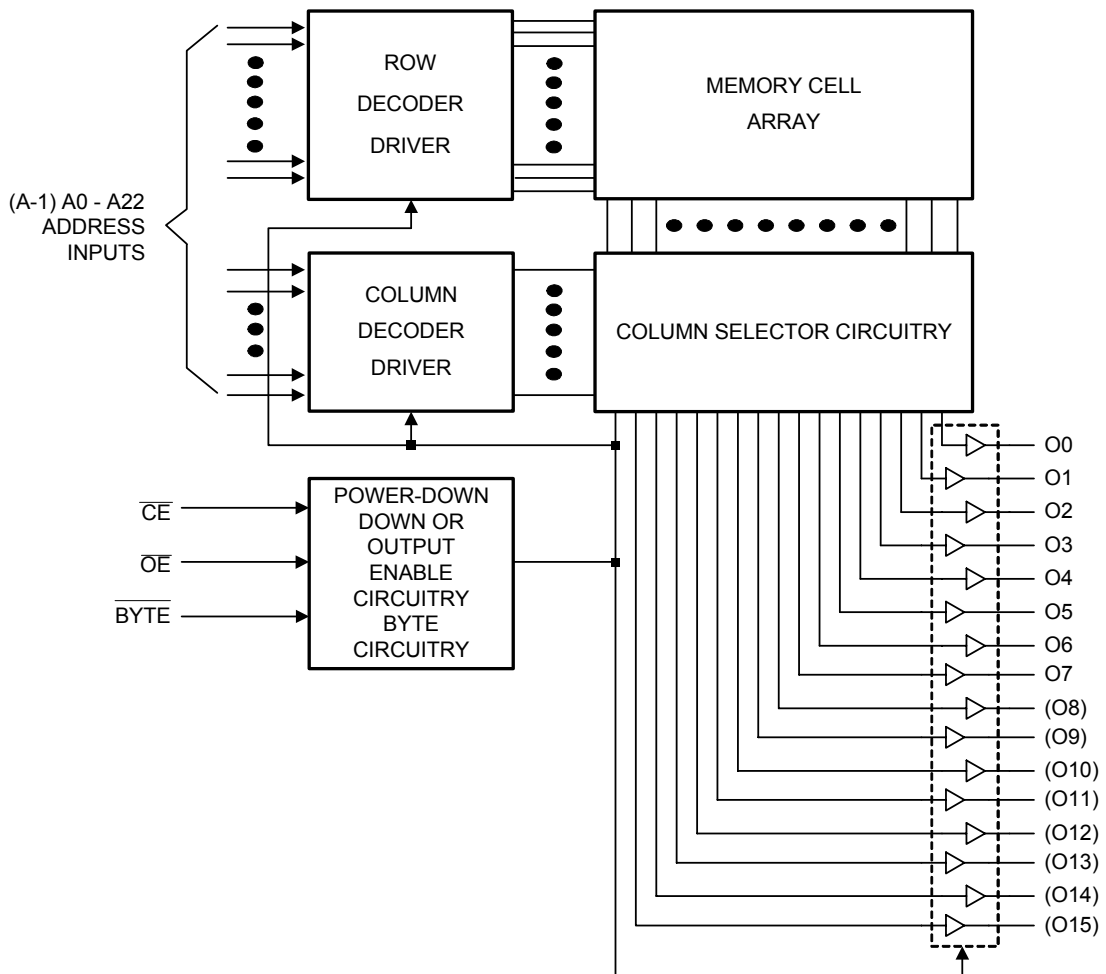


### ■ TSOP (forward type)



### ■ TSOP (reverse type)



**Pin Configurations (continued)**
**■ TSOP (forward type)**

**Block Diagram**


**Pin Descriptions**

Pin No.			Symbol	Description
44L SOP (A23L3616) (16M X 8 only)	48L TSOP (A23L3616)	48L TSOP (A23L36161)		
1-11, 33-44	2-23, 36	1-10, 13, 15-25, 48	A0-A22	Address Inputs
15-22, 24-30	28-35, 39-45	29-36, 38-44	O0-O14	Data Outputs
31	46	45	O15/A-1	Output 15(WORD mode) /LSB Address (BYTE mode)
12	24	26	$\overline{CE}$	Chip Enable Input
14	27	28	$\overline{OE}$	Output Enable Input
No	1	47	$\overline{BYTE}$	BYTE or WORD mode Selection
23	37-38	37	VCC	Power Supply
13, 32	25-26, 47-48	27, 46	GND	Ground
		11-12, 14	NC	No Connection

**Recommended DC Operating Conditions**

 (T<sub>A</sub> = 0°C to + 70°C)

Symbol	Parameter	Min.	Max.	Unit
VCC	Supply Voltage	2.7	3.6	V
GND	Ground	0	0	V
V <sub>IH</sub>	Input High Voltage	2.2	VCC+0.3	V
V <sub>IL</sub>	Input Low Voltage	- 0.3	0.6	V

**Absolute Maximum Ratings\***

Ambient Operating Temperature . . . . . 0°C to + 70°C  
 Storage Temperature . . . . . -65°C to + 125°C  
 Output Voltage . . . . . -0.5V to VCC + 0.5V  
 Input Voltage . . . . . -0.5V to VCC + 0.5V

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

**DC Electrical Characteristics**

(T<sub>A</sub> = 0°C to + 70°C, VCC = 2.7V~3.6V, GND = 0V for -100, VCC = 3.0V~3.6V, GND = 0 for -70)

Symbol	Parameter	Min.	Max.	Unit	Conditions	Note
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -0.4mA (3V)	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 1.6mA (3V)	
V <sub>IH</sub>	Input High Voltage	2.2	VCC + 0.3	V		
V <sub>IL</sub>	Input Low Voltage	-0.3	0.6	V		
I <sub>LI</sub>	Input Leakage Current		+10	μA	VCC = max. V <sub>IN</sub> = VCC to GND	
I <sub>LO</sub>	Output Leakage Current		+10	μA	VCC = max. V <sub>OUT</sub> = VCC to GND	1
I <sub>CC</sub>	Operating Supply Current		60	mA	t <sub>CYC</sub> = min.	2
I <sub>SB</sub>	Standby Supply Current (TTL)		1.5	mA	$\overline{CE} = V_{IH}$	
I <sub>SB1</sub>	Standby Supply Current (CMOS)		30	μA	$\overline{CE} \geq VCC - 0.2V$	

**Capacitance**

Symbol	Parameter	Min.	Max.	Unit	Test Conditions	Note
C <sub>i</sub>	Input Capacitance		10	pF	T <sub>A</sub> = 25°C f = 1.0MHz	3
C <sub>o</sub>	Output Capacitance		10	pF		

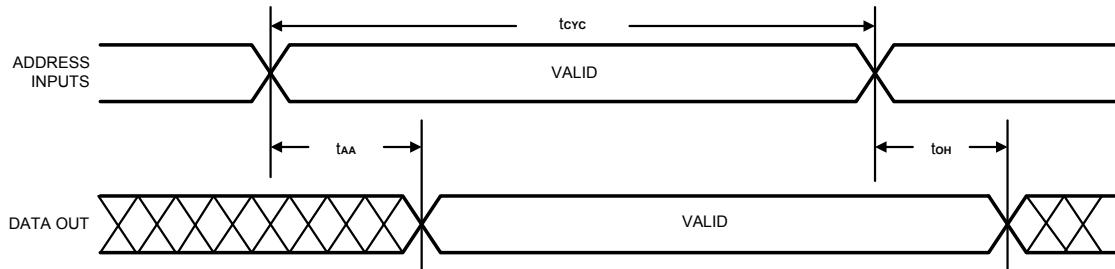
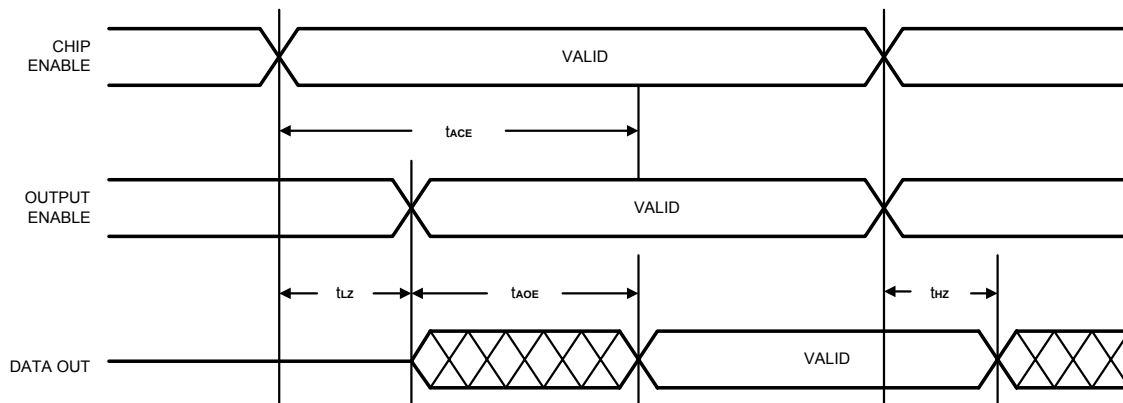
**AC Characteristics** (T<sub>A</sub> = 0°C to +70°C, VCC = 2.7V~3.6V for -120, VCC = 3.0V~3.6V for -100, GND = 0V)

Symbol	Parameter	A23L3616/ A23L36161 -100		A23L3616/ A23L36161 -120		Unit	Note
		Min.	Max.	Min.	Max.		
t <sub>cyC</sub>	Cycle Time	100		120		ns	
t <sub>AA</sub>	Address Access Time		100		120	ns	
t <sub>ACE</sub>	Chip Enable Access Time		100		120	ns	
t <sub>AOE</sub>	Output Enable Access Time		30		50	ns	
t <sub>oH</sub>	Output Hold after Address Change	0		0		ns	
t <sub>LZ</sub>	Output Low Z Delay	0		0		ns	4, 6
t <sub>Hz</sub>	Output High Z Delay*		20		20	ns	5, 6

\* t<sub>Hz</sub> is specified from either  $\overline{OE}$  or  $\overline{CE}$  going disabled, whichever occurs first.

**Notes:**

1.  $\overline{OE} / \overline{CE} = V_{IH}$  (Output is unloaded)
2.  $V_{IN} = V_{IH}/V_{IL}$ ,  $\overline{OE} / \overline{CE} = V_{IL}$  (Output is unloaded)
3. This parameter is periodically sampled and is not 100% tested. All pins, except pins under test, are tied to AC ground.
4. Output LOW impedance delay (t<sub>LZ</sub>) is measured from  $\overline{CE}$  or  $\overline{OE}$  going active.
5. Output HIGH impedance delay (t<sub>Hz</sub>) is measured from  $\overline{CE}$  or  $\overline{OE}$  going inactive.
6. This parameter is sampled and not 100% tested.

**Timing Waveforms**
**Propagation Delay from Address ( $\overline{CE}$  = Active,  $\overline{OE}$  = Active)**

**Propagation Delay from Chip Enable or Output Enable (Address Valid)**

**AC Test Conditions**

Part No.	A23L3616/ A23L36161 -100	A23L3616/ A23L36161 -120
Applied Voltage	3.0V~3.6V	2.7V~3.6V
Input Pulse Levels	0.4V to 2.4V	0.4V to 2.4V
Input Rise and Fall Time	10 ns	10 ns
Timing Measurement Reference Level	$V_{IN} = 1.4V, V_{OUT} = 1.4V$	$V_{IN} = 1.4V, V_{OUT} = 1.4V$
Output Load	1 TTL gate and $C_L = 100pF$	1 TTL gate and $C_L = 100pF$

**Function Table**

$\overline{CE}$	$\overline{OE/NC}$	$\overline{BYTE}$	O15/A-1	O0 - O7	O8 - O15	Mode
L	L	H	Data Pin O15	Data Out	Data out	Word
L	L	L	LSB Address A-1	Data Out	Hi - Z	Byte
H	X	X	X	Hi - Z	Hi - Z	Power-down
L	H	X	X	Hi - Z	Hi - Z	Output Disable

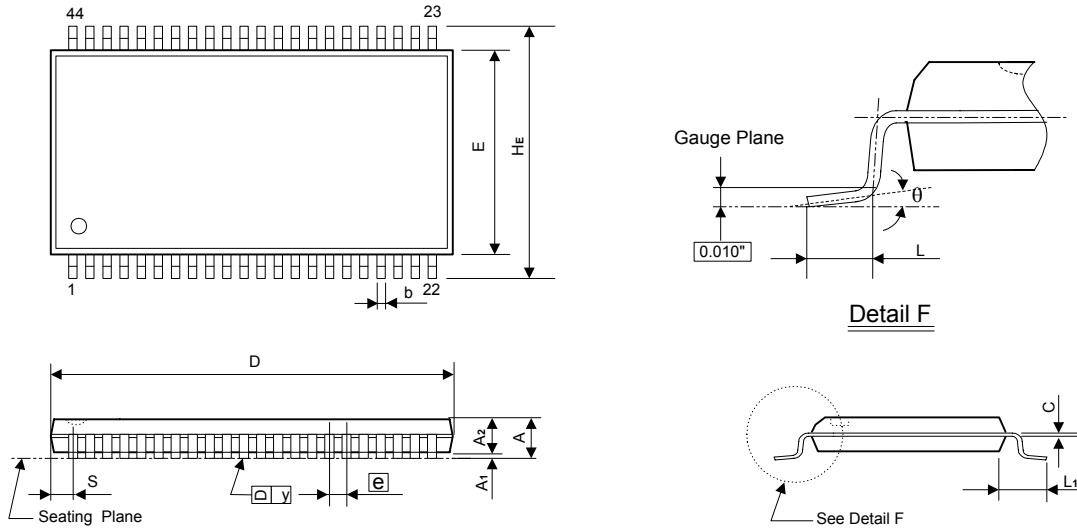
**Ordering Information**

Part No.	Access Time (ns)	Package
A23L3616M-100 (16M X 8 only)	100	44L SOP
A23L3616M-120 (16M X 8 only)	120	44L SOP
A23L3616V-100	100	48L TSOP (Forward)
A23L3616V-120	120	48L TSOP (Forward)
A23L3616R-100	100	48L TSOP (Reverse)
A23L3616R-120	120	48L TSOP (Reverse)
A23L36161V-100	100	48L TSOP (Flash Compatible)
A23L36161V-120	120	48L TSOP (Flash Compatible)



**Package Information**
**SOP 44L Outline Dimensions**

unit: inches/mm



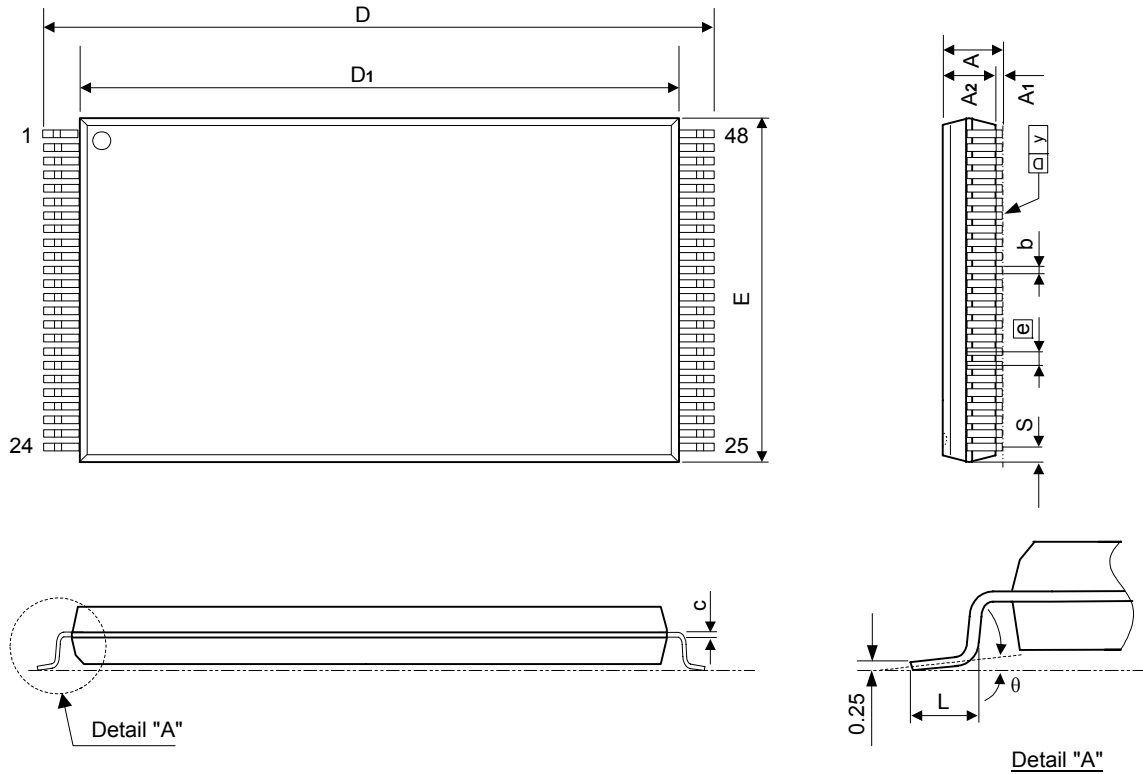
Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.118	-	-	3.00
A1	0.004	-	-	0.10	-	-
A2	0.103	0.106	0.109	2.62	2.69	2.77
b	0.013	0.016	0.020	0.33	0.40	0.50
C	0.007	0.008	0.010	0.18	0.20	0.25
D	-	1.122	1.130	-	28.50	28.70
E	0.490	0.496	0.500	12.45	12.60	12.70
e	-	0.050	-	-	1.27	-
HE	0.620	0.631	0.643	15.75	16.03	16.33
L	0.024	0.032	0.040	0.61	0.80	1.02
L1	-	0.0675	-	-	1.71	-
S	-	-	0.045	-	-	1.14
y	-	-	0.004	-	-	0.10
θ	0°	-	8°	0°	-	8°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.

**Package Information**
**TSOP 48L (Type I) Outline Dimensions**

unit: inches/mm



Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.042	0.94	1.00	1.06
b	0.007	0.009	0.011	0.18	0.22	0.27
c	0.004	-	0.008	0.12	-	0.20
D	0.779	0.787	0.795	19.80	20.00	20.20
D1	0.720	0.724	0.728	18.30	18.40	18.50
E	-	0.472	0.476	-	12.00	12.10
e	0.020 BASIC			0.50 BASIC		
L	0.016	0.020	0.024	0.40	0.50	0.60
S	0.011 Typ.			0.28 Typ.		
y	-	-	0.004	-	-	0.10
theta	0°	-	8°	0°	-	8°

**Notes:**

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension S includes end flash.