ADVANCED

Product Specification

AHA4011

10 MBytes/sec Reed-Solomon Error Correction Device

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PS4011-0793

1.0 INTRODUCTION

The AHA4011 is a single chip integrated circuit that implements a high speed Reed-Solomon Forward Error Correction algorithm conforming to the Intelsat IESS/308 Rev. 6B specification. The device can be operated in two different modes, burst or continuous. Burst mode allows up to 40 MBytes/sec and continuous mode supports up to 10 MBytes/sec data transfers.

The device supports several programmable parameters, including, block size, error threshold, number of check bytes, order of output, and mode of operations. The data input port is used to initialize the programmable parameters and the two-256 byte FIFOs are used to buffer the input and output data. Discontinuities in data flow may be controlled by dedicated control pins.

High operating frequency, input and output data rate flexibility, low processing latency, and various programmable parameters make this device ideal for many applications including: DTV, DBS, ADSL, Satellite Communications, ISDN, High Performance Modems, and networks.

The AHA4011 is a member of the AHA PerFEC™ family of high speed forward error correction (FEC) devices. FEC devices supporting other polynomials, speed, packaging, and testing options are also available from Advanced Hardware Architectures.

This specification provides full electrical and mechanical information to help a system engineer develop a system using AHA4011. This document contains descriptions on correction terms, pinout, functions and features, DC and AC characteristics, package and mechanical specification, ordering information, and Related Technical Publications. Software simulation of the RS code as implemented in the device is also available. Please contact AHA or its authorized sales representatives worldwide for copies of Related Technical Publications and software simulation of the RS code.

1.1 FEATURES

HIGH PERFORMANCE

- Complies to Intelsat IESS-308, Revision 6B and proposed ITU-TS SG-18 (Formerly CCITT SG-18) Standards
- 40 MBytes/sec burst transfer rate with a 40 MHz clock for all block lengths
- Maximum data transfer rates of 10.0 MBytes/sec continuous for block lengths from 54 bytes through 177 bytes using a 40 MHz clock
- Processing latency time less than 10 µsec in continuous modes for block lengths of 100 bytes

FLEXIBILITY

- Programmable to correct from 1 to 10 error bytes or 20 erasure bytes per block
- Block lengths programmable from 3 to 255 bytes
- Operates in encode, decode or pass-through modes
- Outputs corrected data or correction vectors in forward or reverse order
- Continuous or burst mode operation

SYSTEM INTERFACE

- Simple system interface and internal FIFO's eliminate external microprocessor and buffers
- Dedicated control pins permit discontinuities in system data flow

OTHERS

- Low power 350mW max power dissipation
- 44 pin PLCC; 50 mil lead pitch
- Higher speed, packaging, and testing options available
- Software emulation of the algorithm available

1.2 CONVENTIONS, NOTATIONS, AND DEFINITIONS

– Certain signals are logically true at a voltage defined as "low" in the data sheet. All such signals will have an "N" appended to the end of the signal name. For example, RSTN and DSON.
– "Signal assertion" means the output signal is logically true.

– Hex values are defined with a prefix of "0x", such as "0x10".
– A range of signal names is denoted by a set of colons between the numbers. Most significant bit is always shown first, followed by least significant bit. For example, DI[7:0] represents Data Input Bus 7 through 0.
– A product of two variables is expressed with an "x", for example, N x C_i represents Codeword Length multiplied by Input clocks/byte.
– Mega Bytes per second is referred to as MBytes/sec or MB/sec.

1.2.1 DEFINITION OF CORRECTION TERMS

TERM	*NAME (other references)*	*DEFINITION*	*RANGE (number of bytes)*
K	Message Length (user data or message bytes)	Number of user data symbols in one message block. Size of a symbol in AHA4011 is 8-bits. Message length is K = N - R.	1 through 253 (1, 2, 3, 4 . . . 253)
R	Check symbols (parity or redundancy)	Symbols appended to the user data to detect and correct errors. The number of check symbols required in a system is R ≥ E + 2e.*	2 through 20 in increments of 1 (2, 3, 4 . . . 20)
N	Codeword Length (Block length)	Sum of message and check symbols. N = K + R.	3 through 255 (3, 4, 5, 6 . . . 255)
t	Error Corrections	Maximum number of error corrections performed by the device. The value is t = Integer (N - K/2).	1 through 10 (1, 2, 3 . . . 10)
P	Error Threshold	The threshold limit to determine uncorrectability of a Codeword and the number of check bytes allocated for correction-only purposes (not for detection).	2 through 20 (2, 3, 4 . . . 20)
e	Number of Errors	An error is defined as an erroneous byte whose correct value and position within the message block are both unknown.	0 through N
E	Number of Erasures	An erasure is defined as an error whose position is known within the message block.**	0 through N
G	Burden of Correction	A measure of the burden of correction being placed on the capabilities of the device for that message block. The value G = 2e + E.	0 through R

* For every 2 check bytes, the AHA4011 can correct either 2 erasures or 1 error.
** An erasure is detected by a parity detector or a signal dropout detector. The presence of an erasure is indicated by asserting the ERASE signal when the erased byte is clocked into the AHA4011.

2.0 FUNCTIONAL DESCRIPTION

This section gives an architectural overview of the chip and its many functions, features, and operating modes. The block diagram for the chip shows the Reed-Solomon ECC module, the Input and Output FIFOs, and its associated control. All input and output data are clocked on the rising edge of CLK.

2.1 FUNCTIONAL OVERVIEW

The AHA4011 Reed-Solomon codec (coder/decoder) is a member of the AHA PerFEC™ family of high speed forward error correction (FEC) devices. This single chip, three-layer metal, CMOS device can operate as a stand alone encoder, a decoder, or a pass-through device.

Data transfers through the device can operate in two modes: continuous or burst. The system designer determines the mode by controlling the input and output rates, ie., input and output clocks/byte. Processing time or latency within the device is the same in either mode.

Continuous mode is used to maintain a constant flow of data in the system. In continuous mode, a data block is loaded into the Input FIFO and processed through the ECC core, while the previously processed block is unloaded from the Output FIFO simultaneously. After an initial latency, continuous data stream is maintained through the device. Clock cycles required between adjacent input bytes is a function of the block length. The proper device clock rate is required to achieve continuous operation.

Burst mode is used where the system requires high data rate and the system can tolerate discontinuities in input or output data. Burst mode offers higher average rates for higher block lengths. In burst mode, an entire block is loaded into the Input FIFO at data rates up to 40 MBytes/sec while the output signal RDYIN is asserted. When the Input FIFO is completely loaded, RDYIN signal is deasserted. Each block is processed within the ECC core and calculations are made. The entire block is processed through the ECC core, and transferred into the Output FIFO. The device asserts RDYON signal and holds active until the entire block is strobed out of the device.

The ECC core loads the Output FIFO in reverse order for either mode. Data may be strobed out of the device in forward or reverse order. If forward order is desired, output data cannot be strobed out of the device until the entire block has been loaded into the Output FIFO.

The delay required for each block of a given length to pass through the device is fixed, and does not vary with the location or the number of errors received. This delay (or latency), expressed in the number of clocks, is $(N-1) \times C_i + R + 60 + N \times (C_i / C_i - 1)$, where N is the block length, R is the number of check bytes per block, and C_i is clocks per input byte.

In its most powerful mode, where incorrect bytes are flagged by external circuitry, referred to as erasures, the AHA4011 can correct as many as R bytes in error in a message block as long as 255 bytes, where R equals the number of check bytes added to the message block by the Reed-Solomon encoder. If no external error detection is available, the AHA4011 can detect and correct up to t bytes in error, in a block as long as 255 bytes.

The Reed-Solomon codes used by the AHA4011 and by other members of the AHA PerFEC™ family, are among the most powerful binary EDAC (Error Detection and Correction) codes known. Compared with other codes, RS codes require relatively few "overhead" check bytes to be added to the data stream to achieve a high degree of error detection and correction. Since the AHA4011 deals with bytes (or symbols) rather than with individual bits, when a byte is in error it does not matter how many bits within the byte are corrupted; it is counted as one error.

The Reed-Solomon code is defined over the finite field $GF(2^8)$. The field defining primitive polynomial is $P(x) = x^8 + x^7 + x^2 + x + 1$ and the generator polynomial, dependent on the variable R, is given by:

$$G(x) = \prod_{i=120}^{119+R} (x-\alpha^i)$$

where $R \in \{2, 3, 4, 5,...20\}$ for the AHA4011. This polynomial is specified in international standards, Intelsat IESS 308 (Rev 6B) and the proposed CCITT SG-18.

For every 2 check bytes, the decoder can correct either 2 erasures or 1 error. An erasure is an error with a known location. This could be determined with a parity detector or a signal dropout detector, for example. An erasure is indicated by the ERASE signal when the erased byte is clocked in the device. Errors are defined as erroneous bytes whose locations are unknown, ie., there was no corresponding ERASE input for these bytes.

Correcting "erasures" takes only half as much of the correction capability of the RS code as it takes to correct "errors", since the position information is already known for "erasures". The correction ability of the code is bounded as:

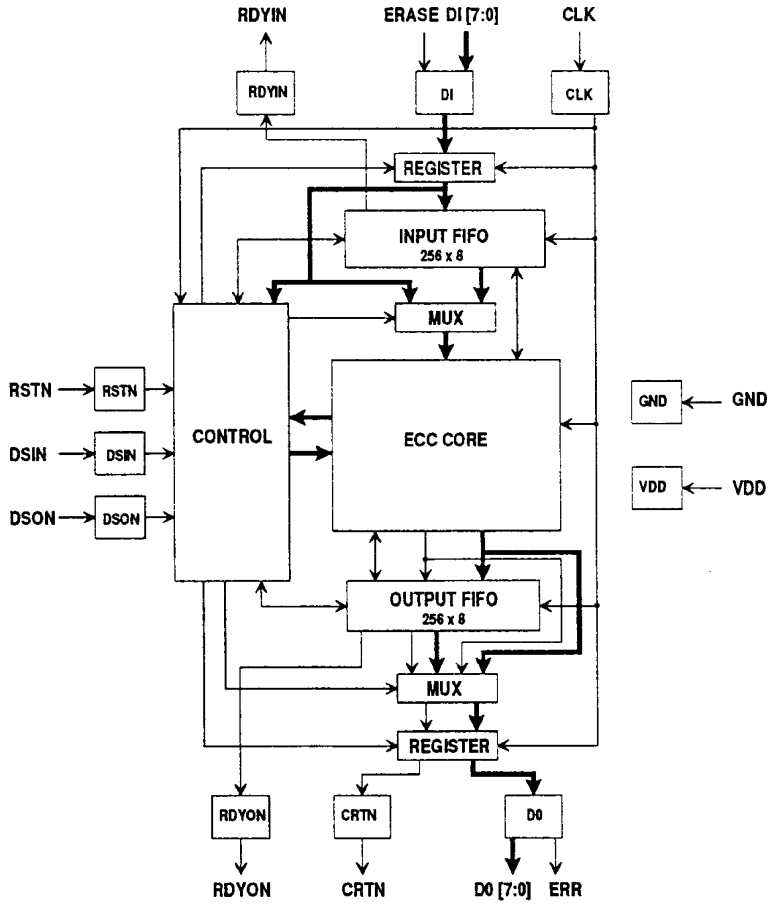
$R \geq$ # erasures + 2(# errors)

Valid block length (N) is defined by the relationship:

$R + 1 \leq N \leq 255$, where R ranges from 2 to 20.

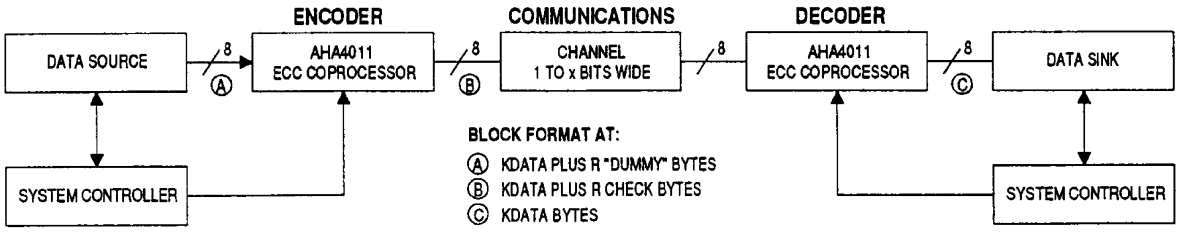
A complete message block can therefore range from a minimum of 1 byte to a maximum of 253 bytes.

Figure 1: Block Diagram



A typical system block diagram is shown in the following figure.

Figure 2: Typical Applications Diagram



2.2 SIGNAL DESCRIPTIONS

DI[7:0] **Data Input Bus.** The input byte is latched on the rising edge of the clock when both **DSIN** and **RDYIN** are active. If either **DSIN** or **RDYIN** are inactive, the byte on **DI** is ignored.

DSIN **Data Input Strobe.** Enables data from **DI** to be loaded into the chip. When **RDYIN** is active, **DSIN** being active on the rising edge of the clock loads the input data in the device. **DSIN** is ignored if **RDYIN** is inactive. Signal is active low.

RDYIN **Ready Input.** Indicates the chip's ability to accept data input on **DI**. If active, **DSIN** is allowed to enable the loading of input data on **DI**. When inactive, **DSIN** is ignored. Signal is active low.

DO[7:0] **Data Output.** The output byte is available on the bus. The value of the output byte is undefined if **RDYON** is inactive. Requires an acknowledge strobe, **DSON**, at a rising edge of the clock to increment internal address counter. **DO** bus is always active and is not tristated by the device.

ERASE **Erasure** input flag for symbol currently on **DI**. Signal is active high.

DSON **Data Output Strobe.** This input strobe acknowledges to the chip that data available on the Output Bus, **DO**, has been received by the system. The device uses this strobe to increment its internal address counter to the next data location. **DSON** is ignored if **RDYON** is inactive. Signal is active low.

RDYON **Ready Output.** This output pin indicates that the output data bus has valid data. If active, **DSON** is allowed to increment the internal address counter for the next data byte. When inactive **DSON** is ignored and **DO** is undefined. Signal is active low.

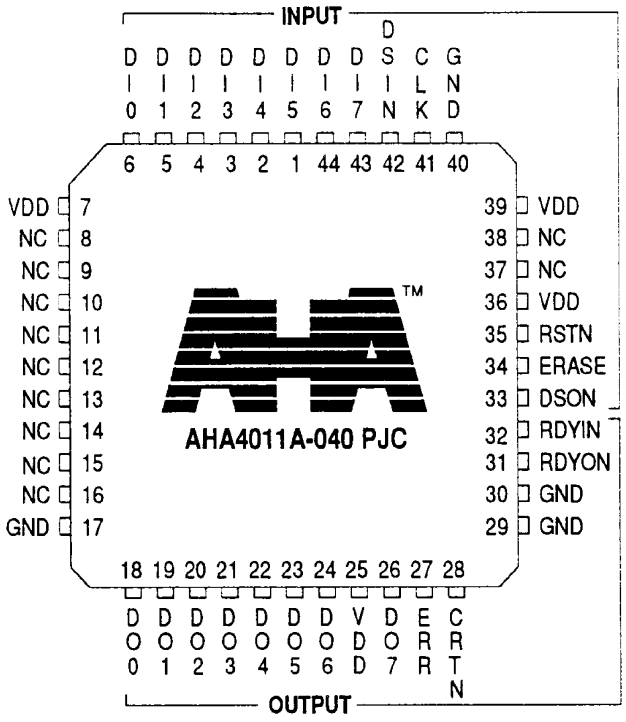
CRTN **Correctable.** The output pin when active indicates the previous block did not exceed the error threshold programmed by P. This signal is valid when the final byte of the block is strobed out of the chip. During all other times the signal is low. Signal is valid for at least one clock. Active low.

RSTN **Reset. Input pin.** When **RSTN** is active and **DSIN** is inactive, the device forces all internal control circuitry into a known state and initializes all data path elements. **RSTN** is also active during Initialization Phase. In this phase chip parameters can be programmed by using **DI** and **DSIN.** Signal is active low.

CLK **Clock. System clock input.** Refer to **AC CHARACTERISTICS** for clock requirements.

ERR **Error.** Output pin indicates the current value on **DO[7:0]** is an error value on a corrected byte.

2.3 PINOUT



2.4 DATA FLOW

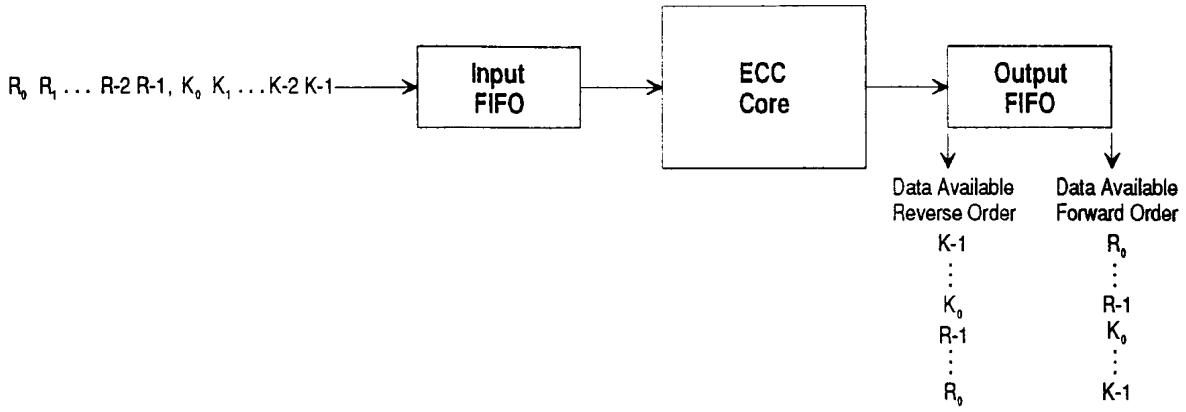
The device is first initialized for various programmable parameters including: Erasure Multiplier, Error Threshold, Number of Check bytes, Number of Message bytes per block, Block Length, and a Control byte. Following a six-byte initialization, the device may be operated in encode, decode, or pass through modes. The device requires reinitialization only when the parameters are changed.

The device processes data as "blocks" containing Message and Check Bytes. Order of the input bytes into the device must be message bytes K - 1 through message byte K_0 followed by check bytes R - 1 through check byte R_0. The device processes the block in this manner:

- a block is clocked into the Input Port FIFO;
- transferred into the ECC module;
- passed to the Output FIFO in the reverse order from what was received at the Input Port; and
- clocked out through the Output Port via the Output FIFO. Consecutive blocks may be input into the Input FIFO while the Output FIFO is being emptied.

Data is available through the Output Port in reverse or forward order. Forward order clocks out the block the same as input and reverse order clocks the check byte R_0 through check bytes R - 1 followed by message byte K_0 through message bytes K - 1.

Figure 3: Data Input and Output Order



2.5 INITIALIZATION SEQUENCE

The two sequences in resetting the device and its internal registers are "Reset" and "Initialization". The chip is first "Reset" by pulling the low RSTN signal for at least two clocks while the DSIN signal is held inactive, ie., high. Resetting the device initializes all internal control circuitry, resets the FIFOs, and clears all data path elements except the Initialization Registers.

Following this Reset, the six internal registers, referred to as "Initialization Registers" are loaded with desired values. Order for loading the bytes is numbers 1 through 6. This sequence must be used if any one register needs updating, ie., all registers must be reinitialized for a change to any one register.

The RSTN must be active low for at least two clocks before the first initialization byte is clocked in and remain active for at least one clock after the final byte. These bytes are clocked into the device similar to message bytes with the exception of RSTN which should be low instead of high. RSTN must be high for at least two clocks before the first message byte can be strobed into the device.

The chip can be reset without effecting the contents of the initialization registers at any time. This is done by pulling low RSTN for at least two clocks.

2.5.1 INITIALIZATION REGISTERS

BYTE 1, ERASURE MULTIPLIER:

[7:0] - Multiplier value that must be programmed as shown in Appendix A. The table shows a value to be programmed corresponding to the block length selected.

BYTE 2, ERROR THRESHOLD:

[4:0] - Number of errors detected before the block is called uncorrectable. Error Threshold must be less than or equal to the number of check bytes. Minimum value of 0x02 sets the Threshold to 2 and 0x14 sets to the maximum, 20.

[7:5] - Reserved. Set to 0.

BYTE 3, CHECK BYTES:

[4:0] - Number of check bytes in RS code, R. Minimum setting of 0x02 indicates two check bytes for R = 2 and 0x14 indicates the maximum of 20. In the pass-through mode, this value is a "Don't Care".

[7:6] - Reserved. Set to 0.

BYTE 4, MESSAGE BYTES:

[7:0] - Number of message bytes in code, K. Minimum setting of 0x01 indicates 1 byte, setting to 0xFD indicates the maximum 253 message bytes.

BYTE 5, BLOCK LENGTH:

[7:0] - Number of bytes in block, N. Setting to 0x03 indicates 3 bytes, setting to 0xFF indicates 255 bytes.

BYTE 6, CONTROL BYTE:

[0] - RESERVED - Reserved. Set to 0.

[1] - NOPAR - Parity Symbol Control

- 0 - Check bytes are output following the message bytes.
- 1 - Check bytes are not output following the message bytes. Correction will be done regardless depending upon the bit 4, RAW, setting.

[2] - CRCTS - Correction Control

- 0 - Outputs corrections vectors; to obtain corrected data, externally XOR the output vector with the corresponding message or check bytes.
- 1 - Outputs corrected data

[3] - FOR - Forward Order Control

- 0 - Outputs the block in reverse order
- 1 - Outputs the block in forward order

[4] - RAW - Raw Data

- 0 - Outputs corrections or corrected data per the CRCTS bit
- 1 - Outputs uncorrected, raw input data or 0's depending upon the CRCTS bit setting. (See table below). NOPAR bit and CHECK BYTE register settings are ignored.

[5] - ERC - Erasure Rejection Control. This bit is only used by the device when the Erasures exceed the ERROR THRESHOLD or R settings. This bit is ignored when the Erasures are less than or equal to ERROR THRESHOLD or R.

- 0 - If Erasures are greater than the ERROR THRESHOLD or R then erasures are discarded and full correction is performed. The block is flagged uncorrectable and the output CRTN will be high during the last output byte of the block.
- 1 - If Erasures are greater than ERROR THRESHOLD or R then erasures are discarded and full correction is performed. The output CRTN will be high only when the block is uncorrectable.

[7:6] - Reserved, Set to 0.

RAW	CRCTS	Output
0	0	Corrections
0	1	Corrected data
1	0	Zero
1	1	Uncorrected data

2.6 ENCODE, DECODE, OR PASS-THROUGH OPERATIONS

The device performs three functions: encoding, decoding, and pass through. As an encoder the device transmits the message block and appends the check bytes at the end of the message bytes. As a

decoder, the device outputs the corrected message bytes or correction vectors with or without check bytes following the message. In the pass-through-mode, the device passes the input data as it is received. In all three operations, the input block flows through the Input FIFO into the ECC module and out of the Output FIFO. Latencies for all three operations are the same.

The device is initialized for the three modes as shown in the table below.

Table 1: Initialization Register Settings for Encode, Decode, and Pass-Through Operations

INITIALIZATION REGISTER	*BIT(S)*	*ENCODE*	*DECODE*	*PASS-THROUGH*
ERASURE MULTIPLIER	[7:0]	Appendix A value	Appendix A value	Appendix A value
ERROR THRESHOLD	[7:0]	Set to R	R or less	0x02
CHECK BYTES	[7:0]	Set to R	R	0x02
MESSAGE BYTES	[7:0]	Set to the Number of Message Bytes in block, K	K	K
BLOCK LENGTH	[7:0]	Set to the total of Message and Check bytes, N	N	K + 2
CONTROL BYTE	0(RESV)	0	0	0
	1(NOPAR)	0	System specific	0
	2(CRCTS)	1	System specific	1
	3(FOR)	System Specific	System specific	System specific
	4 (RAW)	0	0	1
	5 (ERC)	0	0	0
	[7:6] Reserved	0	0	0

As an encoder, the device is used with Erasures feature enabled in the following sequence.

1. After initialization, the device receives the message data followed by dummy check bytes. "Dummy" check bytes are clocked into the device with the ERASE signal asserted. The number of "Dummy" check bytes must equal R.
2. The ECC core processes the block by "correcting" the check bytes and feeding the block into the Output FIFO.
3. The block is then made available on the output bus, DO. The state of the output signal, RDYON determines the availability of data. ERR signal is asserted while the "corrected check bytes" are output on the output bus, DO. CRTN is asserted low during the last byte out of the chip indicating that the previous block did not exceed the error threshold.

As a decoder, the device works similar to the encode operation in the following sequence.

1. Following initialization, the system clocks the message data and the check bytes into the input port FIFO. ERASE signal may be asserted as desired by the system. The state of the output signal, RDYIN determines the chip's ability to accept data input on the DI bus.
2. The ECC Core processes the block by performing the necessary corrections, and feeds the block into the Output FIFO.
3. The data is available on the Output FIFO. The state of the output signal, RDYON determines the availability of valid data. An output byte which has been corrected is indicated by the device asserting ERR signal. CRTN may be asserted high or low depending upon the THRESHOLD Register and ERC bit programmed and the errors encountered.

In the pass-through-mode, data flows through the device similar to the Encode and Decode operations:

1. Following initialization, the system clocks the message data into the Input FIFO.

2. The data is processed by the ECC module and passed on to the Output FIFO without correction.
3. The data is available at the output ports. The state of the RDYON determines the availability of valid data. The ERASE input is ignored during the Input phase and ERR and CRTN outputs are not valid.

2.7 FIFOs

The Input and Output Ports each contain a single-ported 256x8 bytes FIFO. These FIFOs buffer input and output data during the correction process and help maintain the desired system rate. The FIFOs support the ECC module during its operation phases: data-in, calculation, and data out. A Reset operation as described in the Initialization Sequence section clears the FIFOs.

The Input FIFO receives input data on the DI bus when the ECC module is in the calculation or in data-out phases at the desired system rate. The ability of the Input FIFO to accept data is indicated by RDYIN.

The Output FIFO accepts corrections for the ECC during the data-out phase. Corrections are placed in the FIFO at 1 clock/byte by the ECC module to be removed by the system at its desired rate. RDYON is asserted low when the Output FIFO is able to output data.

Input and output operations through the device may occur in burst or continuous modes. Number of clocks used to input or output per byte determines burst or continuous mode operation. Figure 4 shows the two operation modes.

Burst mode permits data to be clocked in and out of the device at the maximum rate, ie., 1 clock per byte. In burst mode, consecutive data blocks are clocked into the device following a processing latency period. Data is input into the Input FIFO and processed through the ECC core. After a processing latency period the entire block of data is transferred to the Output FIFO. While the Output FIFO is being emptied, the Input FIFO is simultaneously filled with the following block at the maximum rate. Writing to the Input FIFO is allowed as long as RDYIN is active and reading from the Output FIFO is permitted as long as RDYON is active. Input and output rates are controlled by the clock speed and clocks/byte.

Continuous mode requires a minimum of 4 through 338 clocks/byte depending upon the block size. Maximum data transfer rates for continuous rate vary accordingly. Blocks may be processed continuously through the device in this mode. The RDYIN and RDYON pins will always be active after the initial latency period.

2.8 DATA RATE AND LATENCIES

This section describes data rates and processing latencies for the two operating modes supported by AHA4011: burst and continuous. Processing latencies are the same for encode, decode, or pass through mode operations. Number of clocks per input or output byte determines the mode of operation.

A minimum of one clock is required per data byte. Input and Output clock rates may be different, depending upon the required system performance. Continuous block flow is achieved by using the appropriate number of clocks/byte and block length. Alternatively, data flow into and out of the device is controlled using control signals, DSIN and DSON.

The AHA4011 can be used in either "burst" or "continuous" modes. Mode of operation is determined by the number of clocks used to clock in and out of the device along with the input control signals DSIN and DSON. The input and output rates need not be the same. No registers are required to program the device for either operation.

Data may be input or output through the device at up to 40 MBytes/sec. In burst mode, the maximum rate of 40 MBytes/sec may be employed for the entire block. The RDYIN and RDYON indicate when the device is ready to accept or output data.

Processing latency, expressed in number of clocks, for burst mode is determined by: $N \times C_i + R + 60 + N$ for forward order output and $N \times C_i + R + 60$ for reverse order output.

Definitions:

C_i = input clocks/byte. For rates below 3 clocks/byte, C_i is fixed at 3 in the equation
N = block length
R = number of check bytes
Processing Latency = Delay from first input byte to first output byte

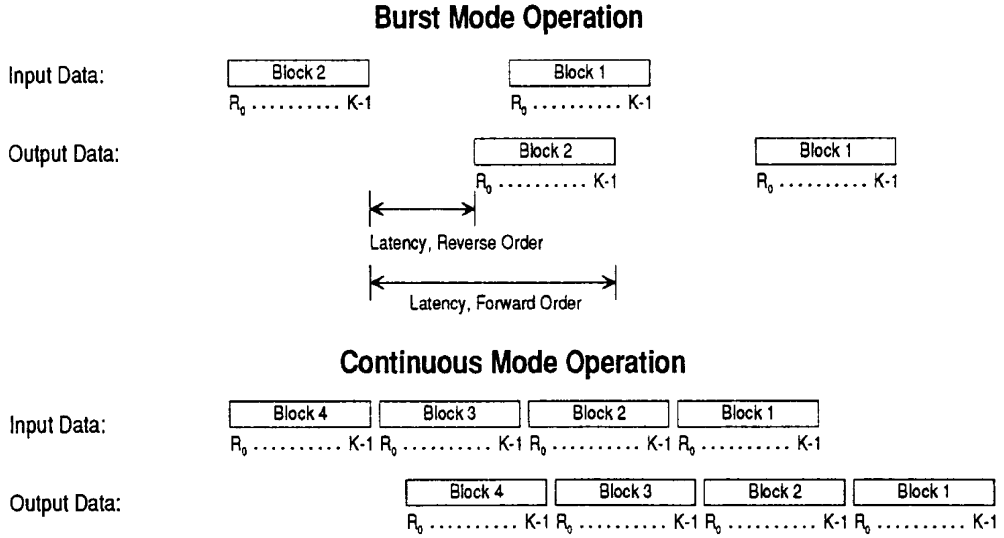
For a 40 MHz system using 1 clock/byte, latencies and data rates for forward order output are shown in the table for burst mode operation. Input and Output Burst Rates in all cases will be 40 MBytes/sec. Note: Other frequency operations are also possible.

Table 2: Burst Mode Operation Using 40 MHz Clock and 1 Clock/Byte

BLOCK LENGTHS 'N'	CHECK BYTES 'R' = 20		CHECK BYTES 'R' = 2	
	MAXIMUM LATENCY (µsecs)	AVERAGE RATE (MBytes/sec)	MAXIMUM LATENCY (µsecs)	AVERAGE RATE (MBytes/sec)
25	3.88	6.45	3.43	7.30
50	5.75	8.70	5.30	9.43
100	9.50	10.50	9.05	11.00
150	13.30	11.30	12.80	11.70
200	17.00	11.80	16.60	12.10
255	21.10	12.10	20.70	12.30

In continuous mode, minimum of 4 through 338 clocks/byte are required depending upon the block size. Maximum data transfer rates for continuous mode vary accordingly. Blocks may be input one after another continuously into the device in this mode since the Input FIFO will never be completely filled.

Figure 4: Operating Modes - Burst and Continuous



The maximum processing latency, expressed in number of clocks, for continuous mode is determined by: $(N - 1) \times C_i + R + 60 + N \times (C_i / C_t - 1)$ for forward order output. Processing latency for reverse order output is approximately N clock cycles less than the forward order.

The following conditions must be met for the continuous mode to operate properly $(R + 60 + N \times C_o /(C_o - 1) - N \times (C_o - C_i)) \times (1/C_i) \leq 256$ and $N - 1 \times C_t \geq R + 48 + 2 \times N \times C_i /(C_i - 1)$

Definitions:

C_i = input clocks/byte

C_0 = output clocks/byte

For a 40 MHz system using the required clocks/byte, maximum latencies and data rates for forward order output are shown in the table for continuous operation. Input and Output rates are assumed the same in this table. Note: Other frequency operations are also possible.

Table 3: Continuous Mode Operation Using 40 MHz Clock and Specified Clocks/Byte

	CHECK BYTES 'R' = 20			*CHECK BYTES 'R' = 2*		
BLOCK LENGTHS 'N'	*MINIMUM REQUIRED (clocks/byte)*	*MAXIMUM DATA RATE (MBytes/sec)*	*MAXIMUM LATENCY (µsecs)*	*MINIMUM REQUIRED (clocks/byte)*	*MAXIMUM DATA RATE (MBytes/sec)*	*MAXIMUM LATENCY (µsecs)*
25	5	8	5.78	5	8	5.33
50	5	8	9.69	4	10	8.12
100	4	10	15.20	4	10	14.80
150	4	10	21.90	4	10	21.50
200	6	6.67	37.90	6	6.67	37.40
225	11	3.64	69.80	11	3.64	69.30
255	338	0.118	2.15E+3	338	0.118	2.15E+3

For Intelsat IESS-308, Rev F, Inner FEC Rates, use Table 4 below for a system with 40 MHz clock. Note: Other frequency operations are also possible.

Table 4: Continuous Mode Operation for IESS-308 Codes Using 40 MHz Clock and Specified Clocks/Byte

BLOCK LENGTHS 'N'	*MESSAGE LENGTH 'K'*	*ERROR CAPABILITY 't'*	*MINIMUM REQUIRED (clocks/byte)*	*MAXIMUM DATA RATE (MBytes/sec)*	*MAXIMUM LATENCY (µsecs)*
126	112	7	4	10	18.60
194	178	8	6	6.67	36.70
208	192	8	7	5.71	49.20
219	201	9	9	4.44	57.20
225	205	10	11	3.64	69.80

Appendix B shows a spreadsheet table of block lengths vs. latencies for a 40 MHz clock system.

2.9 REED-SOLOMON (ECC) MODULE AND ERROR RATE PERFORMANCE

The module implements a full error correcting Reed-Solomon (RS) decoder whose function is to perform the necessary corrections on the input blocks. The code used by the decoder is capable of generating corrections for up to 10 (t = 10) byte-errors in an RS block over the block length between R + 1 to 255 bytes. The number of message bytes in an RS block, K, is equal to the RS block length minus R (K = N - R). The RS code implemented uses the primitive polynomial

$$P(x) = x^8 + x^7 + x^2 + x + 1$$

to generate GF(256). The generator polynomial for the code is:

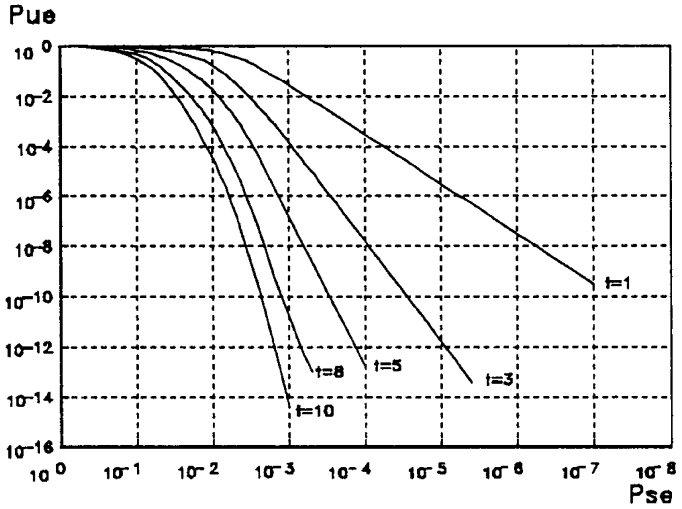
$$G(x) = \prod_{i=120}^{119+R} (x-\alpha^i)$$

An RS block consists of message and redundancy bytes. The number of message bytes in the block, K, is programmable during initialization. The number of check bytes is R and can be programmed during initialization to be 2 through 20 in increments of 1.

The ECC Module may be programmed to be corrections or corrected data. If corrections is selected, to obtain corrected data, externally XOR the output vector with the corresponding message or check byte. For example, if "corrections" is selected for a block of 200 bytes with errors in locations 100, 123, 153, 176, and 199; output block will be 0's for all locations except for those positions. The bytes output at these positions are referred to as vectors and may be XOR'd externally with the message bytes to obtain the correct value. If the output of the AHA4011 is programmed to output corrected data, the correction vector is applied internally and the corrected data is output.

The Symbol Error Rate Performance of the Reed Solomon code used is shown in Figure 5.

Figure 5: Symbol (Byte) Error Rate Performance Curves



The most common measures of performance for Reed-Solomon code are P_{UE}, P_{SE}, and C_{BER}. P_{SE} is the probability of symbol errors and is the ratio of the number of received symbol errors to the total number of received symbols. In the AHA4011 device, a symbol is 8 bits. P_{UE} is the probability of an uncorrectable error and is the ratio of the number of uncorrectable code blocks to the total number of received code blocks. An uncorrectable error occurs when more than t received symbols are in error. C_{BER} is the Corrected Bit Error Rate. The C_{BER} is the reciprocal of expected number of correct bits between errors.

If input noise is random, $P_{SE} = (P_{BE} \times 8)$ and $C_{BER} = m \times N / P_{UE}$.

If $P_{BE} = 10^{-4}$ then $P_{SE} = 8 \times 10^{-4}$ with t = 5, $P_{UE} = 10^{-7}$ and $C_{BER} = 255 \times 8/10^{-7} \approx 1.6 \times 10^{11}$.

The figure shows probability of Symbol Error and Uncorrectable Error for Block Size (N) of 255. It shows the ability of various levels of Reed-Solomon error correction to restore the integrity of the corrupted data. For example, using 255 byte blocks, if 1 out of 1000 of the received bytes have one or more bit errors, RS correction with t = 5 will restore the data to 1 error in 2 million blocks (510 million bytes). The input byte error rate corresponds to an input block error rate of 1 in 4.

For a detailed discussion on Error Rate performance of Reed-Solomon code, refer to the AHA Application Note, ANRS01: Reed-Solomon Primer.

2.10 DETERMINING DECODER PERFORMANCE BOUNDARIES

AHA4011 supports a programmable feature that allows a system designer to determine the channel performance. This programmable feature, referred to as error threshold, P, sets a number of errors to be allowed by the chip prior to flagging the block uncorrectable. Erasure Rejection Control bit of the Control Byte register determines the condition of CRTN output pin.

Caveat: Message bytes output may have additional errors than what was started if the total number of errors exceed t or the sum of errors and marked erasures exceed the R value programmed. For example, if N = 200 and R = 10 and the block has more than 5 byte errors, the device output block may contain more than 5 errors.

P and R are both independently selectable by the user during the Initialization Control sequence. The various configurations of P and R are described as follows:

P > R This is not a sensible choice since this implies that more check bytes are allocated for (correction-only) purposes than there are total check bytes (for both correction and detection). The device will work as if P was set equal to R.

P = R This configuration maximizes the ability to correct errors, particularly if R itself has been chosen to be its maximum value of 10. This is the usual choice.

P < R This increases the relative level of error detection capability; relative to the level of error correction capability. This situation causes the CRTN output to flag a message block as uncorrectable at an error level below that of which the device is capable.

2.11 ERASURES

The chip is capable of utilizing erasure information. R erasures may be corrected in any block assuming there are no unmarked errors.

The correction capability is: $E + 2e \leq R$

Where E = number of erasures (marked errors)
e = number of unmarked errors
R = number of check symbols

If there are more than P or R erasures the erasure information is discarded, and full error correction is attempted. The chip can be programmed to either call such a block uncorrectable or not. If programmed not to call the block uncorrectable (ERC bit set to 1), the ECC will utilize the full error correction capability to decide if the block is correctable.

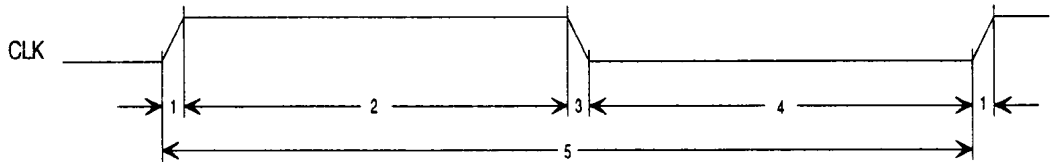
3.0 OPERATIONAL DESCRIPTION

This section describes the relationship of associated signals for various functions of the chip.

3.1 CLOCK

The clock input to the chip must meet the timing requirements shown in Figure 6. The chip is entirely static thus allowing the clock to stop in either the active or inactive state for an indefinite period.

Figure 6: CLK Characteristics



NUMBER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
1	CLK Rise Time		2	nsec
2	CLK High Time	10		nsec
3	CLK Fall Time		2	nsec
4	CLK Low Time	10		nsec
5	CLK Period	25		nsec

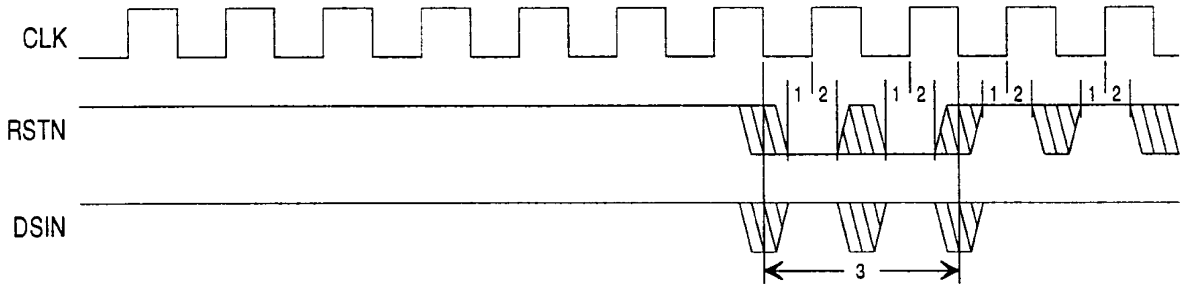
All timing diagrams in this specification use the clock at the CLK pin as the reference point.

3.2 INITIALIZATION

This section describes the Reset and Initialization Sequence timing. For a detailed discussion on these sequences, refer to Section 2.5 "Initialization Sequence".

For the Reset Sequence, RSTN must be active and DSIN inactive for at least two clocks. These signals are sampled during rising edges of the CLK input.

Figure 7: Reset Timing



NUMBER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
1	RSTN and DSIN setup time	12		nsec
2	RSTN and DSIN hold time	0		nsec
3	RSTN and DSIN assertion	2		Clock edges

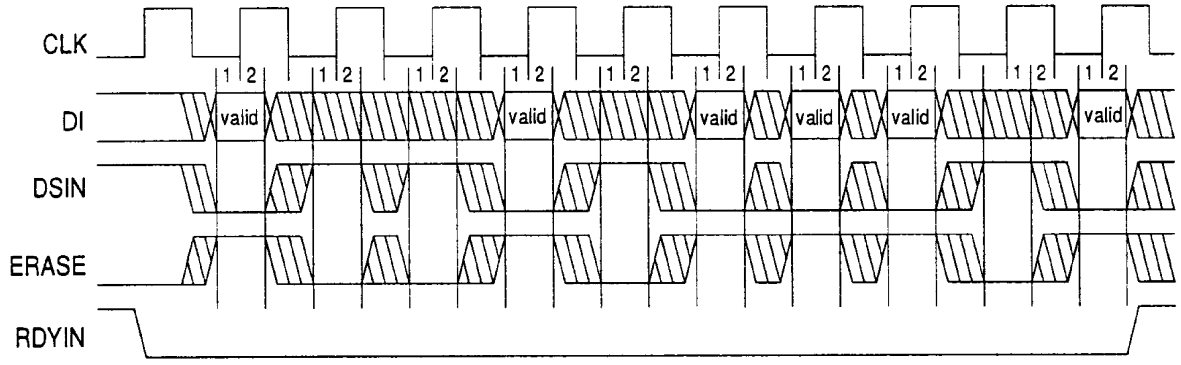
Initialization bytes are strobed into the device while RSTN and DSIN are low during rising edges of CLK. The RSTN must be active low for at least two clocks before the first initialization byte is strobed in and remain active for at least one clock after the final byte. If initialization bytes are not loaded while RSTN is active, the bytes maintain their previously defined values. After power-on the intializing registers' contents are undefined.

For a detailed description of the Initialization Registers, refer to Section 2.5 "Initialization Sequence".

3.3 DATA INPUT MODE

The chip latches the input data on the DI pins on the rising edge of the CLK when DSIN and RDYIN are both active. The two figures below show the timing diagrams for FIFO Ready and FIFO Not Ready conditions.

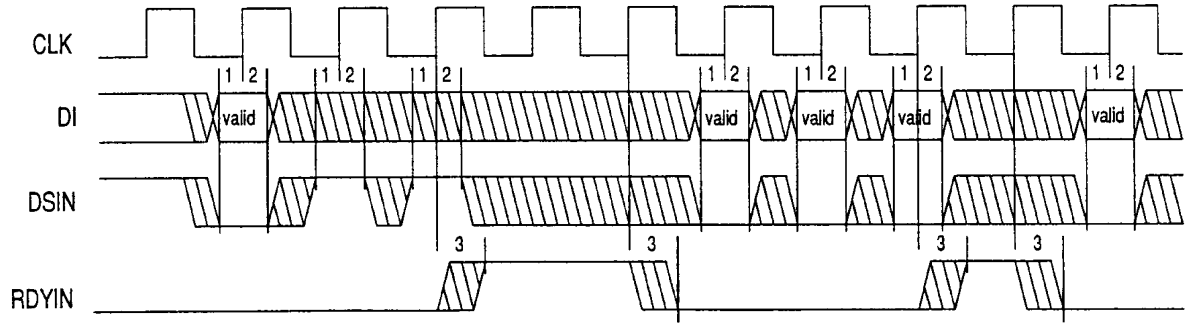
Figure 8: Data Input - Input FIFO Always Ready



If RSTN is low during write, message bytes are treated as being part of the initialization sequence. If RSTN is high, the data is treated as being part of RS block.

NUMBER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
1	DI, ERASE and DSIN setup time	12		nsec
2	DI and DSIN hold time	0		nsec

Figure 9: Data Input - FIFO Not Ready



NUMBER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
1	DI, ERASE and DSIN setup time	12		nsec
2	DI, ERASE and DSIN hold time	0		nsec
3	RDYIN output delay		13	nsec

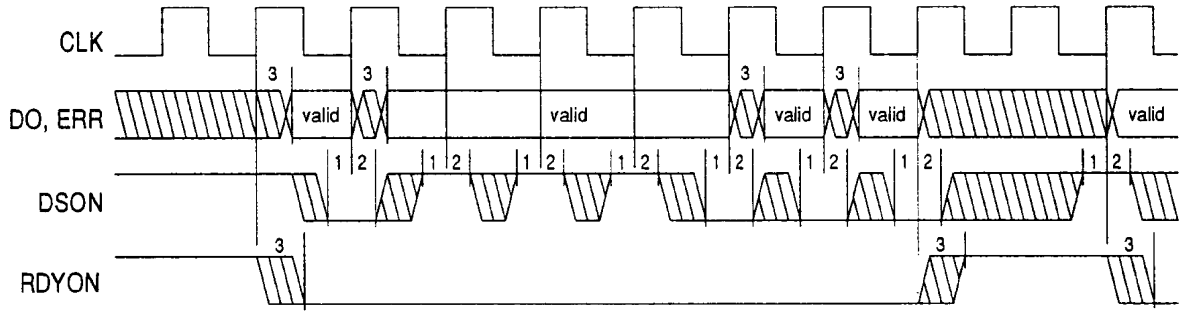
Any input data clocked while RDYIN is inactive are ignored. This is shown in Figure 9.

3.4 DATA OUTPUT

The DO pins are driven from a register clocked on the rising edge of CLK.

Valid data on the DO pins is indicated by RDYON being active. When RDYON is inactive, data on the DO pins is undefined, and DSON is ignored. The DSON signal acknowledges receiving the data and is used by the device to internally increment the address counter. This data output timing is shown in Figure 10.

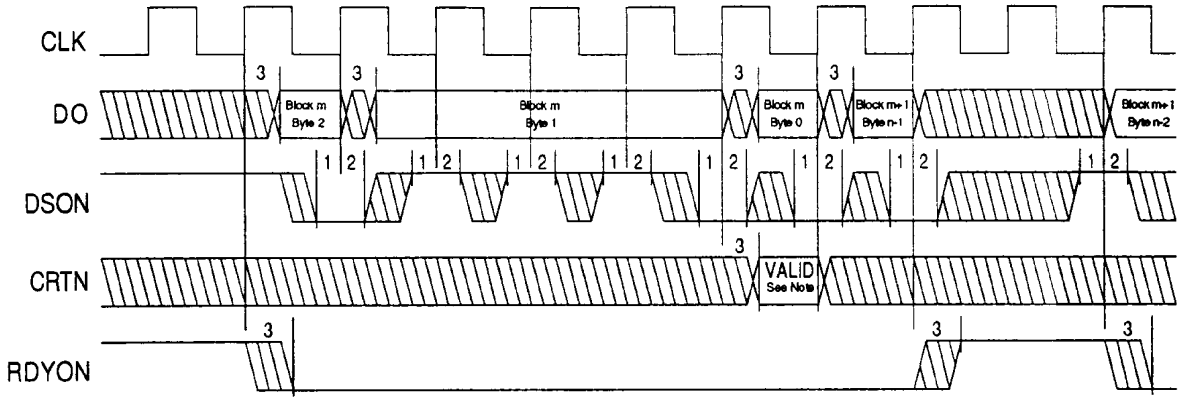
Figure 10: Data Output



NUMBER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
1	DSON setup time	12		nsec
2	DSON hold time	0		nsec
3	DO and RDYON output delay		13	nsec

CRTN is valid for an RS block during the output byte 0 for that block. Therefore CRTN is valid during the last byte of the block out of the device. See Figure 11.

Figure 11: CRTN Timing



Note: CRTN will be active (low) if RS block M was correctable. If the number of errors detected in block M exceeds the error threshold, p, CRTN will be inactive (high).

NUMBER	DESCRIPTION	MINIMUM	MAXIMUM	UNITS
1	DSON setup time	12		nsec
2	DSON hold time	0		nsec
3	DO and RDYON output delay		13	nsec

4.0 SIGNAL SPECIFICATIONS

4.1 INPUT SPECIFICATIONS

PIN NUMBER	SIGNAL NAME	SELF LOAD (MAXIMUM)	TSETUP (MIN IN NSEC)	THOLD (MIN IN NSEC)	STROBE
43	DI[7]	7pF	12	0	CLK
44	DI[6]	7pF	12	0	CLK
1	DI[5]	7pF	12	0	CLK
2	DI[4]	7pF	12	0	CLK
3	DI[3]	7pF	12	0	CLK
4	DI[2]	7pF	12	0	CLK
5	DI[1]	7pF	12	0	CLK
6	DI[0]	7pF	12	0	CLK
42	DSIN	7pF	12	0	CLK
33	DSON	7pF	12	0	CLK
35	RSTN	7pF	12	0	CLK
41	CLK	7pF	N/A	N/A	N/A
34	ERASE	7pF	12	0	CLK

N/A = Not Applicable

(Refer to DC ELECTRICAL CHARACTERISTICS for pad specifications)

4.2 OUTPUT SPECIFICATIONS

PIN NUMBER	SIGNAL NAME	LOAD CAP (MAXIMUM)	TDEL (MIN IN NSEC)	TDEL (MAX IN NSEC)	STROBE REF
26	DO[7]	60pF	N/A	13	CLK
24	DO[6]	60pF	N/A	13	CLK
23	DO[5]	60pF	N/A	13	CLK
22	DO[4]	60pF	N/A	13	CLK
21	DO[3]	60pF	N/A	13	CLK
20	DO[2]	60pF	N/A	13	CLK
19	DO[1]	60pF	N/A	13	CLK
18	DO[0]	60pF	N/A	13	CLK
31	RDYON	60pF	N/A	13	CLK
32	RDYIN	60pF	N/A	13	CLK
28	CRTN	60pF	N/A	13	CLK
27	ERR	60pF	N/A	13	CLK

(Refer to DC ELECTRICAL CHARACTERISTICS for pad specifications)

4.3 POWER & GROUND PINS

PIN NUMBER	*SIGNAL NAME*
40, 30, 29, 17	GND
7, 25, 36, 39	VDD

4.4 AC ELECTRICAL CHARACTERISTICS

CLOCK RATE					
Symbol	**Characteristic**	**Min**	**Max**	**Units**	**Test Conditions**
Fclock	Clock Frequency	0	40	MHz	
Tlow	Clock low time	10		nsec	
Thigh	Clock high time	10		nsec	
Trise	Clock rise time		2	nsec	10% to 90%
Tfall	Clock fall time		2	nsec	90% to 10%

INPUTS					
Symbol	**Characteristic**	**Min**	**Max**	**Units**	**Test Conditions**
Tsetup	Input setup time	12		nsec	See note
Thold	Input hold time	0		nsec	See note
Trise	Input rise time		2	nsec	10% to 90%
Tfall	Input fall time		2	nsec	90% to 10%
(Note: Setup and hold times measured from a valid high [2.4V] on the clock input pin.)					

OUTPUTS					
Symbol	**Characteristic**	**Min.**	**Max.**	**Units**	**Test Conditions**
Tout	Output delay	0	13	nsec	See note
(Note: Output delay measured from valid high [2.4V] on the clock input pad.)					

4.5 DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM STRESS RATINGS					
Symbol	**Characteristics**	**Min.**	**Max.**	**Units**	**Test Conditions**
Tstg	Storage temperature	-55	150	deg C	
Vdd	Supply voltage	-0.5	6.0	V	
Vin	Input voltage	Vss-0.5	Vdd+0.5	V	
Ilp	Latch-up current	-100	100	mA	-2V<Vpin<8V
ESD	Electrostatic Discharge	-3000	+3000	V	Human Body model
Package: 44 -pin PLCC (JEDEC Standard)					

OPERATING CONDITIONS					
Symbol	**Characteristics**	**Min**	**Max**	**Units**	**Test Conditions**
Vdd	Supply Voltage	4.75	5.25	V	
Idd	Supply current		10	mA	Static
Idd	Supply current		60	mA	Dynamic
Ta	Operating temperature	0	70	deg C	
P	Power		0.32	W	

INPUTS					
Symbol	**Characteristics**	**Min**	**Max**	**Units**	**Test Conditions**
Vih	Input High Voltage	2.0	Vdd	V	
Vil	Input Low Voltage	Vss	0.8	V	
Iil	Input Leakage	-10	10	µA	0<Vin<Vdd
Cin	Capacitance		10	pF	

OUTPUTS					
Symbol	**Characteristics**	**Min**	**Max**	**Units**	**Test Conditions**
Voh	Output High Voltage	2.4	Vdd	V	Ioh=.8mA
Vol	Output Low Voltage	Vss	0.4	V	Iol=8mA
Ioh	Output High Current	-8		mA	Voh=2.4V
Iol	Output Low Current		8	mA	Vol=0.4
Ioz	High Impedance Leakage		10	µA	0<Vout<Vdd
Cout	Capacitance		10	pF	

5.0 PACKAGING

PLCC Dimensions

Inches
(Millimeters)

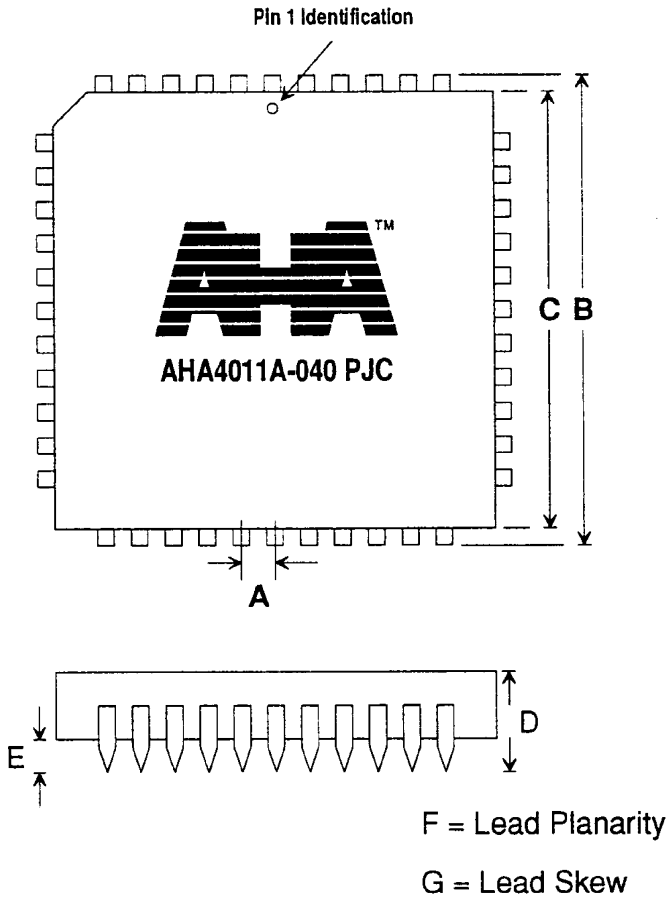
A	*B* *min/max*	*C* *min/max*	*D* *min/max*	*E* *min*	*F* ±	*G* ±
.050 (1.27)	.685/.695 (17.40/17.65)	.650/.656 (16.51/16.66)	.165/.180 (4.19/4.57)	.020 (0.51)	.002 (0.051)	.0035 (0.089)

Shipping

PIN COUNT	*STANDARD QTY/TUBE*	*STANDARD QTY/TRAY*
44	26	40

Units are shipped in quantities stated above. Production Purchase Orders should conform to multiples of 26 or 40 pieces per shipment.

Packaging



Complete Package Drawing Available Upon Request.

6.0 ORDERING INFORMATION

6.1 AVAILABLE PARTS

PART NUMBER	*DESCRIPTION*
AHA4011A-040 PJC	Reed-Solomon ECC Integrated Circuit

6.2 PART NUMBERING

AHA	*4011*	*A -*	*040*	*P*	*J*	*C*
Manufacturer	Device Number	Revision Level	Speed Designation	Package Material	Package Type	Test Specification

Device Number:
4011A

Package Material Codes:
P Plastic

Package Type Codes:
J J - Leaded Chip Carrier

Test Specifications:
C Commercial 0°C to +70°C

Detailed test information is available on request.

7.0 RELATED TECHNICAL PUBLICATIONS

PART NUMBER	*DESCRIPTION*
ANRS01	AHA Application Note - Reed Solomon Primer
ANRS02	AHA Application Note - Reed Solomon Interleaving
PB4011	Product Brief, AHA4011
PS4x10	Product Specification, AHA4510, AHA4010
ABSTD1	AHA Data Compression and R-S Standards
IESS-308, Rev 6B, Appendix F	Concatenation of Reed-Solomon (RS) Outer Coding with the Existing Inner FEC

APPENDIX A

Table of Elements

BLOCK SIZE 'N'	HEX VALUE	BLOCK SIZE 'N'	HEX VALUE	BLOCK SIZE 'N'	HEX VALUE	BLOCK SIZE 'N'	HEX VALUE
1	1	2	2	3	4	4	8
5	10	6	20	7	40	8	80
9	87	10	89	11	95	12	ad
13	dd	14	3d	15	7a	16	f4
17	6f	18	de	19	3b	20	76
21	ec	22	5f	23	be	24	fb
25	71	26	e2	27	43	28	86
29	8b	30	91	31	a5	32	cd
33	1d	34	3a	35	74	36	e8
37	57	38	ae	39	db	40	31
41	62	42	c4	43	f	44	1e
45	3c	46	78	47	f0	48	67
49	ce	50	1b	51	36	52	6c
53	d8	54	37	55	6e	56	dc
57	3f	58	7e	59	fc	60	7f
61	fe	62	7b	63	f6	64	6b
65	d6	66	2b	67	56	68	ac
69	df	70	39	71	72	72	e4
73	4f	74	9e	75	bb	76	f1
77	65	78	ca	79	13	80	26
81	4c	82	98	83	b7	84	e9
85	55	86	aa	87	d3	88	21
89	42	90	84	91	8f	92	99
93	b5	94	ed	95	5d	96	ba
97	f3	98	61	99	c2	100	3
101	6	102	c	103	18	104	30
105	60	106	c0	107	7	108	e
109	1c	110	38	111	70	112	e0
113	47	114	8e	115	9b	116	b1
117	e5	118	4d	119	9a	120	b3
121	e1	122	45	123	8a	124	93
125	a1	126	c5	127	d	128	1a

BLOCK SIZE 'N'	HEX VALUE	BLOCK SIZE 'N'	HEX VALUE	BLOCK SIZE 'N'	HEX VALUE	BLOCK SIZE 'N'	HEX VALUE
129	34	130	68	131	d0	132	27
133	4e	134	9c	135	bf	136	f9
137	75	138	ea	139	53	140	a6
141	cb	142	11	143	22	144	44
145	88	146	97	147	a9	148	d5
149	2d	150	5a	151	b4	152	ef
153	59	154	b2	155	e3	156	41
157	82	158	83	159	81	160	85
161	8d	162	9d	163	bd	164	fd
165	7d	166	fa	167	73	168	e6
169	4b	170	96	171	ab	172	d1
173	25	174	4a	175	94	176	af
177	d9	178	35	179	6a	180	d4
181	2f	182	5e	183	bc	184	ff
185	79	186	f2	187	63	188	c6
189	b	190	16	191	2c	192	58
193	b0	194	e7	195	49	196	92
197	a3	198	c1	199	5	200	a
201	14	202	28	203	50	204	a0
205	c7	206	9	207	12	208	24
209	48	210	90	211	a7	212	c9
213	15	214	2a	215	54	216	a8
217	d7	218	29	219	52	220	a4
221	cf	222	19	223	32	224	64
225	c8	226	17	227	2e	228	5c
229	b8	230	f7	231	69	232	d2
233	23	234	46	235	8c	236	9f
237	b9	238	f5	239	6d	240	da
241	33	242	66	243	cc	244	1f
245	3e	246	7c	247	f8	248	77
249	ee	250	5b	251	b6	252	eb
253	51	254	a2	255	c3		

For example, for a block size of 205, the value to be programed in Byte 1 of the Initialization Register is 0xc7.

APPENDIX B

AHA4011 Data Rate Calculations in Continuous Mode Operation

Assumptions:

1. 40 MHz Clock is used
2. Input Rate (C_i) = Output Rate (C_o) = 4 clocks/byte
3. Latency = C_i x (N -1) + (R + 60) + N x (C_i / (C_i-1)) Forward: maximum; C_i x (N -1) + (R + 60) Reverse: minimum
4. Average Rate = 40 MHz/4 clocks/byte
5. GOOD or BAD based on inequality equation: (R x 60 + (N) x (C_o) / (C_o-1)-(N) x (C_o-C_i)) x (1/C_i) + N ≤ 256
6. GOOD or BAD based on inequality equation: (N - 1) x C_i ≥ R + 48 + 2 x (C_i / C_i - 1) x N

			FORWARD ORDER		REVERSE ORDER				
CLOCKS /BYTE	N	T	CLOCKS /BLOCK	MAXIMUM LATENCY (sec)	CLOCKS /BLOCK	MINIMUM LATENCY (sec)	DATA RATE (MB/sec)	EQUATION 5	EQUATION 6
4	25	10	209	5.23E-06	176	4.40E-06	10.00	GOOD	BAD
4	50	10	343	8.57E-06	276	6.90E-06	10.00	GOOD	BAD
4	53	10	359	8.97E-06	288	7.20E-06	10.00	GOOD	BAD
4	75	10	476	1.19E-05	376	9.40E-06	10.00	GOOD	GOOD
4	100	10	609	1.52E-05	476	1.19E-05	10.00	GOOD	GOOD
4	126	7	742	1.86E-05	574	1.44E-05	10.00	GOOD	GOOD
6	194	8	1467	3.67E-05	1234	3.09E-05	6.67	GOOD	GOOD
8	208	8	1970	4.92E-05	1732	4.33E-05	5.00	GOOD	GOOD
9	219	9	2286	5.72E-05	2040	5.10E-05	4.44	GOOD	GOOD
4	200	10	1143	2.86E-05	876	2.19E-05	10.00	BAD	GOOD
11	225	10	2792	6.98E-05	2544	6.36E-05	3.64	GOOD	GOOD
4	250	10	1409	3.52E-05	1076	2.69E-05	10.00	BAD	GOOD
4	255	10	1436	3.59E-05	1096	2.74E-05	10.00	BAD	GOOD

			FORWARD ORDER		REVERSE ORDER				
CLOCKS /BYTE	N	T	CLOCKS /BLOCK	MAXIMUM LATENCY (sec)	CLOCKS /BLOCK	MINIMUM LATENCY (sec)	DATA RATE (MB/sec)	EQUATION 5	EQUATION 6
4	25	5	199	4.98E-06	166	4.15E-06	10.00	GOOD	BAD
4	50	5	333	8.32E-06	266	6.65E-06	10.00	GOOD	GOOD
4	75	5	466	1.17E-05	366	9.15E-06	10.00	GOOD	GOOD
4	100	5	599	1.50E-05	466	1.17E-05	10.00	GOOD	GOOD
4	125	5	733	1.83E-05	566	1.42E-05	10.00	GOOD	GOOD
4	150	5	866	2.17E-05	666	1.67E-05	10.00	GOOD	GOOD
4	175	5	999	2.50E-05	766	1.92E-05	10.00	GOOD	GOOD

			FORWARD ORDER		REVERSE ORDER				
CLOCKS /BYTE	N	T	CLOCKS /BLOCK	MAXIMUM LATENCY (sec)	CLOCKS /BLOCK	MINIMUM LATENCY (sec)	DATA RATE (MB/sec)	EQUATION 5	EQUATION 6
4	200	5	1133	2.83E-05	866	2.17E-05	10.00	BAD	GOOD
4	225	5	1266	3.17E-05	966	2.42E-05	10.00	BAD	GOOD
4	250	5	1399	3.50E-05	1066	2.67E-05	10.00	BAD	GOOD
4	255	5	1426	3.57E-05	1086	2.72E-05	10.00	BAD	GOOD

			FORWARD ORDER		REVERSE ORDER				
CLOCKS /BYTE	N	T	CLOCKS /BLOCK	MAXIMUM LATENCY (sec)	CLOCKS /BLOCK	MINIMUM LATENCY (sec)	DATA RATE (MB/sec)	EQUATION 5	EQUATION 6
4	25	3	195	4.88E-06	162	4.05E-06	10.00	GOOD	BAD
4	50	3	329	8.22E-06	262	6.55E-06	10.00	GOOD	GOOD
4	75	3	462	1.16E-05	362	9.05E-06	10.00	GOOD	GOOD
4	100	3	595	1.49E-05	462	1.16E-05	10.00	GOOD	GOOD
4	125	3	729	1.82E-05	562	1.41E-05	10.00	GOOD	GOOD
4	150	3	862	2.16E-05	662	1.66E-05	10.00	GOOD	GOOD
4	175	3	995	2.49E-05	762	1.91E-05	10.00	GOOD	GOOD
4	200	3	1129	2.82E-05	862	2.16E-05	10.00	BAD	GOOD
4	225	3	1262	3.16E-05	962	2.41E-05	10.00	BAD	GOOD
4	250	3	1395	3.49E-05	1062	2.66E-05	10.00	BAD	GOOD
4	255	3	1422	3.56E-05	1082	2.71E-05	10.00	BAD	GOOD

			FORWARD ORDER		REVERSE ORDER				
CLOCKS /BYTE	N	T	CLOCKS /BLOCK	MAXIMUM LATENCY (sec)	CLOCKS /BLOCK	MINIMUM LATENCY (sec)	DATA RATE (MB/sec)	EQUATION 5	EQUATION 6
4	25	1	191	4.78E-06	158	3.95E-06	10.00	GOOD	BAD
4	50	1	325	8.12E-06	258	6.45E-06	10.00	GOOD	GOOD
4	75	1	458	1.15E-05	358	8.95E-06	10.00	GOOD	GOOD
4	100	1	591	1.48E-05	458	1.15E-05	10.00	GOOD	GOOD
4	125	1	725	1.81E-05	558	1.40E-05	10.00	GOOD	GOOD
4	150	1	858	2.15E-05	658	1.65E-05	10.00	GOOD	GOOD
4	175	1	991	2.48E-05	758	1.90E-05	10.00	GOOD	GOOD
4	200	1	1125	2.81E-05	858	2.15E-05	10.00	BAD	GOOD
4	225	1	1258	3.15E-05	958	2.40E-05	10.00	BAD	GOOD
4	250	1	1391	3.48E-05	1058	2.65E-05	10.00	BAD	GOOD
4	255	1	1418	3.55E-05	1078	2.70E-05	10.00	BAD	GOOD