N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
240V	45Ω	150mA	2N7007

Features

- ☐ Free from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

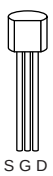
- ☐ Motor controls
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±30V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Package Options



TO-92

Note 1: See Package Outline section for dimensions.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}*	I_{DRM}
TO-92	65mA	260mA	1W	125	170	65mA	260mA

* I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	240			V	I_D = 100µA, V_{GS} = 0V
$V_{GS(th)}$	Gate Threshold Voltage	1		2.5	V	V_{GS} = V_{DS}, I_D = 250µA
I_{GSS}	Gate Body Leakage			10	nA	V_{GS} = ±20V, V_{DS} = 0V
I_{DSS}	Zero Gate Voltage Drain Current			100	nA	V_{GS} = 0V, V_{DS} = 120V
				1	µA	V_{GS} = 0V, V_{DS} = 120V T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	50			mA	V_{GS} = 4.5V, V_{DS} = 20V
		150				V_{GS} = 10V, V_{DS} = 20V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			45	Ω	V_{GS} = 4.5V, I_D = 20mA
				45		V_{GS} = 10V, I_D = 50mA
G_{FS}	Forward Transconductance	30			m℧	V_{DS} = 10V, I_D = 50mA
C_{ISS}	Input Capacitance			30	pF	V_{GS} = 0V, V_{DS} = 25V f = 1 MHz
C_{OSS}	Common Source Output Capacitance			15		
C_{RSS}	Reverse Transfer Capacitance			10		
$t_{(ON)}$	Turn-ON Time			30	ns	V_{DD} = 60V, I_D = 50 mA, R_{GEN} = 25Ω
$t_{(OFF)}$	Turn-OFF Time			20		
V_{SD}	Diode Forward Voltage Drop			1.2	V	I_{SD} = 65mA, V_{GS} = 0V

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit