PowerPC 405GP Embedded Processor Data Sheet

Features

- IBM PowerPC™ 405 32-bit RISC processor core operating up to 266 MHz
- PC-100 Synchronous DRAM (SDRAM) interface operating up to 133 MHz
  - 32-bit interface for non-ECC applications
  - 40-bit interface serves 32 bits of data plus 8 check bits for ECC applications
- 4KB On-chip Memory (OCM)
- External Peripheral Bus
  - Flash ROM/Boot ROM interface
  - Direct support for 8-, 16-, or 32-bit SRAM and external peripherals
  - Up to eight devices
  - External Mastering supported
- DMA support for external peripherals, internal UART and memory
  - Scatter-gather chaining supported
  - Four channels
- PCI Revision 2.2 Compliant Interface (32-bit, up to 66MHz)
  - PCI Bus interface can be configured to operate synchronously or asynchronously to the chip input clock
  - Internal PCI Bus Arbiter which can be disabled for use with an external arbiter
- Ethernet 10/100Mbps (full-duplex) support with Medium Independent Interface (MII)
- Programmable Interrupt Controller supports interrupts from a variety of sources
  - Seven external and 19 internal
  - Edge triggered or level-sensitive
  - Positive or negative active
  - Non-critical or critical interrupt to processor core
  - Programmable critical interrupt priority ordering
  - Programmable critical interrupt vector for faster vector processing
- Programmable Timers
- Two serial ports (16550 compatible UART)
- One IIC (I^2C) interface
- General Purpose I/O (GPIO) available
- Supports JTAG for board level testing
- Internal Processor Local Bus (PLB) runs at SDRAM interface frequency
- Supports PowerPC processor boot from PCI memory

Description

Designed specifically to address embedded applications, the PowerPC 405GP (PPC405GP) provides a high-performance, low-power solution that interfaces to a wide range of peripherals by incorporating on-chip power management features and intrinsically lower power dissipation requirements.

This chip contains a high-performance RISC processor core, SDRAM controller, PCI bus interface, Ethernet interface, control for external ROM and peripherals, DMA with scatter-gather support, serial ports, IIC interface, and general purpose I/O.

Technology: IBM CMOS SA12E 0.25 µm (0.18 µm L_{eff})

Package: 456-ball (35mm or 27mm), or 413-ball (25mm) enhanced plastic ball grid array (E-PBGA)

Power (estimated): Typical 1.5W, Maximum 2.0W

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Figures

Ordering, PVR, and JTAG Information

Product Name	Order Part Number[1]	Processor Frequency	Package	Rev Level	PVR Value	JTAG ID
PPC405GP	IBM25PPC405GP-3BD200C	200MHz	35mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP3BD200CZ	200MHz	35mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP-3DD200C	200MHz	27mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP3DD200CZ	200MHz	27mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP-3ED200C	200MHz	25mm, 413 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP3ED200CZ	200MHz	25mm, 413 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP-3BD266C	266MHz	35mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP3BD266CZ	266MHz	35mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP-3DD266C	266MHz	27mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP3DD266CZ	266MHz	27mm, 456 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP-3ED266C	266MHz	25mm, 413 E-PBGA	D	0x401100C4	0x22050049
PPC405GP	IBM25PPC405GP3ED266CZ	266MHz	25mm, 413 E-PBGA	D	0x401100C4	0x22050049

Note 1: Z at the end of the Order Part Number indicates a tape and reel shipping package. Otherwise, the chips are shipped in a tray.

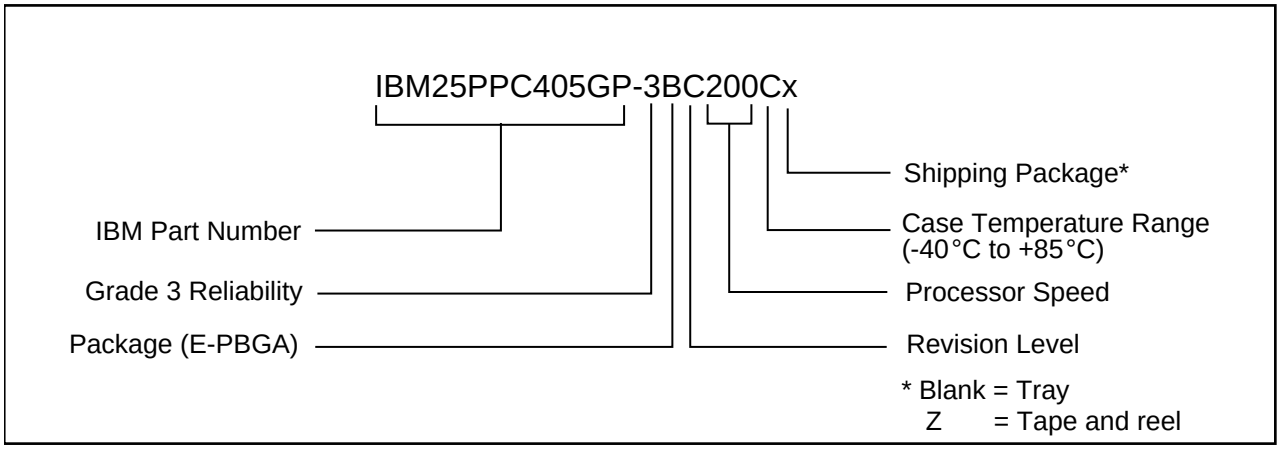
This section provides the part numbering nomenclature for the PPC405GP. For availability, contact your local IBM sales office.

The part number contains a part modifier. This modifier provides for identification of future enhancements (for example, higher performance).

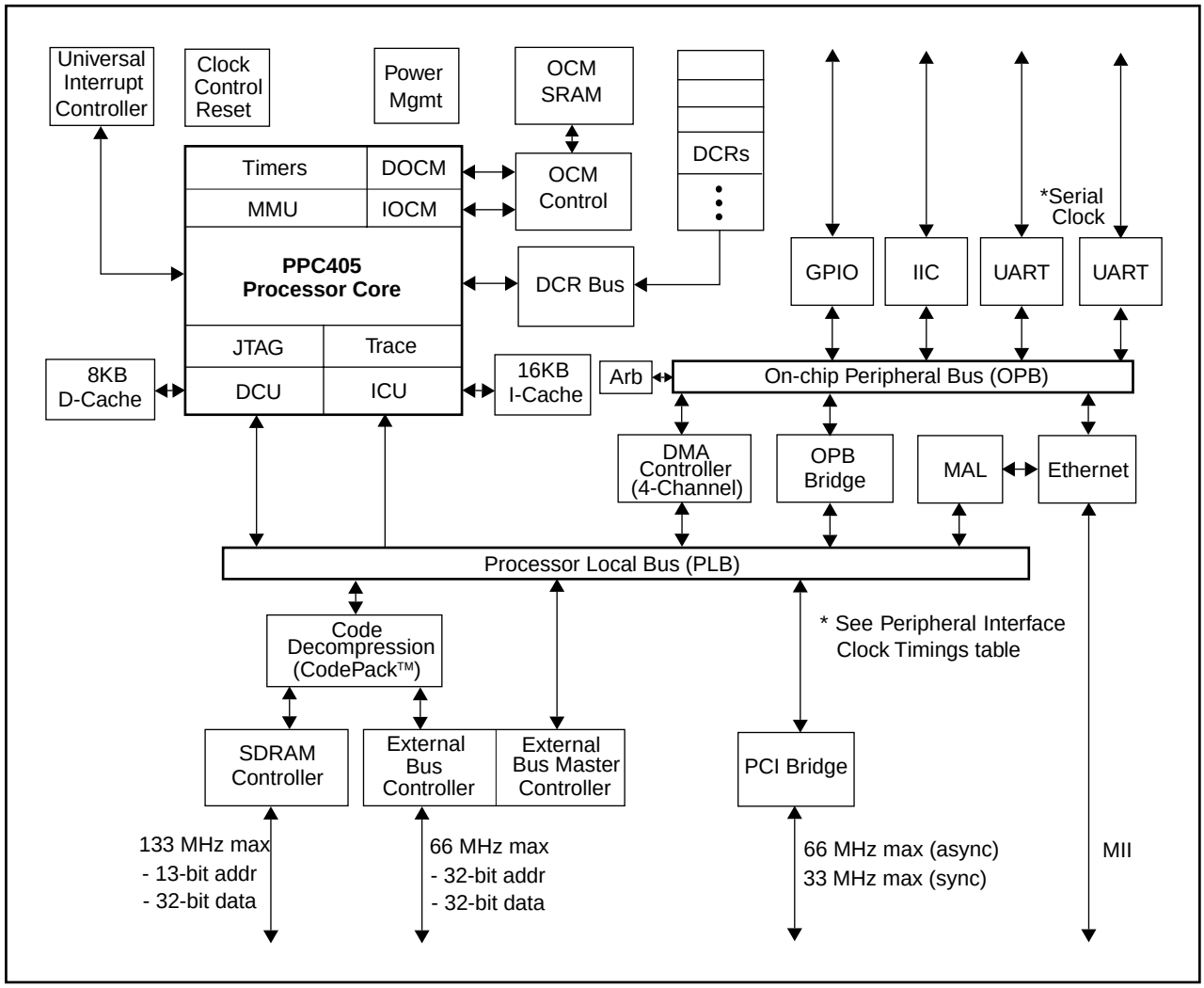
Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

The PVR (Processor Version Register) is software accessible and contains additional information about the revision level of the part. Refer to the PPC405GP User's Manual for details on the register content.

IBM Part Number Key



PPC405GP Embedded Controller Functional Block Diagram



The PPC405GP is designed using the IBM Microelectronics Blue Logic™ methodology in which major functional blocks are integrated together to create an application-specific ASIC product. This approach provides a consistent way to create complex ASICs using IBM CoreConnect™ Bus Architecture.

Note: IBM CoreConnect busses provide:

- 64-bit PLB interfaces up to 133MHz
- 32-bit OPB interfaces up to 66MHz

Address Map Support

The PPC405GP incorporates two simple and separate address maps. The first is a fixed processor address map that serves the PowerPC family of processors. This address map defines the possible contents of various address regions which the processor can access. The second address map is for Device Configuration Registers (DCR). This address map is accessed by software running on the PPC405GP processor through the use of MTDCR and MFDCR commands.

SysMem Memory Address Map 4GB System Memory

Function	Sub Function	Start Address	End Address	Size
Local Memory/Peripherals[1]		00000000	7FFFFFFF	2GB
PCI	Total	80000000	EF5FFFFF	1.74GB
	PCI Memory	80000000	E7FFFFFF	1.63GB
	PCI I/O	E8000000	E800FFFF	64KB
	Reserved	E8010000	E87FFFFF	
	PCI I/O	E8800000	EBFFFFFF	56MB
	Reserved	EC000000	EEBFFFFF	
	PCI Configuration Registers	EEC00000	EEC00007	8B
	Reserved	EEC00008	EECFFFFF	
	PCI Interrupt Acknowledge	EED00000	EEDFFFFF	1MB
	Reserved	EEE00000	EF3FFFFF	
	PCI local Configuration Registers	EF400000	EF40003F	64B
	Reserved	EF400040	EF5FFFFF	
Internal Peripherals	Total	EF600000	EFFFFFFF	10MB
	UART0	EF600300	EF600307	8B
	Reserved	EF600308	EF6003FF	
	UART1	EF600400	EF600407	8B
	Reserved	EF600408	EF6004FF	
	IIC0	EF600500	EF60051F	32B
	Reserved	EF600520	EF6005FF	
	OPB Arbiter	EF600600	EF60063F	64B
	Reserved	EF600640	EF6006FF	
	GPIO Controller Registers	EF600700	EF60077F	128B
	Reserved	EF600780	EF6007FF	
	Ethernet Controller Registers	EF600800	EF6008FF	256B
	Reserved	EF600900	EFFFFFFF	.
Expansion ROM[2]		F0000000	FFDFFFFF	254MB
Boot ROM[2, 3]		FFE00000	FFFFFFFF	2MB

Notes:

1. The Local Memory/Peripheral area of the memory map can be configured for SDRAM, ROM or Peripherals.
2. The Boot ROM and Expansion ROM area of the memory map are intended for use by ROM or Flash-type devices. While locating volatile SDRAM and SRAM in this region is supported by the controller it is not recommended that these regions be used for this purpose.
3. When the optional boot from PCI Memory is selected, the PCI Boot ROM address space begins at FFFE 0000 (size is 128KB).

DCR Address Map 4KB Device Configuration Register

Function	Base Address Strap/Parameter	Start Address(0:9)	End Address(0:9)	Size
DCR Address Space[1]		000	3FF	1KW (4KB)[1]
Reserved		000	0OF	16W
Memory Controller Registers	[0:8] = 000001000	010	011	2W
External Bus Controller Registers	[0:8] = 000001001	012	013	2W
Decompression Controller Registers	[0:8] = 000001010	014	015	2W
Reserved		016	017	2W
On-Chip Memory Controller Registers	[0:8] = 000001011	018	01F	8W
Reserved		020	07F	96W
PLB Registers	[0:5] = 000100	080	08F	16W
Reserved		090	09F	16W
OPB Bridge Out Registers	[0:6] = 000110 0	0A0	0A7	8W
Reserved		0A8	0AF	8W
Clock, Control and Reset	parm=0x0B0	0B0	0B7	8W
Power Management	parm=0x0B8	0B8	0BF	8W
Interrupt Controller	parm=0x0C0	0C0	0CF	16W
Reserved		0D0	0FF	48W
DMA Controller Registers	[0:3] = 0100	100	13F	64W
Reserved		140	17F	64W
Ethernet MAL Registers	[0:2] = 011	180	1FF	128W
Reserved		200	3FF	512W

Notes:

1. DCR address space is addressable with up to 10 bits (1024 or 1K unique addresses). Each unique address represents a single 32-bit (word) register, or 1 kiloword (KW) (which equals 4 KB).

On-Chip Memory

The On-Chip Memory feature comprises a memory controller and a one-port 4KB static RAM (SRAM) accessed by the processor core.

Features include:

- Low-latency access to critical instructions and data
- Performance identical to cache hits without misses
- Contents change only under program control

PLB to PCI Interface

The PLB to PCI interface core provides a mechanism for connecting PCI devices to the local PowerPC processor and local memory. This interface is compliant with version 2.2 of the PCI Specification.

Features include:

- Internal PCI bus arbiter for up to six external devices at PCI bus speeds up to 66MHz. Internal arbiter use is optional and can be disabled for systems which employ an external arbiter.
- PLB 3.0 Compliant
- PLB bus frequency up to 133MHz
- 64-bit PLB Master
- 32-bit PLB Slave
- PCI bus frequency up to 66MHz
  - Synchronous operation at 1/n fractions of PLB speed (n = 1 to 4) to 33MHz maximum
  - Asynchronous operation from 1/8 PLB frequency to 66MHz maximum
- 32-bit PCI Address/Data Bus
- Power Management:
  - PCI Bus Power Management v1.1 compliant
- Supports 1:1, 2:1, 3:1, 4:1 clock ratios from PLB to PCI
- Buffering between PLB and PCI:
  - PCI Target 64-byte write post buffer
  - PCI Target 96-byte read prefetch buffer
  - PLB Slave 8-byte write post buffer
  - PLB Slave 64-byte read prefetch buffer
- Error tracking/status
- Supports PCI Target side configuration

- Supports processor access to all PCI address spaces:
  - Single-byte PCI I/O reads and writes
  - PCI memory single-beat and prefetch-burst reads and single-beat writes
  - Single-byte PCI configuration reads and writes (type 0 and type 1)
  - PCI interrupt acknowledge
  - PCI special cycle
- Supports PCI target access to all PLB address spaces
- Supports PowerPC processor boot from PCI memory

SDRAM Memory Controller

The PPC405GP Memory Controller core provides a low latency access path to SDRAM memory. A variety of system memory configurations are supported. The memory controller supports up to four logical banks. Up to 256 MB per bank are supported, up to a maximum of 1 GB. Memory timings, address and bank sizes, and memory addressing modes are programmable.

Features include:

- 11x8 to 13x11 addressing for SDRAM (2- and 4-bank)
- Memory bus operates at same frequency as PLB
- 32-bit memory interface support
- Programmable address compare for each bank of memory
  - 4 GB of address space
- Industry standard 168-pin DIMMS are supported (some configurations)
- Up to 133 MHz Memory, includes PC133 support
- 4 MB to 256 MB per bank
- Programmable address mapping and timing
- Auto refresh
- Page Mode Accesses with up to 4 open pages
- Sync DRAM configuration via mode set command
- Power Management (self-refresh)
- Error Checking and Correction (ECC) support
  - Standard SEC/DED coverage
  - Aligned nibble error detect
  - Address error logging

- Mixed ECC/non-ECC banks
- Bypass mode

External Peripheral Bus Controller (EBC)

- Up to eight ROM, EPROM, SRAM, Flash, and Slave Peripheral I/O banks supported
- Up to 66 MHz operation
- Burst and non-burst devices
- 8-, 16-, 32-bit byte-addressable data bus width support
- Latch data on Ready, Synchronous or Asynchronous
- Programmable 2K clock time-out counter with disable for Ready
- Programmable access timing per device
  - 256 Wait States for non-burst
  - 32 Burst Wait States for first access and up to 8 Wait States for subsequent accesses
  - Programmable CSon, CSoff relative to address
  - Programmable OEon, WEon, WEoff (1 to 4 clock cycles) relative to CS
- Programmable address mapping
- Peripheral Device pacing with external “Ready”
- External master interface
  - Write posting from external master
  - Read prefetching on PLB for external master reads
  - Bursting capable from external master
  - Allows external master access to all non-EBC PLB slaves
  - External master can control EBC slaves for own access and control

DMA Controller

- Supports the following transfers:
  - Memory-to-memory transfers
  - Buffered peripheral to memory transfers
  - Buffered memory to peripheral transfers
- Four channels
- Scatter/Gather capability for programming multiple DMA operations
- 8-, 16-, 32-bit peripheral support (OPB and external)

- 32-bit addressing
- Address increment or decrement
- Internal 32-byte data buffering capability
- Supports internal and external peripherals
- Support for memory mapped peripherals
- Support for peripherals running on slower frequency buses

UART

- One 8-pin UART and one 4-pin UART interface provided
- Selectable internal or external serial clock to allow wide range of baud rates
- Register compatibility with NS16550 register set
- Complete status reporting capability
- Transmitter and receiver are each buffered with16-byte FIFOs when in FIFO mode
- Fully programmable serial-interface characteristics
- Supports DMA using internal DMA engine

IIC Bus Interface

- Compliant with Phillips® Semiconductors I^2C Specification, dated 1995
- Operation at 100kHz or 400kHz
- 8-bit data
- 10- or 7-bit address
- Slave transmitter and receiver
- Master transmitter and receiver
- Multiple bus masters
- Supports fixed V_{DD} IIC interface
- Two independent 4 x 1 byte data buffers
- Twelve memory-mapped, fully programmable configuration registers
- One programmable interrupt request signal
- Provides full management of all IIC bus protocol
- Programmable error recovery

General Purpose IO (GPIO) Controller

- Controller functions and GPIO registers are programmed and accessed via memory-mapped OPB bus master accesses
- All GPIOs are pin-shared with other functions. DCRs control whether a particular pin that has GPIO capabilities acts as a GPIO or is used for another purpose. Twenty-three GPIOs are multiplexed with:
  - 7 of 8 chip selects
  - All seven external interrupts
  - All nine instruction trace pins
- Each GPIO output is separately programmable to emulate an open-drain driver (i.e., drives to zero, three-stated if output bit is 1)

Universal Interrupt Controller (UIC)

The Universal Interrupt Controller (UIC) provides the control, status, and communications necessary between the various sources of interrupts and the local PowerPC processor.

Features include:

- Supports 7 external and 19 internal interrupts
- Edge triggered or level-sensitive
- Positive or negative active
- Non-critical or critical interrupt to PPC405 processor core
- Programmable critical interrupt priority ordering
- Programmable critical interrupt vector for faster vector processing

10/100 Mbps Ethernet MAC

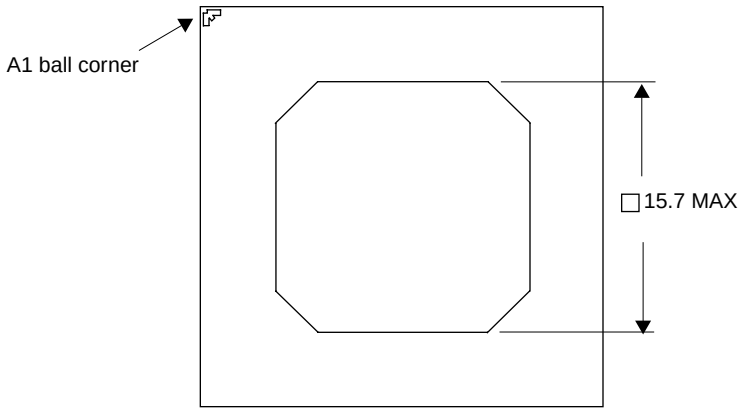
- Capable of handling full/half duplex 100 Mbps and 10 Mbps operation
- Uses the Medium Independent Interface (MII) to the physical layer (PHY not included on chip)

JTAG

- IEEE 1149.1 Test Access Port
- IBM RISCWatch Debugger support
- JTAG Boundary Scan Description Language (BSDL)

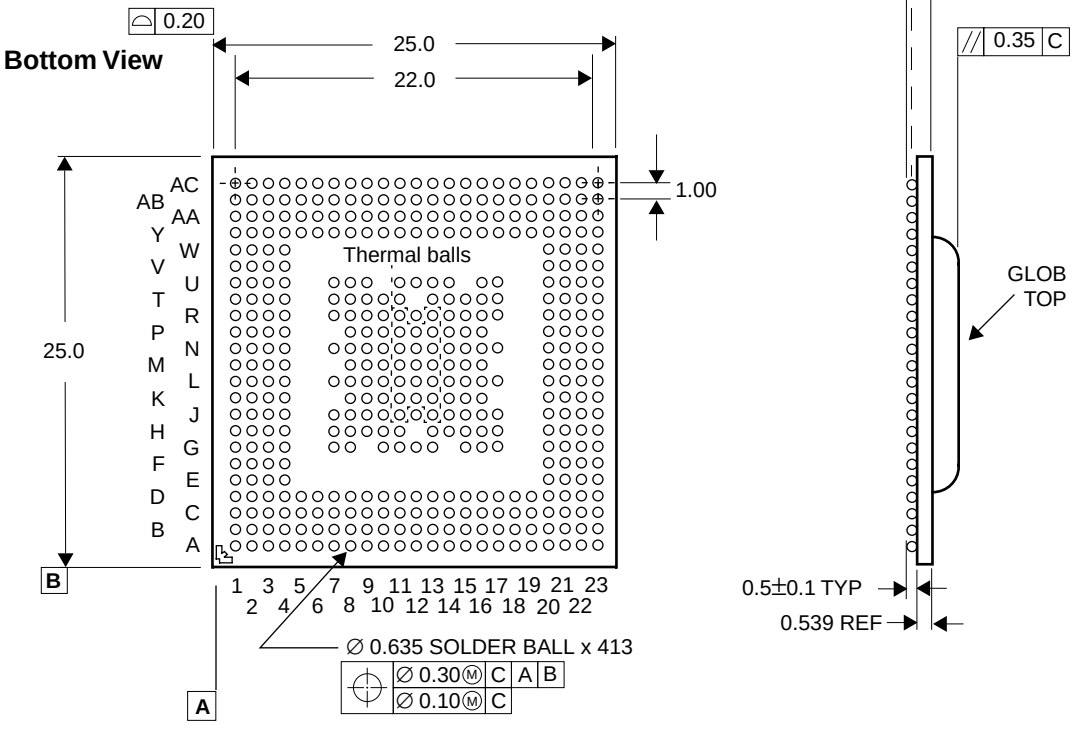
25mm, 413-Ball E-PBGA Package

Top View

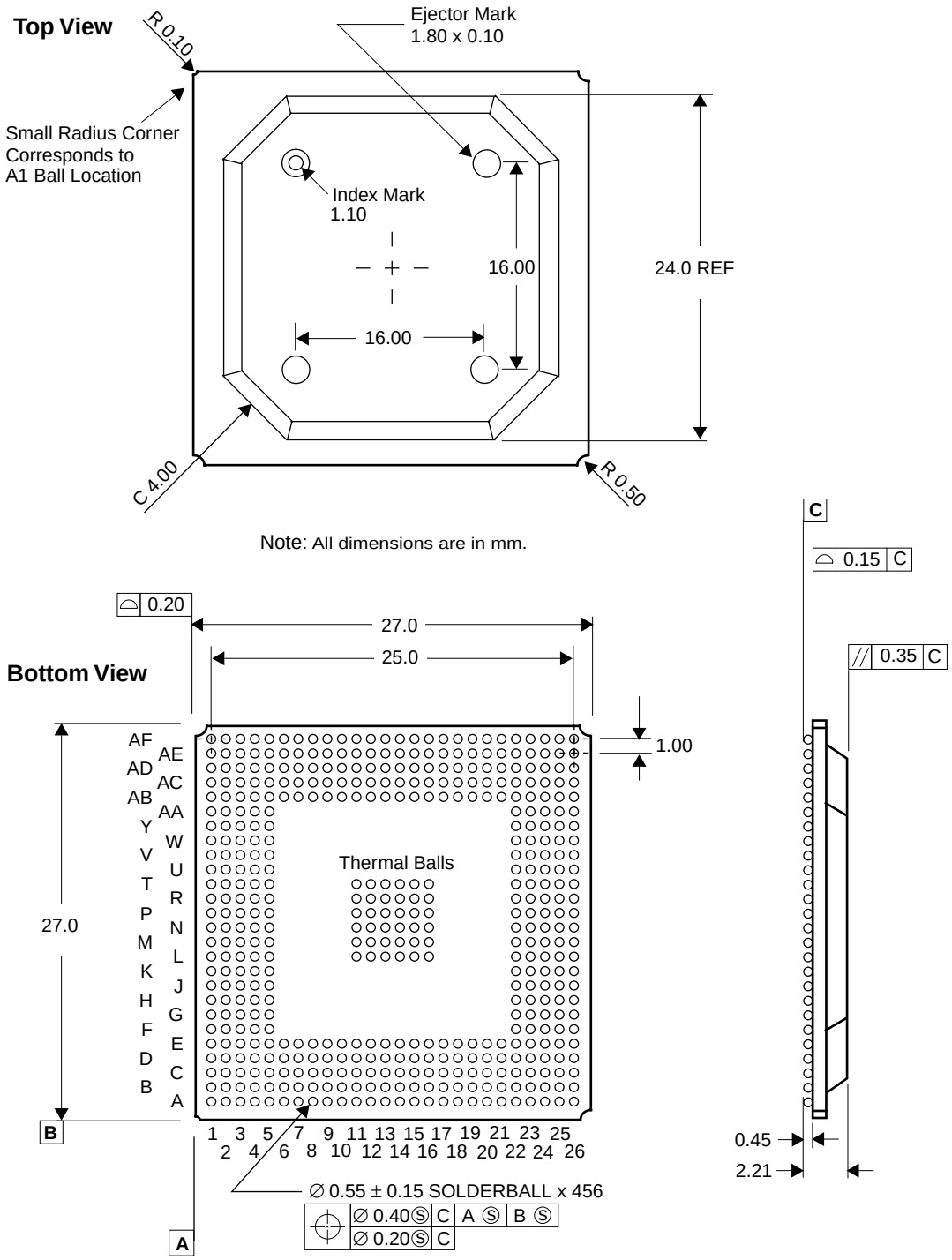


Note: All dimensions are in mm.

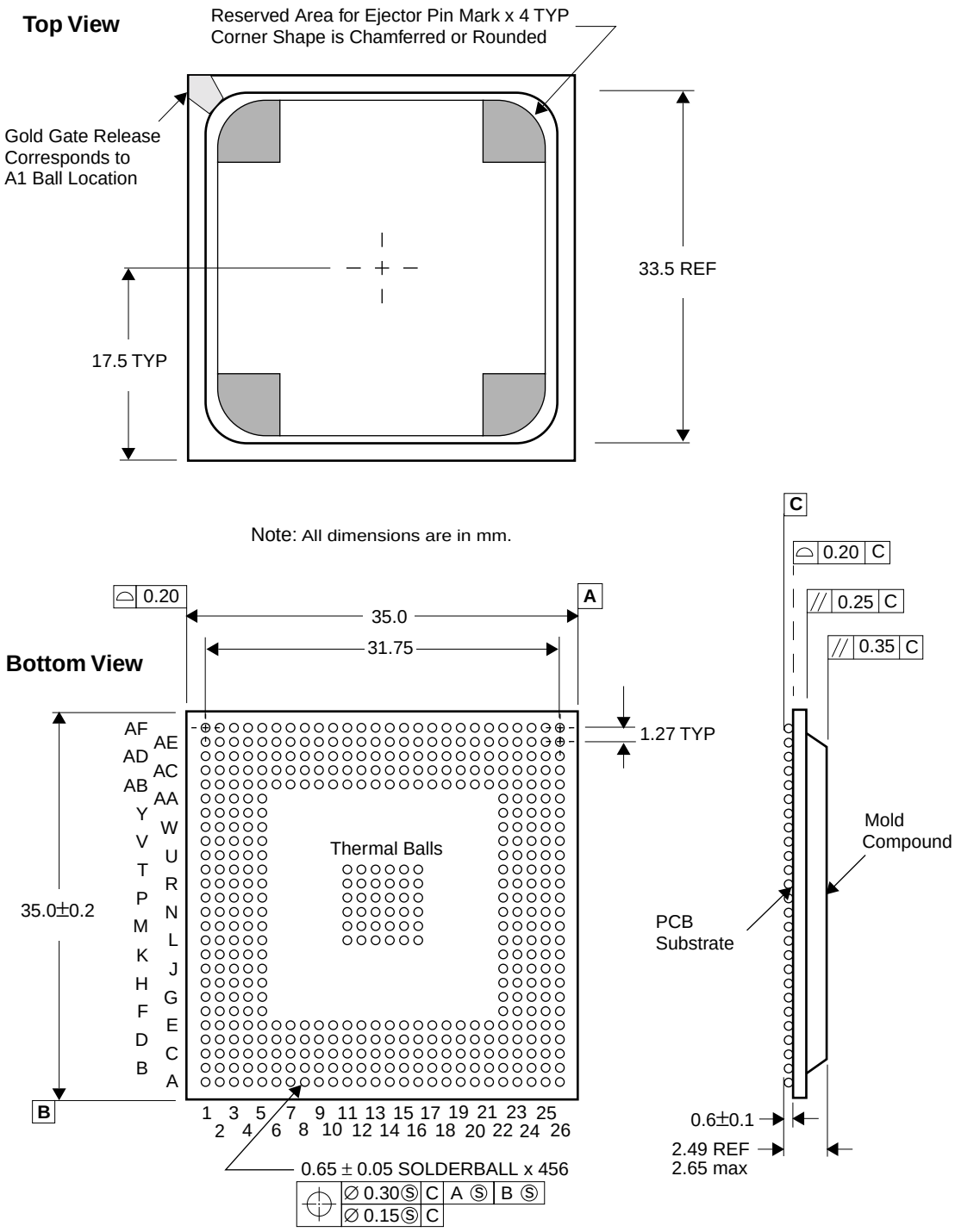
Bottom View



27 mm, 456-Ball E-PBGA Package



35mm, 456-Ball E-PBGA Package



Pin Lists

The PPC405GP embedded controller is available as a 456-ball or a 413-ball E-PBGA package. The 456-ball package is available in two sizes—35 millimeters and 27 millimeters. The 413-ball package size is 25 millimeters. In this section there are three tables that correlate the external signals to the physical package pin (ball) on which they appear.

The following table lists all the external signals in alphabetical order and shows the ball number on which the signal appears. Multiplexed signals are shown as a signal name followed by a second signal name in brackets. The page number listed gives the page in “Signal Functional Description” on page 33 where the signals in the indicated interface group begin.

Signals Listed Alphabetically (Part 1 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
AV_{DD}	L21	D25	System	43
BA0 BA1	N16 N17	AB24 AC24	SDRAM	36
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	AC19 AB17 AC17 AB14	AD17 AF17 AE15 AC14	SDRAM	36
$\overline{\text{BE0}}$[PCIC0] $\overline{\text{BE1}}$[PCIC1] $\overline{\text{BE2}}$[PCIC2] $\overline{\text{BE3}}$[PCIC3]	D16 C22 E23 P23	D19 F24 K24 R26	PCI	33
BusReq	T1	R3	External MASTER Peripheral	41
$\overline{\text{CAS}}$	R15	AB23	SDRAM	36
ClkEn0 ClkEn1	AB22 Y20	AB25 AC25	SDRAM	36
DMAAck0 DMAAck1 DMAAck2 DMAAck3	A17 B14 A15 A8	D16 B15 B14 C12	External SLAVE Peripheral	38
DMAReq0 DMAReq1 DMAReq2 DMAReq3	C13 A16 B9 C6	C16 D14 C11 A7	External SLAVE Peripheral	38
DQM0 DQM1 DQM2 DQM3	U12 AC5 AC2 AA2	AC12 AC10 AC6 AA3	SDRAM	36
DQMCB	AB13	AC15	SDRAM F	36
DrvrInh1 DrvrInh2	H17 G17	E24 E23	System	43
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	AA12 AC15 AB12 AC14 AC12 AC10 AC9 AB11	AE14 AF15 AF14 AD13 AF13 AF12 AE13 AD12	SDRAM	36
EMCMDClk	J20	H24	Ethernet	35
EMCMDIO[PHYMDIO]	T17	AD26	Ethernet	35

Signals Listed Alphabetically (Part 2 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
EMCTxD0 EMCTxD1 EMCTxD2 EMCTxD3	F22 K21 J22 R23	J26 L25 L24 P25	Ethernet	35
EMCTxEn	J21	K23	Ethernet	35
EMCTxErr	K20	K25	Ethernet	35
EOT0[TC0] EOT1[TC1] EOT2[TC2] EOT3[TC3]	C2 G4 U3 V3	F3 G2 V2 Y1	External SLAVE Peripheral	38
$\overline{\text{ExtAck}}$	U4	Y3	External MASTER Peripheral	41
$\overline{\text{ExtReq}}$	V4	Y4	External MASTER Peripheral	41
$\overline{\text{ExtReset}}$	R2	T3	External MASTER Peripheral	41
GND	A1 A6 A18 A23 C14 D14 F1 F23 J11 J13 K11-K13 L1 L4 L11-L13 M4 M11-M13 M20 N11-N13 N20 N23 P11-P13 R11 R13 V1 V23 Y10 AA10 AC1 AC6 AC18 AC23	A1 A2 A6 A11 A16 A19[1] A21 A26 B2 B25 B26 C3 C24 D4 D23 E5 E9 E13 E14 E18 E22 F1 F26 H1[1] J5 J22 L1 L11-L16 L26 M11-M16 N5 N11-N16 N22 P5 P11-P16 P22 R11-R16 T1 T11-T16 T26 V5 V22 W26[1] AA1 AA26 AB5	Ground **Notes:** 1. Reserved on 27mm package. GND on 35mm package. 2. On the 456-ball packages, L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls. 3. On the 413-ball package, J11, J13, K11-K13, L11-L13, M11-N13 , N11-N13, P11-P13, R11, and R13 are also thermal balls.	44

Signals Listed Alphabetically (Part 3 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
GND		AB9 AB13 AB14 AB18 AB22 AC4 AC23 AD3 AD24 AE1 AE2 AE25 AF1 AF6 AF8[1] AF11 AF16 AF21 AF25 AF26	Ground **Notes:** 1. Reserved on 27mm package. GND on 35mm package. 2. On the 456-ball packages, L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls. 3. On the 413-ball package, J11, J13, K11-K13, L11-L13, M11-N13 , N11-N13, P11-P13, R11, and R13 are also thermal balls.	44
$\overline{\text{Gnt}}$[$\overline{\text{PCIReq0}}$]	D15	C19	PCI	33
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]	A20 C19 A21 AB18 AC4 AB4 AC3 Y6 T7	D18 C20 A22 AF18 AC9 AE8 AF5 AC7 AB3	System	43
GPIO10[$\overline{\text{PerCS1}}$] GPIO11[$\overline{\text{PerCS2}}$] GPIO12[$\overline{\text{PerCS3}}$] GPIO13[$\overline{\text{PerCS4}}$] GPIO14[$\overline{\text{PerCS5}}$] GPIO15[$\overline{\text{PerCS6}}$] GPIO16[$\overline{\text{PerCS7}}$]	H11 G8 D5 C7 D10 B6 C10	C4 C5 A4 B9 B10 A9 B11	System	43
GPIO17[IRQ0] GPIO18[IRQ1] GPIO19[IRQ2] GPIO20[IRQ3] GPIO21[IRQ4] GPIO22[IRQ5] GPIO23[IRQ6]	U21 Y23 R20 Y22 W21 U20 AA22	V25 V23 W24 W25 Y24 Y25 AA24	System	43
$\overline{\text{Halt}}$	AA23	AB26	System	43
HoldAck	P4	U2	External MASTER Peripheral	41
HoldPri	P3	T2	External MASTER Peripheral	41
HoldReq	V2	V1	External MASTER Peripheral	41
IICSCL	AB3	AD6	Internal Peripheral	41
IICSDA	Y7	AE7	Internal Peripheral	41
IRQ0[GPIO17] IRQ1[GPIO18] IRQ2[GPIO19] IRQ3[GPIO20] IRQ4[GPIO21] IRQ5[GPIO22] IRQ6[GPIO23]	U21 Y23 R20 Y22 W21 U20 AA22	V25 V23 W24 W25 Y24 Y25 AA24	Interrupts	42

Signals Listed Alphabetically (Part 4 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
MemAddr0	AA21	AE22		
MemAddr1	AC22	AC21		
MemAddr2	AA20	AE21		
MemAddr3	AB21	AD21		
MemAddr4	AA19	AF22		
MemAddr5	AB20	AE20		
MemAddr6	AC21	AC19	SDRAM	36
MemAddr7	Y16	AE19		
MemAddr8	Y15	AD19		
MemAddr9	AB19	AC18		
MemAddr10	AC20	AF19		
MemAddr11	AA16	AD18		
MemAddr12	AA15	AC17		
MemClkOut0	W20	AC26	SDRAM	36
MemClkOut1	AB23	AA23		
MemData0	AC8	AC13		
MemData1	AB10	AE12		
MemData2	AA11	AD11		
MemData3	AC7	AC11		
MemData4	AB7	AF10		
MemData5	AB9	AE11		
MemData6	AB8	AD10		
MemData7	AB6	AF9		
MemData8	AA9	AD9		
MemData9	AA7	AE9		
MemData10	Y9	AD8		
MemData11	AA6	AF7		
MemData12	Y8	AC8		
MemData13	AA5	AD7		
MemData14	AA4	AE6		
MemData15	AB2	AE5	SDRAM	36
MemData16	Y4	AE4		
MemData17	T11	AD5		
MemData18	U11	AD4		
MemData19	R9	AC5		
MemData20	M9	AD1		
MemData21	AA3	AB2		
MemData22	AB1	AA4		
MemData23	Y3	AA2		
MemData24	W3	AB1		
MemData25	Y2	Y2		
MemData26	AA1	W4		
MemData27	T4	W2		
MemData28	R4	W3		
MemData29	W2	V4		
MemData30	Y1	W1		
MemData31	T3	V3		

Signals Listed Alphabetically (Part 5 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
OV_{DD}	A11 D11 G10 G15 H9 H10 H14 H15 J7 J8 J10 J14 J16 J17 K3 K4 K8 K16 L23 N1 P8 P16 P20 P21 R7 R8 R10 R14 R16 R17 T9 T10 T14 T15 U9 U14 Y13 AC13	B17[1] C13[1] E6 E7 E8 E19 E20 E21 F5 F22 G5 G22 H5 H22 K2[1] N24[1] P3[1] U25[1] W5 W22 Y5 Y22 AA5 AA22 AB6 AB7 AB8 AB19 AB20 AB21 AD14[1] AE10[1]	Output driver voltage **Notes:** 1. Reserved on 27mm package. OV_{DD} on 35mm package.	44

Signals Listed Alphabetically (Part 6 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
PCIAD0	B17	A17	PCI	33
PCIAD1	B15	B16		
PCIAD2	B16	C17		
PCIAD3	B18	A18		
PCIAD4	A19	D17		
PCIAD5	C15	C18		
PCIAD6	C17	B18		
PCIAD7	C18	A20		
PCIAD8	C20	B21		
PCIAD9	D19	A23		
PCIAD10	A22	D21		
PCIAD11	B22	B22		
PCIAD12	D20	B23		
PCIAD13	H13	C22		
PCIAD14	M15	C26		
PCIAD15	D21	F25		
PCIAD16	G22	K26		
PCIAD17	H22	L23		
PCIAD18	G23	M25		
PCIAD19	L22	M23		
PCIAD20	M21	N25		
PCIAD21	J23	M26		
PCIAD22	M22	N26		
PCIAD23	K23	P24		
PCIAD24	N22	R24		
PCIAD25	M16	R23		
PCIAD26	T23	P23		
PCIAD27	P22	R25		
PCIAD28	N21	T24		
PCIAD29	U22	U26		
PCIAD30	R22	T25		
PCIAD31	V22	V26		
PCIC0[$\overline{BE0}$]	D16	D19	PCI	33
PCIC1[$\overline{BE1}$]	C22	F24		
PCIC2[$\overline{BE2}$]	E23	K24		
PCIC3[$\overline{BE3}$]	P23	R26		
PCIClk	D17	B20	PCI	33
$\overline{PCIDevSel}$	H20	H25	PCI	33
$\overline{PCIFrame}$	H21	J24	PCI	33
$\overline{PCIGnt0}$[$\overline{Req}$]	W23	U23	PCI	33
$\overline{PCIGnt1}$	U23	T23		
$\overline{PCIGnt2}$	B23	F23		
$\overline{PCIGnt3}$	D23	H26		
$\overline{PCIGnt4}$	K22	N23		
$\overline{PCIGnt5}$	H23	M24		
PCIIDSel	M23	P26	PCI	33
$\overline{PCIINT}$[$\overline{PerWE}$]	G13	C23	PCI	33
$\overline{PCIIRDY}$	E22	J23	PCI	33
PCIParity	E21	E26	PCI	33
$\overline{PCIPErr}$	D22	G25	PCI	33
$\overline{PCIReq0}$[$\overline{Gnt}$]	D15	C19	PCI	33
$\overline{PCIReq1}$	B21	C21		
$\overline{PCIReq2}$	B20	B19		
$\overline{PCIReq3}$	G16	A24		
$\overline{PCIReq4}$	F20	G23		
$\overline{PCIReq5}$	G21	J25		
$\overline{PCIReset}$	K14	B24	PCI	33
$\overline{PCISErr}$	G20	G24	PCI	33

Signals Listed Alphabetically (Part 7 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
PCIStop	C23	H23	PCI	33
PCITRDY	F21	G26	PCI	33
PerAddr0	G7	D5	External SLAVE Peripheral **Note:** PerAddr0 is the most significant bit (msb) on this bus.	38
PerAddr1	J12	A3		
PerAddr2	C11	B4		
PerAddr3	C3	B5		
PerAddr4	A2	D6		
PerAddr5	C4	B6		
PerAddr6	B3	C6		
PerAddr7	D6	D7		
PerAddr8	C5	A5		
PerAddr9	B4	B7		
PerAddr10	D7	C7		
PerAddr11	A3	D8		
PerAddr12	D8	B8		
PerAddr13	D9	C8		
PerAddr14	B5	D9		
PerAddr15	A4	A8		
PerAddr16	C8	C9		
PerAddr17	C9	D10		
PerAddr18	A5	C10		
PerAddr19	B7	A10		
PerAddr20	B8	D11		
PerAddr21	A7	B12		
PerAddr22	B10	D13		
PerAddr23	B11	D12		
PerAddr24	C12	B13		
PerAddr25	A9	A12		
PerAddr26	B12	A13		
PerAddr27	A10	C14		
PerAddr28	A12	A14		
PerAddr29	A14	A15		
PerAddr30	B13	C15		
PerAddr31	G12	D15		
PerBLast	D3	F2	External SLAVE Peripheral	38
PerClk	J9	E4	External MASTER Peripheral	41
PerCS0	G11	B3	External SLAVE Peripheral	38
PerCS1[GPIO10]	H11	C4		
PerCS2[GPIO11]	G8	C5		
PerCS3[GPIO12]	D5	A4		
PerCS4[GPIO13]	C7	B9		
PerCS5[GPIO14]	D10	B10		
PerCS6[GPIO15]	B6	A9		
PerCS7[GPIO16]	C10	B11		

Signals Listed Alphabetically (Part 8 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31	R3 W1 U2 T2 U1 P2 N2 M3 R1 M2 P1 M1 K1 J1 L2 M8 H1 K2 L3 G1 G2 J2 H2 F2 E1 J3 G3 D1 J4 F3 D2 H4	U4 U3 U1 T4 R2 P4 R4 P2 R1 P1 N3 N1 M1 N2 M3 M4 N4 M2 L3 L4 K1 L2 K3 J1 K4 J3 J2 J4 H3 G1 H2 H4	External SLAVE Peripheral **Note:** PerData0 is the most significant bit (msb) on this bus.	38
PerErr	H8	B1	External MASTER Peripheral	41
$\overline{\text{PerOE}}$	K10	C2	External SLAVE Peripheral	38
PerPar0 PerPar1 PerPar2 PerPar3	L7 F4 E3 C1	D3 G4 G3 E1	External SLAVE Peripheral	38
PerReady	L8	E3	External SLAVE Peripheral	38
PerR/$\overline{\text{W}}$	H7	C1	External SLAVE Peripheral	38
$\overline{\text{PerWBE0}}$ $\overline{\text{PerWBE1}}$ $\overline{\text{PerWBE2}}$ $\overline{\text{PerWBE3}}$	D4 B2 B1 E4	D2 E2 F4 D1	External SLAVE Peripheral	38
$\overline{\text{PerWE}}$[$\overline{\text{PCIINT}}$]	G13	C23	PCI	33
PHYCol	Y21	AA25	Ethernet	35
PHYCrS	T20	W23	Ethernet	35
PHYRxClk	AA18	AF20	Ethernet	35
PHYMDIO[EMCMDIO]	T17	AD26	Ethernet	35
PHYRxD0 PHYRxD1 PHYRxD2 PHYRxD3	AA13 Y19 Y18 Y17	AE23 AF23 AC20 AD20	Ethernet	35
PHYRxDV	R21	V24	Ethernet	35
PHYRxErr	T22	U24	Ethernet	35
PHYTxClk	C21	E25	Ethernet	35

Signals Listed Alphabetically (Part 9 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
$\overline{RAS}$	R12	AF24	SDRAM	36
RcvrInh	L17	C25	System	43
$\overline{Req}$[$\overline{PCIGnt0}$]	W23	U23	PCI	33
Reserved	B19 C16 D18 E2 H3 T21 V20 V21 W22 Y5[1] AA8 AB5	A19[2] B17[3] C13[3] D20 H1[2] K2[3] N24[3] P3[3] U25[3] W26[2] Y23 Y26 AF4[1] AF8[2] AD14[3] AE10[3]	Other **Notes:** 1. Y5 (on the 413-ball package) and AF4 must be tied to OV_{DD} or GND. All other reserved pins should be left unconnected. 2. Reserved on 27mm package. GND on 35mm package. 3. Reserved on 27mm package. OV_{DD} on 35mm package.	44
SysClk	H16	A25	System	43
SysErr	P14	AD25	System	43
$\overline{SysReset}$	J15	D22	System	43
TCK	U16	AD22	JTAG	42
TC0[EOT0] TC1[EOT1] TC2[EOT2] TC3[EOT3]	C2 G4 U3 V3	F3 G2 V2 Y1	External SLAVE Peripheral	38
TDI	U13	AE24	JTAG	42
TDO	T13	AD23	JTAG	42
$\overline{TestEn}$	E20	D26	System	43
TmrClk	L16	D24	System	43
TMS	U17	AC22	JTAG	42
TrcClk[GPIO9]	T7	AB3	System	43
$\overline{TRST}$	T16	AE26	JTAG	42
TS1E[GPIO1] TS2E[GPIO2] TS1O[GPIO3] TS2O[GPIO4] TS3[GPIO5] TS4[GPIO6] TS5[GPIO7] TS6[GPIO8]	A20 C19 A21 AB18 AC4 AB4 AC3 Y6	D18 C20 A22 AF18 AC9 AE8 AF5 AC7		43
$\overline{UART0\_CTS}$	U7	AB4	Internal Peripheral	41
$\overline{UART0\_DCD}$	AA17	AE18	Internal Peripheral	41
$\overline{UART0\_DSR}$	P10	AE3	Internal Peripheral	41
$\overline{UART0\_DTR}$	T8	AF2	Internal Peripheral	41
$\overline{UART0\_RI}$	AC16	AD15	Internal Peripheral	41
$\overline{UART0\_RTS}$	AB15	AD16	Internal Peripheral	41
UART0_Rx	AA14	AE16	Internal Peripheral	41
UART0_Tx	U8	AF3	Internal Peripheral	41

Signals Listed Alphabetically (Part 10 of 10)

Signal Name	413 -Ball	456-Ball	Interface Group	Page
$\overline{\text{UART1\_CTS}}$[$\overline{\text{UART1\_DSR}}$]	N8	AC3	Internal Peripheral	41
$\overline{\text{UART1\_DSR}}$[$\overline{\text{UART1\_CTS}}$]	N8	AC3	Internal Peripheral	41
$\overline{\text{UART1\_DTR}}$[$\overline{\text{UART1\_RTS}}$]	N7	AD2	Internal Peripheral	41
$\overline{\text{UART1\_RTS}}$[$\overline{\text{UART1\_DTR}}$]	N7	AD2	Internal Peripheral	41
UART1_Rx	W4	AC1	Internal Peripheral	41
UART1_Tx	N3	AC2	Internal Peripheral	41
UARTSerClk	Y14	AE17	Internal Peripheral	41
V_{DD}	A13 D12 D13 K9 K15 L9 L10 L14 L15 L20 M10 M14 N4 N9 N10 N14 N15 P9 P15 Y11 Y12 AC11	E10 E11 E12 E15 E16 E17 K5 K22 L5 L22 M5 M22 R5 R22 T5 T22 U5 U22 AB10 AB11 AB12 AB15 AB16 AB17	Logic voltage	44
$\overline{\text{WE}}$	AB16	AC16	SDRAM	36

Signals Listed by Ball Assignment—413-Ball Package (Part 1 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	GND	B17	PCIAD0	D10	PerCS5[GPIO14]	G13	PCIINT[PerWE]
A2	PerAddr4	B18	PCIAD3	D11	OV_{DD}	G15	OV_{DD}
A3	PerAddr11	B19	Reserved	D12	V_{DD}	G16	PCIReq3
A4	PerAddr15	B20	PCIReq2	D13	V_{DD}	G17	DrvrInh2
A5	PerAddr18	B21	PCIReq1	D14	GND	G20	PCISErr
A6	GND	B22	PCIAD11	D15	PCIReq0[Gnt]	G21	PCIReq5
A7	PerAddr21	B23	PCIGnt2	D16	PCIC0[BE0]	G22	PCIAD16
A8	DMAAck3	C1	PerPar3	D17	PCIClk	G23	PCIAD18
A9	PerAddr25	C2	EOT0[TC0]	D18	Reserved	H1	PerData16
A10	PerAddr27	C3	PerAddr3	D19	PCIAD9	H2	PerData22
A11	OV_{DD}	C4	PerAddr5	D20	PCIAD12	H3	Reserved
A12	PerAddr28	C5	PerAddr8	D21	PCIAD15	H4	PerData31
A13	V_{DD}	C6	DMAReq3	D22	PCIPErr	H7	PerR/W
A14	PerAddr29	C7	PerCS4[GPIO13]	D23	PCIGnt3	H8	PerErr
A15	DMAAck2	C8	PerAddr16	E1	PerData24	H9	OV_{DD}
A16	DMAReq1	C9	PerAddr17	E2	Reserved	H10	OV_{DD}
A17	DMAAck0	C10	PerCS7[GPIO16]	E3	PerPar2	H11	PerCS1[GPIO10]
A18	GND	C11	PerAddr2	E4	PerWBE3	H13	PCIAD13
A19	PCIAD4	C12	PerAddr24	E20	TestEn	H14	OV_{DD}
A20	GPIO1[TS1E]	C13	DMAReq0	E21	PCIParity	H15	OV_{DD}
A21	GPIO3[TS1O]	C14	GND	E22	PCIIRDY	H16	SysClk
A22	PCIAD10	C15	PCIAD5	E23	PCIC2[BE2]	H17	DrvInh1
A23	GND	C16	Reserved	F1	GND	H20	PCIDevSel
B1	PerWBE2	C17	PCIAD6	F2	PerData23	H21	PCIFrame
B2	PerWBE1	C18	PCIAD7	F3	PerData29	H22	PCIAD17
B3	PerAddr6	C19	GPIO2[TS2E]	F4	PerPar1	H23	PCIGnt5
B4	PerAddr9	C20	PCIAD8	F20	PCIReq4	J1	PerData13
B5	PerAddr14	C21	PHYTxClk	F21	PCITRDY	J2	PerData21
B6	PerCS6[GPIO15]	C22	PCIC1[BE1]	F22	EMCTxD0	J3	PerData25
B7	PerAddr19	C23	PCIStop	F23	GND	J4	PerData28
B8	PerAddr20	D1	PerData27	G1	PerData19	J7	OV_{DD}
B9	DMAReq2	D2	PerData30	G2	PerData20	J8	OV_{DD}
B10	PerAddr22	D3	PerBLast	G3	PerData26	J9	PerClk
B11	PerAddr23	D4	PerWBE0	G4	EOT1[TC1]	J10	OV_{DD}
B12	PerAddr26	D5	PerCS3[GPIO12]	G7	PerAddr0	J11	GND
B13	PerAddr30	D6	PerAddr7	G8	PerCS2[GPIO11]	J12	PerAddr1
B14	DMAAck1	D7	PerAddr10	G10	OV_{DD}	J13	GND
B15	PCIAD1	D8	PerAddr12	G11	PerCS0	J14	OV_{DD}
B16	PCIAD2	D9	PerAddr13	G12	PerAddr31	J15	SysReset

Signals Listed by Ball Assignment—413-Ball Package (Part 2 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
J16	OV_{DD}	L20	V_{DD}	N22	PCIAD24	T1	BusReq
J17	OV_{DD}	L21	AV_{DD}	N23	GND	T2	PerData3
J20	EMCMDClk	L22	PCIAD19	P1	PerData10	T3	MemData31
J21	EMCTxEn	L23	OV_{DD}	P2	PerData5	T4	MemData27
J22	EMCTxD2	M1	PerData11	P3	HoldPri	T7	GPIO9[TrcClk]
J23	PCIAD21	M2	PerData9	P4	HoldAck	T8	$\overline{\text{UART0\_DTR}}$
K1	PerData12	M3	PerData7	P8	OV_{DD}	T9	OV_{DD}
K2	PerData17	M4	GND	P9	V_{DD}	T10	OV_{DD}
K3	OV_{DD}	M8	PerData15	P10	$\overline{\text{UART0\_DSR}}$	T11	MemData17
K4	OV_{DD}	M9	MemData20	P11	GND	T13	TDO
K8	OV_{DD}	M10	V_{DD}	P12	GND	T14	OV_{DD}
K9	V_{DD}	M11	GND	P13	GND	T15	OV_{DD}
K10	$\overline{\text{PerOE}}$	M12	GND	P14	SysErr	T16	$\overline{\text{TRST}}$
K11	GND	M13	GND	P15	V_{DD}	T17	EMCMDIO [PHYMDIO]
K12	GND	M14	V_{DD}	P16	OV_{DD}	T20	PHYCrS
K13	GND	M15	PCIAD14	P20	OV_{DD}	T21	Reserved
K14	$\overline{\text{PCIReset}}$	M16	PCIAD25	P21	OV_{DD}	T22	PHYRxErr
K15	V_{DD}	M20	GND	P22	PCIAD27	T23	PCIAD26
K16	OV_{DD}	M21	PCIAD20	P23	PCIC3[$\overline{\text{BE3}}$]	U1	PerData4
K20	EMCTxErr	M22	PCIAD22	R1	PerData8	U2	PerData2
K21	EMCTxD1	M23	PCIIDSel	R2	$\overline{\text{ExtReset}}$	U3	EOT2[TC2]
K22	$\overline{\text{PCIGnt4}}$	N1	OV_{DD}	R3	PerData0	U4	$\overline{\text{ExtAck}}$
K23	PCIAD23	N2	PerData6	R4	MemData28	U7	$\overline{\text{UART0\_CTS}}$
L1	GND	N3	UART1_Tx	R7	OV_{DD}	U8	UART0_Tx
L2	PerData14	N4	V_{DD}	R8	OV_{DD}	U9	OV_{DD}
L3	PerData18	N7	$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]	R9	MemData19	U11	MemData18
L4	GND	N8	$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]	R10	OV_{DD}	U12	DQM0
L7	PerPar0	N9	V_{DD}	R11	GND	U13	TDI
L8	PerReady	N10	V_{DD}	R12	$\overline{\text{RAS}}$	U14	OV_{DD}
L9	V_{DD}	N11	GND	R13	GND	U16	TCK
L10	V_{DD}	N12	GND	R14	OV_{DD}	U17	TMS
L11	GND	N13	GND	R15	$\overline{\text{CAS}}$	U20	IRQ5[GPIO22]
L12	GND	N14	V_{DD}	R16	OV_{DD}	U21	IRQ0[GPIO17]
L13	GND	N15	V_{DD}	R17	OV_{DD}	U22	PCIAD29
L14	V_{DD}	N16	BA0	R20	IRQ2[GPIO19]	U23	$\overline{\text{PCIGnt1}}$
L15	V_{DD}	N17	BA1	R21	PHYRxDV	V1	GND
L16	TmrClk	N20	GND	R22	PCIAD30	V2	HoldReq
L17	RcvInh	N21	PCIAD28	R23	EMCTxD3	V3	EOT3[TC3]

Signals Listed by Ball Assignment—413-Ball Package (Part 3 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
V4	$\overline{\text{ExtReq}}$	Y15	MemAddr8	AA19	MemAddr4	AB23	MemClkOut1
V20	Reserved	Y16	MemAddr7	AA20	MemAddr2	AC1	GND
V21	Reserved	Y17	PHYRxD3	AA21	MemAddr0	AC2	DQM2
V22	PCIAD31	Y18	PHYRxD2	AA22	IRQ6[GPIO23]	AC3	GPIO7[TS5]
V23	GND	Y19	PHYRxD1	AA23	$\overline{\text{Halt}}$	AC4	GPIO5[TS3]
W1	PerData1	Y20	ClkEn1	AB1	MemData22	AC5	DQM1
W2	MemData29	Y21	PHYCol	AB2	MemData15	AC6	GND
W3	MemData24	Y22	IRQ3[GPIO20]	AB3	IICSCL	AC7	MemData3
W4	UART1_Rx	Y23	IRQ1[GPIO18]	AB4	GPIO6[TS4]	AC8	MemData0
W20	MemClkOut0	AA1	MemData26	AB5	Reserved	AC9	ECC6
W21	IRQ4[GPIO21]	AA2	DQM3	AB6	MemData7	AC10	ECC5
W22	Reserved	AA3	MemData21	AB7	MemData4	AC11	V_{DD}
W23	$\overline{\text{PCIGnt0[Req]}}$	AA4	MemData14	AB8	MemData6	AC12	ECC4
Y1	MemData30	AA5	MemData13	AB9	MemData5	AC13	OV_{DD}
Y2	MemData25	AA6	MemData11	AB10	MemData1	AC14	ECC3
Y3	MemData23	AA7	MemData9	AB11	ECC7	AC15	ECC1
Y4	MemData16	AA8	Reserved	AB12	ECC2	AC16	$\overline{\text{UART0\_RI}}$
Y5	Reserved	AA9	MemData8	AB13	DQMCB	AC17	$\overline{\text{BankSel2}}$
Y6	GPIO8[TS6]	AA10	GND	AB14	$\overline{\text{BankSel3}}$	AC18	GND
Y7	IICSDA	AA11	MemData2	AB15	$\overline{\text{UART0\_RTS}}$	AC19	$\overline{\text{BankSel0}}$
Y8	MemData12	AA12	ECC0	AB16	$\overline{\text{WE}}$	AC20	MemAddr10
Y9	MemData10	AA13	PHYRxD0	AB17	$\overline{\text{BankSel1}}$	AC21	MemAddr6
Y10	GND	AA14	UART0_Rx	AB18	GPIO4[TS2O]	AC22	MemAddr1
Y11	V_{DD}	AA15	MemAddr12	AB19	MemAddr9	AC23	GND
Y12	V_{DD}	AA16	MemAddr11	AB20	MemAddr5		
Y13	OV_{DD}	AA17	$\overline{\text{UART0\_DCD}}$	AB21	MemAddr3		
Y14	UARTSerClk	AA18	PHYRxClk	AB22	ClkEn0		

Signals Listed by Ball Assignment—456-Ball Package (Part 1 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
A1	GND	B14	DMAAck2	D1	PerWBE3	E14	GND
A2	GND	B15	DMAAck1	D2	PerWBE0	E15	V_{DD}
A3	PerAddr1	B16	PCIAD1	D3	PerPar0	E16	V_{DD}
A4	PerCS3[GPIO12]	B17	Res – 27/OV_{DD} – 35	D4	GND	E17	V_{DD}
A5	PerAddr8	B18	PCIAD6	D5	PerAddr0	E18	GND
A6	GND	B19	PCIReq2	D6	PerAddr4	E19	OV_{DD}
A7	DMAReq3	B20	PCIClk	D7	PerAddr7	E20	OV_{DD}
A8	PerAddr15	B21	PCIAD8	D8	PerAddr11	E21	OV_{DD}
A9	PerCS6[GPIO15]	B22	PCIAD11	D9	PerAddr14	E22	GND
A10	PerAddr19	B23	PCIAD12	D10	PerAddr17	E23	DrvrInh2
A11	GND	B24	PCIReset	D11	PerAddr20	E24	DrvInh1
A12	PerAddr25	B25	GND	D12	PerAddr23	E25	PHYTxClk
A13	PerAddr26	B26	GND	D13	PerAddr22	E26	PCIParity
A14	PerAddr28	C1	PerR/W	D14	DMAReq1	F1	GND
A15	PerAddr29	C2	PerOE	D15	PerAddr31	F2	PerBLast
A16	GND	C3	GND	D16	DMAAck0	F3	EOT0[TC0]
A17	PCIAD0	C4	PerCS1[GPIO10]	D17	PCIAD4	F4	PerWBE2
A18	PCIAD3	C5	PerCS2[GPIO11]	D18	GPIO1[TS1E]	F5	OV_{DD}
A19	Res – 27/GND – 35	C6	PerAddr6	D19	PCIC0[BE0]	F22	OV_{DD}
A20	PCIAD7	C7	PerAddr10	D20	Reserved	F23	PCIGnt2
A21	GND	C8	PerAddr13	D21	PCIAD10	F24	PCIC1[BE1]
A22	GPIO3[TS1O]	C9	PerAddr16	D22	SysReset	F25	PCIAD15
A23	PCIAD9	C10	PerAddr18	D23	GND	F26	GND
A24	PCIReq3	C11	DMAReq2	D24	TmrClk	G1	PerData29
A25	SysClk	C12	DMAAck3	D25	AV_{DD}	G2	EOT1[TC1]
A26	GND	C13	Res – 27/OV_{DD} – 35	D26	TestEn	G3	PerPar2
B1	PerErr	C14	PerAddr27	E1	PerPar3	G4	PerPar1
B2	GND	C15	PerAddr30	E2	PerWBE1	G5	OV_{DD}
B3	PerCS0	C16	DMAReq0	E3	PerReady	G22	OV_{DD}
B4	PerAddr2	C17	PCIAD2	E4	PerClk	G23	PCIReq4
B5	PerAddr3	C18	PCIAD5	E5	GND	G24	PCISErr
B6	PerAddr5	C19	PCIReq0[Gnt]	E6	OV_{DD}	G25	PCIPErr
B7	PerAddr9	C20	GPIO2[TS2E]	E7	OV_{DD}	G26	PCITRDY
B8	PerAddr12	C21	PCIReq1	E8	OV_{DD}	H1	Res – 27/GND – 35
B9	PerCS4[GPIO13]	C22	PCIAD13	E9	GND	H2	PerData30
B10	PerCS5[GPIO14]	C23	PCIINT[PerWE]	E10	V_{DD}	H3	PerData28
B11	PerCS7[GPIO16]	C24	GND	E11	V_{DD}	H4	PerData31
B12	PerAddr21	C25	RcvInh	E12	V_{DD}	H5	OV_{DD}
B13	PerAddr24	C26	PCIAD14	E13	GND	H22	OV_{DD}

Signals Listed by Ball Assignment—456-Ball Package (Part 2 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
H23	PCIStop	M1	PerData12	P14	GND	U1	PerData2
H24	EMCMDClk	M2	PerData17	P15	GND	U2	HoldAck
H25	PCIDevSel	M3	PerData14	P16	GND	U3	PerData1
H26	PCIGnt3	M4	PerData15	P22	GND	U4	PerData0
J1	PerData23	M5	V_{DD}	P23	PCIAD26	U5	V_{DD}
J2	PerData26	M11	GND	P24	PCIAD23	U22	V_{DD}
J3	PerData25	M12	GND	P25	EMCTxD3	U23	PCIGnt0[Req]
J4	PerData27	M13	GND	P26	PCIIDSel	U24	PHYRxErr
J5	GND	M14	GND	R1	PerData8	U25	Res – 27/OV_{DD} – 35
J22	GND	M15	GND	R2	PerData4	U26	PCIAD29
J23	PCIIRDY	M16	GND	R3	BusReq	V1	HoldReq
J24	PCIFrame	M22	V_{DD}	R4	PerData6	V2	EOT2[TC2]
J25	PCIReq5	M23	PCIAD19	R5	V_{DD}	V3	MemData31
J26	EMCTxD0	M24	PCIGnt5	R11	GND	V4	MemData29
K1	PerData20	M25	PCIAD18	R12	GND	V5	GND
K2	Res – 27/OV_{DD} – 35	M26	PCIAD21	R13	GND	V22	GND
K3	PerData22	N1	PerData11	R14	GND	V23	IRQ1[GPIO18]
K4	PerData24	N2	PerData13	R15	GND	V24	PHYRxDV
K5	V_{DD}	N3	PerData10	R16	GND	V25	IRQ0[GPIO17]
K22	V_{DD}	N4	PerData16	R22	V_{DD}	V26	PCIAD31
K23	EMCTxEn	N5	GND	R23	PCIAD25	W1	MemData30
K24	PCIC2[BE2]	N11	GND	R24	PCIAD24	W2	MemData27
K25	EMCTxErr	N12	GND	R25	PCIAD27	W3	MemData28
K26	PCIAD16	N13	GND	R26	PCIC3[BE3]	W4	MemData26
L1	GND	N14	GND	T1	GND	W5	OV_{DD}
L2	PerData21	N15	GND	T2	HoldPri	W22	OV_{DD}
L3	PerData18	N16	GND	T3	ExtReset	W23	PHYCrS
L4	PerData19	N22	GND	T4	PerData3	W24	IRQ2[GPIO19]
L5	V_{DD}	N23	PCIGnt4	T5	V_{DD}	W25	IRQ3[GPIO20]
L11	GND	N24	Res – 27/OV_{DD} – 35	T11	GND	W26	Res – 27/GND – 35
L12	GND	N25	PCIAD20	T12	GND	Y1	EOT3[TC3]
L13	GND	N26	PCIAD22	T13	GND	Y2	MemData25
L14	GND	P1	PerData9	T14	GND	Y3	ExtAck
L15	GND	P2	PerData7	T15	GND	Y4	ExtReq
L16	GND	P3	Res – 27/OV_{DD} – 35	T16	GND	Y5	OV_{DD}
L22	V_{DD}	P4	PerData5	T22	V_{DD}	Y22	OV_{DD}
L23	PCIAD17	P5	GND	T23	PCIGnt1	Y23	Reserved
L24	EMCTxD2	P11	GND	T24	PCIAD28	Y24	IRQ4[GPIO21]
L25	EMCTxD1	P12	GND	T25	PCIAD30	Y25	IRQ5[GPIO22]
L26	GND	P13	GND	T26	GND	Y26	Reserved

Signals Listed by Ball Assignment—456-Ball Package (Part 3 of 3)

Ball	Signal Name	Ball	Signal Name	Ball	Signal Name	Ball	Signal Name
AA1	GND	AB26	$\overline{\text{Halt}}$	AD9	MemData8	AE18	$\overline{\text{UART0\_DCD}}$
AA2	MemData23	AC1	UART1_Rx	AD10	MemData6	AE19	MemAddr7
AA3	DQM3	AC2	UART1_Tx	AD11	MemData2	AE20	MemAddr5
AA4	MemData22	AC3	$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]	AD12	ECC7	AE21	MemAddr2
AA5	OV_{DD}	AC4	GND	AD13	ECC3	AE22	MemAddr0
AA22	OV_{DD}	AC5	MemData19	AD14	Res – 27/OV_{DD} – 35	AE23	PHYRxD0
AA23	MemClkOut1	AC6	DQM2	AD15	$\overline{\text{UART0\_RI}}$	AE24	TDI
AA24	IRQ6[GPIO23]	AC7	GPIO8[TS6]	AD16	$\overline{\text{UART0\_RTS}}$	AE25	GND
AA25	PHYCol	AC8	MemData12	AD17	$\overline{\text{BankSel0}}$	AE26	$\overline{\text{TRST}}$
AA26	GND	AC9	GPIO5[TS3]	AD18	MemAddr11	AF1	GND
AB1	MemData24	AC10	DQM1	AD19	MemAddr8	AF2	$\overline{\text{UART0\_DTR}}$
AB2	MemData21	AC11	MemData3	AD20	PHYRxD3	AF3	UART0_Tx
AB3	GPIO9[TrcClk]	AC12	DQM0	AD21	MemAddr3	AF4	Reserved
AB4	$\overline{\text{UART0\_CTS}}$	AC13	MemData0	AD22	TCK	AF5	GPIO7[TS5]
AB5	GND	AC14	$\overline{\text{BankSel3}}$	AD23	TDO	AF6	GND
AB6	OV_{DD}	AC15	DQMCB	AD24	GND	AF7	MemData11
AB7	OV_{DD}	AC16	$\overline{\text{WE}}$	AD25	SysErr	AF8	Res – 27/GND – 35
AB8	OV_{DD}	AC17	MemAddr12	AD26	EMCMDIO [PHYMDIO]	AF9	MemData7
AB9	GND	AC18	MemAddr9	AE1	GND	AF10	MemData4
AB10	V_{DD}	AC19	MemAddr6	AE2	GND	AF11	GND
AB11	V_{DD}	AC20	PHYRxD2	AE3	$\overline{\text{UART0\_DSR}}$	AF12	ECC5
AB12	V_{DD}	AC21	MemAddr1	AE4	MemData16	AF13	ECC4
AB13	GND	AC22	TMS	AE5	MemData15	AF14	ECC2
AB14	GND	AC23	GND	AE6	MemData14	AF15	ECC1
AB15	V_{DD}	AC24	BA1	AE7	IICSDA	AF16	GND
AB16	V_{DD}	AC25	ClkEn1	AE8	GPIO6[TS4]	AF17	$\overline{\text{BankSel1}}$
AB17	V_{DD}	AC26	MemClkOut0	AE9	MemData9	AF18	GPIO4[TS2O]
AB18	GND	AD1	MemData20	AE10	Res – 27/OV_{DD} – 35	AF19	MemAddr10
AB19	OV_{DD}	AD2	$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]	AE11	MemData5	AF20	PHYRxClk
AB20	OV_{DD}	AD3	GND	AE12	MemData1	AF21	GND
AB21	OV_{DD}	AD4	MemData18	AE13	ECC6	AF22	MemAddr4
AB22	GND	AD5	MemData17	AE14	ECC0	AF23	PHYRxD1
AB23	$\overline{\text{CAS}}$	AD6	IICSCL	AE15	$\overline{\text{BankSel2}}$	AF24	$\overline{\text{RAS}}$
AB24	BA0	AD7	MemData13	AE16	UART0_Rx	AF25	GND
AB25	ClkEn0	AD8	MemData10	AE17	UARTSerClk	AF26	GND

Signal List

The table following table provides a summary of the number of package pins associated with each functional interface group.

Pin Summary

Group	No. of Pins		
	413-Ball package	456-Ball Package	
		35 mm	27 mm
PCI	60	60	60
Ethernet	18	18	18
SDRAM	71	71	71
External peripheral	96	96	96
External master	9	9	9
Internal peripheral	15	15	15
Interrupts	7	7	7
JTAG	5	5	5
System	19	19	19
Total Signal Pins	**300**	**300**	**300**
OV_{DD}	38	32	24
V_{DD}	22	24	24
Gnd	26	60	56
Thermal (and Gnd)	15	36	36
Reserved	12	4	16
Total Pins	**413**	**456**	**456**

In the table “Signal Functional Description” on page 33, each external signal is listed along with a short description of the signal function. Some signals are multiplexed on the same package pin (ball) so that the pin can be used for different functions. Multiplexed signals are shown as a default signal followed by a secondary signal in square brackets (for example, C0:3[$\overline{BE0:3}$]) The two signals are described consecutively within each functional description. Active-low signals such as $\overline{BE0:3}$ are marked with an overline.

It is expected that in any single application a particular pin will always be programmed to serve the same function. The flexibility of multiplexing allows a single chip to offer a richer pin selection than would otherwise be possible.

In addition to multiplexing, many pins are also multi-purpose. For example, the EBC peripheral controller address pins are used as outputs by the PPC405GP to broadcast an address to external slave devices when the PPC405GP has control of the external bus. When, during the course of normal chip operation, an external master gains ownership of the external bus, these same pins are used as inputs which are driven by the external master and received by the EBC in the PPC405GP. In this example, the pins are also bidirectional, serving as both inputs and outputs.

One group of pins is used as strapped inputs during system reset. These pins function as strapped inputs only during reset and are used for other functions during normal operation (see “Strapping” on page 56). Note that these are *not multiplexed* pins since the function of the pins is not programmable.

The following table lists all of the I/O signals provided by the PPC405GP. Please refer to “Signals Listed Alphabetically” on page 16 for the pin number to which each signal is assigned.

Signal Functional Description (Part 1 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCI Interface				
PCIAD31 PCIAD30 PCIAD29 PCIAD28 PCIAD27 PCIAD26 PCIAD25 PCIAD24 PCIAD23 PCIAD22 PCIAD21 PCIAD20 PCIAD19 PCIAD18 PCIAD17 PCIAD16 PCIAD15 PCIAD14 PCIAD13 PCIAD12 PCIAD11 PCIAD10 PCIAD9 PCIAD8 PCIAD7 PCIAD6 PCIAD5 PCIAD4 PCIAD3 PCIAD2 PCIAD1 PCIAD0	PCI Address/Data Bus. Multiplexed address and data bus	I/O	5V tolerant 3.3V PCI	4
PCIC0[$\overline{\text{BE3}}$] PCIC1[$\overline{\text{BE2}}$] PCIC2[$\overline{\text{BE1}}$] PCIC3[$\overline{\text{BE0}}$]	PCI C (bus command) or $\overline{\text{B}}$yte enable	I/O	5V tolerant 3.3V PCI	4
PCIParity	PCI parity. Parity is even across PCIAD0:31 and PCIC0:3[$\overline{\text{BE0:3}}$]. PCIParity is valid one cycle after either an address or data phase. The PCI device that drove PCIAD0:31 is responsible for driving PCIParity on the next PCI bus clock.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIFrame}}$	$\overline{\text{PCIFrame}}$ is driven by the current PCI bus master to indicate beginning and duration of a PCI access.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCIIRDY}}$	$\overline{\text{PCIIRDY}}$ is driven by the current PCI bus master. Assertion of $\overline{\text{PCIIRDY}}$ indicates that the PCI initiator is ready to transfer data.	I/O	5V tolerant 3.3V PCI	4
$\overline{\text{PCITRDY}}$	The target of the current PCI transaction drives $\overline{\text{PCITRDY}}$. Assertion of $\overline{\text{PCITRDY}}$ indicates that the PCI target is ready to transfer data.	I/O	5V tolerant 3.3V PCI	4

Signal Functional Description (Part 2 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PCIStop	The target of the current PCI transaction can assert PCIStop to indicate to the requesting PCI master that it wants to end the current transaction.	I/O	5V tolerant 3.3V PCI	4
PCIDevSel	PCIDevSel is driven by the target of the current PCI transaction. A PCI target asserts PCIDevSel when it has decoded an address and command encoding and claims the transaction.	I/O	5V tolerant 3.3V PCI	4
PCIIDSel	PCIIDSel is used during configuration cycles to select the PCI slave interface for configuration	I	5V tolerant 3.3V PCI Rcvr	5
PCISErr	PCISErr is used for reporting address parity errors or catastrophic failures detected by a PCI target.	I/O	5V tolerant 3.3V PCI	4
PCIPErr	PCIPErr is used for reporting data parity errors on PCI transactions. PCIPErr is driven active by the device receiving PCIAD0:31, PCIC0:3[BE0:3], and PCIParity, two PCI clocks following the data in which bad parity is detected.	I/O	5V tolerant 3.3V PCI	4
PCIClk	PCIClk is used as the asynchronous PCI clock when in asynch mode. It is unused when the PCI interface is operated synchronously with the PLB bus.	I	5V tolerant 3.3V PCI Rcvr	5
PCIReset	PCI specific reset	O	5V tolerant 3.3V PCI	
PCIINT[PerWE]	PCI interrupt. Open-drain output (two states; 0 or open circuit) or Peripheral write enable. Logical AND of the four PerWBE0:3 write byte enables	O	5V tolerant 3.3V PCI	
PCIReq0[Gnt]	Multipurpose signal, used as PCIReq0 when internal arbiter is used, and as Gnt when external arbiter is used.	I	5V tolerant 3.3V PCI Rcvr	4
PCIReq1 PCIReq2 PCIReq3 PCIReq4 PCIReq5	Used as PCIReq1:5 input when internal arbiter is used	I	5V tolerant 3.3V PCI Rcvr	4
PCIGnt0[Req]	Gnt0 when internal arbiter is used or Req when external arbiter is used	O	5V tolerant 3.3V PCI	
PCIGnt1 PCIGnt2 PCIGnt3 PCIGnt4 PCIGnt5	Used as PCIGnt1:5 output when internal arbiter is used.	O	5V tolerant 3.3V PCI	

Signal Functional Description (Part 3 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Ethernet Interface				
PHYRxD3 PHYRxD2 PHYRxD1 PHYRxD0	Received data. This is a nibble wide bus from the PHY. The data is synchronous with the PHYRxClk.	I	5V tolerant 3.3V Rcvr	1, 4
EMCTxD3 EMCTxD2 EMCTxD1 EMCTxD0	Transmit data. A nibble wide data bus towards the net. The data is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
PHYRxErr	Receive Error. This signal comes from the PHY and is synchronous to the PHYRxClk.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
PHYRxClk	Receiver Medium clock. This signal is generated by the PHY.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
PHYRxDV	Receive Data Valid. Data on the Data Bus is valid when this signal is activated. Deassertion of this signal indicates end of the frame reception.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
PHYCrS	Carrier Sense signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
EMCTxErr	Transmit Error. This signal is generated by the Ethernet controller, is connected to the PHY and is synchronous with the PHYTxClk. It informs the PHY that an error was detected.	O	5V tolerant 3.3V LVTTL	6
EMCTxEn	Transmit data Enabled. This signal is driven by EMAC2 to the PHY. Data is valid during the active state of this signal. Deassertion of this signal indicates end of frame transmission. This signal is synchronous to the PHYTxClk.	O	5V tolerant 3.3V LVTTL	6
PHYTxClk	This clock comes from the PHY and is the Medium Transmit clock.	I	5V tolerant 3V LVTTL Rcvr	1, 4
PHYCol	Collision signal from the PHY. This is an asynchronous signal.	I	5V tolerant 3.3V LVTTL Rcvr	1, 5
EMCMDClk	Management Data Clock. The MDClk is sourced to the PHY. This clock has a period of 400ns, adjustable via EMAC0_STACR[OPBC]. Management information is transferred synchronously with respect to this clock.	O	5V tolerant 3.3V LVTTL	
EMCMDIO[PHYMDIO]	Management Data Input/Output is a bidirectional signal between the Ethernet controller and the PHY. It is used to transfer control and status information.	I/O	5V tolerant 3.3V LVTTL	1, 4

Signal Functional Description (Part 4 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
SDRAM Interface				
MemData0 MemData1 MemData2 MemData3 MemData4 MemData5 MemData6 MemData7 MemData8 MemData9 MemData10 MemData11 MemData12 MemData13 MemData14 MemData15 MemData16 MemData17 MemData18 MemData19 MemData20 MemData21 MemData22 MemData23 MemData24 MemData25 MemData26 MemData27 MemData28 MemData29 MemData30 MemData31	Memory data bus **Notes:** 1. MemData0 is the most significant bit (msb). 2. MemData31 is the least significant bit (lsb).	I/O	3.3V LVTTL	4
MemAddr12 MemAddr11 MemAddr10 MemAddr9 MemAddr8 MemAddr7 MemAddr6 MemAddr5 MemAddr4 MemAddr3 MemAddr2 MemAddr1 MemAddr0	Memory address bus **Notes:** 1. MemAddr12 is the most significant bit (msb). 2. MemAddr0 is the least significant bit (lsb).	O	3.3V LVTTL	

Signal Functional Description (Part 5 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
BA1 BA0	Bank Address supporting up to 4 internal banks	O	3.3V LVTTL	
$\overline{\text{RAS}}$	Row Address Strobe	O	3.3V LVTTL	
$\overline{\text{CAS}}$	Column Address Strobe	O	3.3V LVTTL	
DQM0 DQM1 DQM2 DQM3	DQM for byte lanes 0 (MemData0:7), 1 (MemData8:15), 2 (MemData16:23), and 3 (MemData24:31)	O	3.3V LVTTL	
DQMCB	DQM for ECC check bits	O	3.3V LVTTL	
ECC0 ECC1 ECC2 ECC3 ECC4 ECC5 ECC6 ECC7	ECC check bits 0:7	I/O	3.3V LVTTL	4
$\overline{\text{BankSel0}}$ $\overline{\text{BankSel1}}$ $\overline{\text{BankSel2}}$ $\overline{\text{BankSel3}}$	Select up to four external SDRAM banks	O	3.3V LVTTL	
$\overline{\text{WE}}$	Write Enable	O	3.3V LVTTL	
ClkEn0 ClkEn1	SDRAM Clock Enable	O	3.3V LVTTL	
MemClkOut0 MemClkOut1	Two copies of an SDRAM clock allows, in some cases, glueless SDRAM attach without requiring this signal to be repowered by a PLL or zero-delay buffer.	O	3.3V LVTTL	

Signal Functional Description (Part 6 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External SLAVE Peripheral Interface				
PerData0 PerData1 PerData2 PerData3 PerData4 PerData5 PerData6 PerData7 PerData8 PerData9 PerData10 PerData11 PerData12 PerData13 PerData14 PerData15 PerData16 PerData17 PerData18 PerData19 PerData20 PerData21 PerData22 PerData23 PerData24 PerData25 PerData26 PerData27 PerData28 PerData29 PerData30 PerData31	Peripheral data bus used by PPC405GP when not in external master mode, otherwise used by external master **Note:** PerData0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1

Signal Functional Description (Part 7 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
PerAddr0 PerAddr1 PerAddr2 PerAddr3 PerAddr4 PerAddr5 PerAddr6 PerAddr7 PerAddr8 PerAddr9 PerAddr10 PerAddr11 PerAddr12 PerAddr13 PerAddr14 PerAddr15 PerAddr16 PerAddr17 PerAddr18 PerAddr19 PerAddr20 PerAddr21 PerAddr22 PerAddr23 PerAddr24 PerAddr25 PerAddr26 PerAddr27 PerAddr28 PerAddr29 PerAddr30 PerAddr31	Peripheral address bus used by PPC405GP when not in external master mode, otherwise used by external master. **Note:** PerAddr0 is the most significant bit (msb) on this bus.	I/O	5V tolerant 3.3V LVTTL	1
PerPar0 PerPar1 PerPar2 PerPar3	Peripheral byte parity signals	I/O	5V tolerant 3.3V LVTTL	1
$\overline{\text{PerWBE0}}$ $\overline{\text{PerWBE1}}$ $\overline{\text{PerWBE2}}$ $\overline{\text{PerWBE3}}$	As outputs, these pins can act as byte-enables which are valid for an entire cycle or as write-byte-enables which are valid for each byte on each data transfer, allowing partial word transactions. As outputs, pins are used by either peripheral controller or DMA controller depending upon the type of transfer involved. Used as inputs when external bus master owns the external interface	I/O	5V tolerant 3.3V LVTTL	1, 2
$\overline{\text{PerCS0}}$	Peripheral chip select bank 0	O	5V tolerant 3.3V LVTTL	2
$\overline{\text{PerCS1}}$[GPIO10] $\overline{\text{PerCS2}}$[GPIO11] $\overline{\text{PerCS3}}$[GPIO12] $\overline{\text{PerCS4}}$[GPIO13] $\overline{\text{PerCS5}}$[GPIO14] $\overline{\text{PerCS6}}$[GPIO15] $\overline{\text{PerCS7}}$[GPIO16]	Seven additional peripheral chip selects or General Purpose I/O - To access this function, software must toggle a DCR register bit.	O[I/O]	5V tolerant 3.3V LVTTL [mux'd]	1,2

Signal Functional Description (Part 8 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
$\overline{\text{PerOE}}$	Used by either peripheral controller or DMA controller depending upon the type of transfer involved. When the PPC405GP is the bus master, it enables the selected SDRAMs to drive the bus.	O	5V tolerant 3.3V LVTTL	2
PerR/$\overline{\text{W}}$	Used by the PPC405GP when not in external master mode, as output by either the peripheral controller or DMA controller depending upon the type of transfer involved. High indicates a read from memory, low indicates a write to memory. Otherwise it used by the external master as an input to indicate the direction of transfer.	I/O	5V tolerant	1, 2
PerReady	Used by a peripheral slave to indicate it is ready to transfer data.	I	5V tolerant Rcvr	1, 2
$\overline{\text{PerBLast}}$	Used by the PPC405GP when not in external master mode, otherwise used by external master. Indicates the last transfer of a memory access.	I/O	5V tolerant 3.3V LVTTL	1, 4
DMAReq0 DMAReq1 DMAReq2 DMAReq3	DMAReq0:3 are used by slave peripherals to indicate they are prepared to transfer data.	I	5V tolerant Rcvr	1, 5
DMAAck0 DMAAck1 DMAAck2 DMAAck3	DMAAck0:3 are used by the PPC405GP to indicate that data transfers have occurred.	O	5V tolerant 3.3V LVTTL	6
EOT0[TC0] EOT1[TC1] EOT2[TC2] EOT3[TC3]	End Of Transfer/Terminal Count	I/O	5V tolerant 3.3V LVTTL	1, 5

Signal Functional Description (Part 9 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
External MASTER Peripheral Interface				
PerClk	Peripheral clock to be used by an external master and by synchronous peripheral slaves	O	5V tolerant 3.3V LVTTL	
$\overline{\text{ExtReset}}$	Peripheral reset to be used by an external master and by synchronous peripheral slaves	O	5V tolerant 3.3V LVTTL	
HoldReq	Hold Request, used by an external master to request ownership of the peripheral bus	I	5V tolerant Rcvr	1, 5
HoldAck	Hold Acknowledge, used by the PPC405GP to transfer ownership of peripheral bus to an external master	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{ExtReq}}$	ExtReq is used by an external master to indicate it is prepared to transfer data	I	5V tolerant Rcvr	1, 4
$\overline{\text{ExtAck}}$	ExtAck is used by the PPC405GP to indicate that a data transfer occurred.	O	5V tolerant 3.3V LVTTL	6
HoldPri	Used by an external master to indicate the priority of a given transfer (0 = high, 1 = low)	I	5V tolerant Rcvr	1, 4
BusReq	Used when the PPC405GP needs to regain control of peripheral interface from an external Master	O	5V tolerant 3.3V LVTTL	
PerErr	Used as an input. Used to record external Master errors and external slave peripheral errors	I	5V tolerant Rcvr	1, 5
Internal Peripheral Interface				
UARTSerClk	Serial Clock used to provide an alternative clock to the internally generated serial clock. Used in cases where the allowable internally generated baud rates are not satisfactory. This input can be individually connected to either UART.	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Rx	UART0 Serial Data In	I	5V tolerant 3.3V LVTTL	1, 4
UART0_Tx	UART0 Serial Data Out	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_DCD}}$	UART0 Data Carrier Detect	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_DSR}}$	UART0 Data Set Ready	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_CTS}}$	UART0 Clear To Send	I	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{UART0\_DTR}}$	UART0 Data Terminal Ready	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_RTS}}$	UART0 Request To Send	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART0\_RI}}$	UART0 Ring Indicator	I	5V tolerant 3.3V LVTTL Rcvr	1, 4

Signal Functional Description (Part 10 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
UART1_Rx	UART1 Serial Data In	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
UART1_Tx	UART1 Serial Data Out	O	5V tolerant 3.3V LVTTL	6
$\overline{\text{UART1\_DSR}}$ [$\overline{\text{UART1\_CTS}}$]	UART1 Data Set Ready or UART1 Clear To Send. To access this function, software must toggle a DCR register bit.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
$\overline{\text{UART1\_RTS}}$ [$\overline{\text{UART1\_DTR}}$]	UART1 Request To Send or UART1 Data Terminal Ready. To access this function, software must toggle a DCR register bit.	O	5V tolerant 3.3V LVTTL	6
IICSCL	IIC Serial Clock	I/O	5V tolerant 3.3V LVTTL	1, 2
IICSDA	IIC Serial Data	I/O	5V tolerant 3.3V LVTTL	1, 2
Interrupts Interface				
IRQ0[GPIO17] IRQ1[GPIO18] IRQ2[GPIO19] IRQ3[GPIO20] IRQ4[GPIO21] IRQ5[GPIO22] IRQ6[GPIO23]	Interrupt requests or General Purpose I/O. To access this function, software must toggle a DCR register bit.]	I[I/O]	5V tolerant 3.3V LVTTL	1, 5
JTAG Interface				
TDI	Test data in	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
TMS	JTAG test mode select	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
TDO	Test data out	O	5V tolerant 3.3V LVTTL	
TCK	JTAG test clock	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
$\overline{\text{TRST}}$	JTAG reset	I	5V tolerant Rcvr	5

Signal Functional Description (Part 11 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
System Interface				
SysClk	Main system clock input	I	5V tolerant 3.3V LVTTL Rcvr	
$\overline{\text{SysReset}}$	Main system reset. External logic can drive this bidirectional pin low (minimum of 16 cycles) to initiate a system reset. The PPC405GP then holds the output low for 8192 cycles to reset all internal and external logic connected to $\overline{\text{SysReset}}$. A system reset can also be initiated by software. Implemented as open-drain I (two output states; 0 or open circuit).	I/O	5V tolerant 3.3V LVTTL Rcvr	1, 2
AV_{DD}	Clean voltage input for the PLL	I		
SysErr	Set to 1 when a Machine Check is generated.	O	5V tolerant 3.3V LVTTL	
$\overline{\text{Halt}}$	Halt from external debugger.	I	5V tolerant 3.3V LVTTL Rcvr	1, 4
GPIO1[TS1E] GPIO2[TS2E]	General Purpose I/O or Even Trace execution status.To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 6
GPIO3[TS1O] GPIO4[TS2O]	General Purpose I/O or Odd Trace execution status. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1 (A22, AF18), 6 (AF18 only)
GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6]	General Purpose I/O Trace status. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 4
GPIO9[TrcClk]	General Purpose I/O or Trace interface clock. A toggling signal that is always half of the CPU core frequency. To access this function, software must toggle a DCR register bit.	I/O[O]	5V tolerant 3.3V LVTTL	1, 4
$\overline{\text{TestEn}}$	Test Enable. Used only for manufacturing tests. Pull down for normal operation.	I	5V tolerant Rcvr w/ PD	3
RcvrInh	Receiver Inhibit. Used only for manufacturing tests. Pull up for normal operation.	I	5V tolerant Rcvr	2
DrvrInh1 DrvrInh2	Driver Inhibit 1 and 2. Used only for manufacturing tests. Pull up for normal operation.	I	5V tolerant Rcvr	2
TmrClk	This input must toggle at a rate of less than one half the CPU core frequency (less than 100MHz in most cases). In most cases this input toggles much slower (in the 1MHz to 10MHz range).	I	5V tolerant 3.3V LVTTL Rcvr	1, 4

Signal Functional Description (Part 12 of 12)

Multiplexed signals are shown in brackets following the first signal name assigned to each multiplexed ball.

Notes:

1. Receiver input has hysteresis
2. Must pull up (recommended value is 3kΩ to 3.3V, 10kΩ to 5V)
3. Must pull down (recommended value is 1kΩ)
4. If not used, must pull up (recommended value is 3kΩ to 3.3V)
5. If not used, must pull down (recommended value is 1kΩ)
6. Strapping input during reset; pull-up or pull-down required

Signal Name	Description	I/O	Type	Notes
Ground pins				
GND	Ground **Note:** On the 456-ball packages, L11-L16, M11-M16, N11-N16, P11-P16, R11-R16, and T11-T16 are also thermal balls. On the 413-ball package, J11, J13, K11-K13, L11-L13, M11-N13 , N11-N13, P11-P13, R11, and R13 are also thermal balls.			
OV_{DD} pins				
OV_{DD}	Output driver voltage—3.3V			
V_{DD} pins				
V_{DD}	Logic voltage—2.5V			
Other pins				
Reserved	Reserved—Ex cept for Y5 (on the 413-ball package) or AF4, do not connect signals, voltage, or ground to these pins. Y5 (on the 413-ball package) and AF4 must be tied to OV_{DD} or GND.			

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device

Characteristic	Symbol	Value	Unit
Supply Voltage (Internal Logic)	V_{DD}	0 to 2.7[1]	V
Supply Voltage (I/O Interface)	OV_{DD}	0 to 3.6[1]	V
PLL Supply Voltage	AV_{DD}	0 to 2.7	V
Input Voltage (3.3V LVTTL receivers)	V_{IN}	0 to 3.6	V
Input Voltage (5.0V LVTTL receivers)	V_{IN}	0 to 5.5	V
Storage Temperature Range	T_{STG}	-55 to 150	°C
Case temperature under bias	T_C	-40 to +120	°C

Notes:

1. If $OV_{DD} \geq 0.4$V it is required that $V_{DD} \geq 0.4$V. Supply excursions not meeting this criteria must be limited to less than 25ms duration during each power up or power down event.

Package Thermal Specifications

The PPC405GP is designed to operate within a case temperature range of -40˚C to 120˚C. Thermal resistance values for the E-PBGA packages in a convection environment are as follows:

Package—Thermal Resistance	Symbol	Airflow ft/min (m/sec)			Unit
		0 (0)	100 (0.51)	200 (1.02)	
35mm, 456-balls—Junction-to-Case	θ_{JC}	2	2	2	°C/W
35mm, 456-balls—Case-to-Ambient[1]	θ_{CA}	14	13	12	°C/W
27mm, 456-balls—Junction-to-Case	θ_{JC}	2	2	2	°C/W
27mm, 456-balls—Case-to-Ambient[1]	θ_{CA}	18	16	15	°C/W
25mm, 413-balls—Junction-to-Case	θ_{JC}	1.5	1.5	1.5	°C/W
25mm, 413-balls—Case-to-Ambient[1]	θ_{CA}	17	15	13	°C/W

Notes:

1. For a chip mounted on a JEDEC 2S2P card without a heat sink.
2. For a chip mounted on a card with at least one signal and two power planes, the following relationships exist:
   a. Case temperature, T_C, is measured at top center of case surface with device soldered to circuit board.
   b. $T_A = T_C - P \times \theta_{CA}$, where T_A is ambient temperature and P is power consumption.
   c. $T_{CMax} = T_{JMax} - P \times \theta_{JC}$, where T_{JMax} is maximum junction temperature and P is power consumption.

Recommended DC Operating Conditions

Device operation beyond the conditions specified is not recommended. Extended operation beyond the recommended conditions can affect device reliability.

Notes:

1. PCI drivers meet PCI specifications.
2. It is recommended that your system design derive the V_{DD} supply from the OV_{DD} supply so as to minimize the possibility of V_{DD} being present in the absence of OV_{DD}.

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Logic Supply Voltage	V_{DD}	2.3	2.5	2.7	V	2
I/O Supply Voltage	OV_{DD}	3.0	3.3	3.6	V	2
PLL Supply Voltage	AV_{DD}	2.3	2.5	2.7	V	
Input Logic High (3.3V LVTTL receivers)	V_{IH}	2.0		OV_{DD}	V	
Input Logic High (5.0V LVTTL receivers)	V_{IH}	2.0		5.5	V	
Input Logic Low	V_{IL}	0		0.8	V	
Output Logic High	V_{OH}	2.4		OV_{DD}	V	
Output Logic Low	V_{OL}	0		0.4	V	
Input Leakage Current (No pull-up or pull-down)	I_{IL1}	0		0	µA	
Input Leakage Current for Pull-Down	I_{IL2}	0 (LPDL)		400 (MPUL)	µA	
Input Leakage Current for Pull-Up	I_{IL3}	–250 (LPDL)		0 (MPUL)	µA	
Input Max Allowable Overshoot (3.3V LVTTL receivers)	V_{IMAO3}			OV_{DD} + 0.6	V	
Input Max Allowable Overshoot (5.0V LVTTL receivers)	V_{IMAO5}			5.5	V	
Input Max Allowable Undershoot (3.3V or 5.0V receivers)	V_{IMAU}	– 0.6			V	
Output Max Allowable Overshoot (3.3V or 5.0V receivers)	V_{OMAO}			OV_{DD} + 0.3	V	
Output Max Allowable Undershoot (3.3V and 5.0V receivers)	V_{OMAU3}	– 0.6			V	
Case Temperature	T_C	– 40		85	°C	

Capacitance

Parameter	Symbol	Maximum	Unit	Notes
Input Capacitance Group 1 (3.3V LVTTL //O)	C_{IN1}	2.5	pF	
Input Capacitance Group 2 (5V tolerant LVTTL I/O)	C_{IN2}	3.5	pF	
Input Capacitance Group 3 (PCI I/O)	C_{IN3}	5.0	pF	
Input Capacitance Group 1 (RX only pins)	C_{IN4}	0.75	pF	

DC Electrical Characteristics

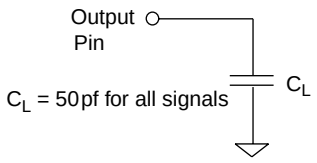
Parameter	Symbol	Minimum	Typical	Maximum	Unit
Active Operating Current (V_{DD})–200MHz	I_{DD}		550	670	mA
Active Operating Current (V_{DD})–266MHz	I_{DD}		730	880	mA
Active Operating Current (OV_{DD})–200MHz	I_{ODD}		35	37	mA
Active Operating Current (OV_{DD})–266MHz	I_{ODD}		37	40	mA
PLL Voltage (AV_{DD})	V_{PLL}	2.3	2.5	2.7	V
PLL V_{DD} Input current	I_{PLL}		16	23	mA
Active Operating Power–200MHz	P_{DD}		1.5	2.0[1]	W
Active Operating Power–266MHz	P_{DD}		2.0	2.6[1]	W

Notes:

1. V_{DD} = 2.7V, OV_{DD} = 3.6 V, T_C = 85°C, PCI Clk = ???MHz, CPU/PLB/OPB/PCI = 266/133/66/33MHz. Measurements taken across process (w/c silicon to b/c silicon), while running an instruction set designed to simulate a maximum environment.

Test Conditions

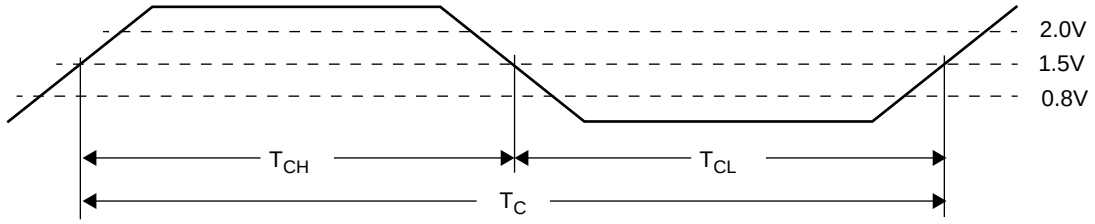
Clock timing and switching characteristics are specified in accordance with operating conditions shown in the table “Recommended DC Operating Conditions.” AC specifications are characterized at V_{DD} = 3.14V and T_J = 100˚C with the 50pF test load (C_L) shown in the figure at right.



SysClk and MemClk Timing

Symbol	Parameter	Min	Max	Units
SysClk Input				
F_C	SysClk clock input frequency	25	66.6	MHz
T_C	SysClk clock period	15	40	ns
T_{CS}	Clock edge stability		0.15	ns
T_{CH}	Clock input high time	40% of nominal period	60% of nominal period	ns
T_{CL}	Clock input low time	40% of nominal period	60% of nominal period	ns
Note: Input slew rate > 2V/ns				
MemClk Output				
F_C	MemClk clock output frequency–200MHz		100	MHz
T_C	MemClk clock period–200MHz	10		ns
F_C	MemClk clock output frequency–266MHz		133	MHz
T_C	MemClk clock period–266MHz	7.5		ns
T_{CH}	Clock output high time	35% of nominal period	65% of nominal period	ns
T_{CL}	Clock output low time	35% of nominal period	65% of nominal period	ns

Timing Waveform



Spread Spectrum Clocking

Care must be taken when using a spread spectrum clock generator (SSCG) with the PPC405GP. This controller uses a PLL for clock generation inside the chip. The accuracy with which the PLL follows the SSCG is referred to as tracking skew. The PLL bandwidth and phase angle determine how much tracking skew there is between the SSCG and the PLL for a given frequency deviation and modulation frequency. When using an SSCG with the PPC405GP the following conditions must be met:

- The frequency deviation must not violate the minimum clock cycle time. Therefore, when operating the PPC405GP with one or more internal clocks at their maximum supported frequency, the SSCG can only lower the frequency.
- The maximum frequency deviation cannot exceed –3%, and the modulation frequency cannot exceed 40kHz. In some cases, on-board PPC405GP peripherals impose more stringent requirements (see Note 1).
- Use the Peripheral Bus Clock for logic that is synchronous to the peripheral bus since this clock tracks the modulation.
- Use the SDRAM MemClk since it also tracks the modulation.

Notes:

1. The PCI clock specification for 66MHz allows a maximum frequency deviation of –1% at a modulation between 30kHz and 33kHz. PCI asynchronous mode is unaffected.
2. The serial port baud rates are synchronous to the modulated clock. The serial port has a tolerance of approximately 1.5% on baud rate before framing errors begin to occur. The 1.5% tolerance assumes that the connected device is running at precise baud rates. If an external serial clock is used the baud rate is unaffected by the modulation
3. Ethernet operation is unaffected.
4. IIC operation is unaffected.

Caution: It is up to the system designer to ensure that any SSCG used with the PPC405GP meets the above requirements and does not adversely affect other aspects of the system.

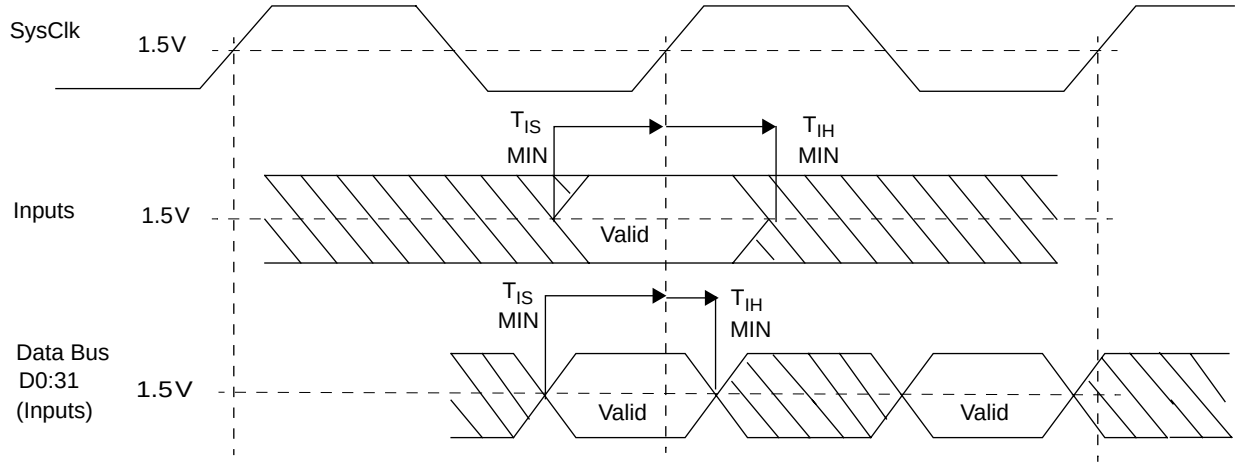
Peripheral Interface Clock Timings

Parameter	Min	Max	Units
PCIClk input frequency (asynchronous mode)	Note 1	66	MHz
PCIClk period (asynchronous mode)	15	Note 1	ns
PCI Clock frequency (synchronous mode)	25	33	MHz
PCI Clock period (synchronous mode - Note 2)	30	40	ns
PCIClk input high time	40% of nominal period	60% of nominal period	ns
PCIClk input low time	40% of nominal period	60% of nominal period	ns
EMCMDClk output frequency	–	2.5	MHz
EMCMDClk period	400	–	ns
EMCMDClk output high time	160	–	ns
EMCMDClk output low time	160	–	ns
PHYTxClk input frequency	2.5	25	MHz
PHYTxClk period	40	400	ns
PHYTxClk input high time	35% of nominal period	–	ns
PHYTxClk input low time	35% of nominal period	–	ns
PHYRxClk input frequency	2.5	25	MHz
PHYRxClk period	40	400	ns
PHYRxClk input high time	35% of nominal period	–	ns
PHYRxClk input low time	35% of nominal period	–	ns
PerClk output frequency–200 MHz (for external master or synchronous slaves)	–	50	MHz
PerClk period–200 MHz	20	–	ns
PerClk output frequency–266 MHz (for external master or synchronous slaves)	–	66	
PerClk period–266 MHz	15	–	
PerClk output high time	50% of nominal period	66% of nominal period	ns
PerClk output low time	33% of nominal period	50% of nominal period	ns
UARTSerClk input frequency (Note 3)	–	$1000/(2T_{OPB}+2ns)$	MHz
UARTSerClk period	$2T_{OPB}+2$	–	ns
UARTSerClk input high time	$T_{OPB}+1$	–	ns
UARTSerClk input low time	$T_{OPB}+1$	–	ns
TmrClk input frequency–200 MHz	–	50	MHz
TmrClk period–200 MHz	20	–	ns
TmrClk input frequency–266 MHz	–	66	
TmrClk period–266 MHz	15	–	
TmrClk input high time	40% of nominal period	60% of nominal period	ns
TmrClk input low time	40% of nominal period	60% of nominal period	ns

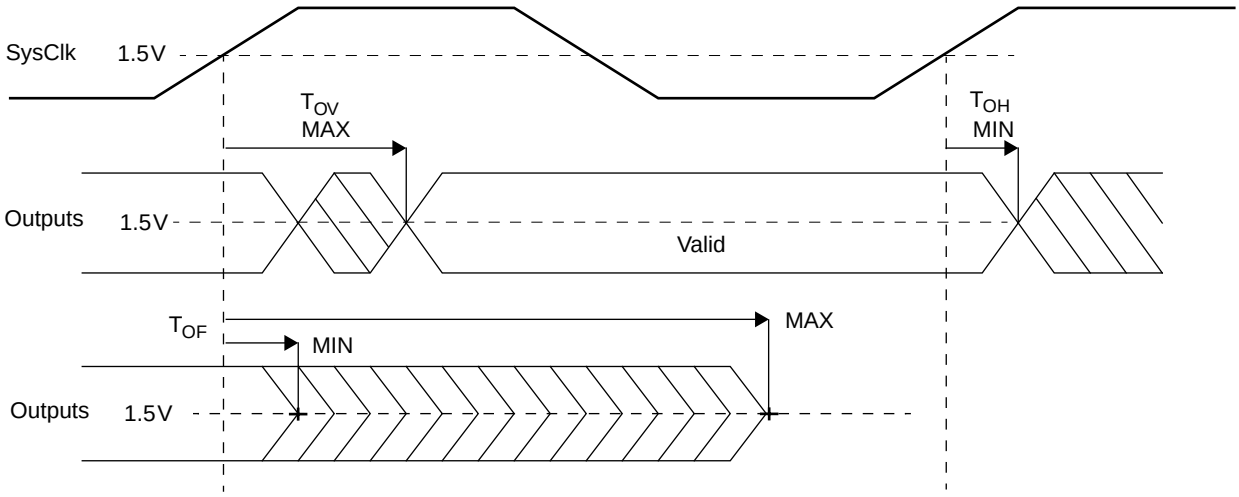
Notes:

1. In asynchronous PCI mode the minimum PCIClk frequency is 1/8 the PLB Clock. Refer to the PPC405GP User's Manual for more information.
2. In synchronous PCI mode the PCI clock is derived from SysClk and the PCIClk input pin is unused.
3. T_{OPB} is the period in ns of the OPB clock. The internal OPB clock runs at 1/2 the frequency of the PLB clock. The maximum OPB clock frequency is 50 MHz for 200 MHz parts and 66 MHz.for 266 MHz parts.

Input Setup and Hold Waveform



Output Delay and Float Timing Waveform



I/O Specifications—All (Part 1 of 2)

Notes:

1. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
PCI Interface								
PCIAD31:0	3	0	6	1.8	12.3	15.5	PCIClk	1
PCIC3:0[$\overline{\text{BE3:0}}$]	3	0	6	1.8	12.3	15.5	PCIClk	1
PCIClk	dc	dc		n/a	n/a	n/a		async
$\overline{\text{PCIDevSel}}$	3	0	6	1.8	12.3	15.5	PCIClk	1
$\overline{\text{PCIFrame}}$	3	0	6	1.8	12.3	15.5	PCIClk	1
$\overline{\text{PCIGnt0}}$[$\overline{\text{Req}}$] PCIGnt1:5	n/a	n/a	6	1.8	12.3	15.5	PCIClk	1
PCIIDSel	3	0	6	1.8	n/a	n/a	PCIClk	1
$\overline{\text{PCIINT}}$[PerWE]	n/a	n/a	dc	dc	12.3	15.5	PCIClk	async
$\overline{\text{PCIIRDY}}$	3	0	6	1.8	12.3	15.5	PCIClk	1
PCIParity	3	0	6	1.8	12.3	15.5	PCIClk	1
$\overline{\text{PCIPErr}}$	3	0	6	1.8	12.3	15.5	PCIClk	1
$\overline{\text{PCIReq0}}$[$\overline{\text{Gnt}}$] PCIReq1:5	5	0	n/a	n/a	n/a	n/a	PCIClk	1
$\overline{\text{PCIReset}}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{\text{PCISErr}}$	n/a	n/a	n/a	n/a	12.3	15.5	PCIClk	
$\overline{\text{PCIStop}}$	3	0	6	1.8	12.3	15.5	PCIClk	1
$\overline{\text{PCITRDY}}$	3	0	6	1.8	12.3	15.5	PCIClk	1
Ethernet Interface								
EMCMDClk	n/a	n/a	settable	2	9	6		2, async
EMCMDIO[PHYMDIO]	100	0	1 OPB clock period + 10ns	1 OPB clock period	9	6	EMCMDClk	2
EMCTxD3:0	n/a	n/a	20	2	9	6	PHYTX	2
EMCTxEn	n/a	n/a	20	2	9	6	PHYTX	2
EMCTxErr	n/a	n/a	20	2	9	6	PHYTX	2
PHYCol					9	6		2, async
PHYCrS					9	6		2, async
PHYRxClk					n/a	n/a		2, async
PHYRxD3:0	4	1	n/a	n/a	9	6	PHYRX	2
PHYRxDV	4	1	n/a	n/a	9	6	PHYRX	2
PHYRxErr	4	1	n/a	n/a	9	6	PHYRX	2
PHYTxClk					n/a	n/a		2, async

I/O Specifications—All (Part 2 of 2)

Notes:

1. PCI timings are for asynchronous operation up to 66MHz. PCI output hold time requirement is 1ns for 66MHz and 2ns for 33MHz.
2. Ethernet interface meets timing requirements as defined by IEEE 802.3 standard.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
Internal Peripheral Interface								
IICSCL	n/a	n/a	n/a	n/a	19	12		
IICSDA	n/a	n/a	n/a	n/a	19	12		
UART0_CTS	n/a	n/a			12	8		
UART0_DCD	n/a	n/a			12	8		
UART0_DSR	n/a	n/a			12	8		
UART0_DTR					12	8		
UART0_RI	n/a	n/a			12	8		
UART0_RTS			n/a	n/a	12	8		
UART0_Rx	n/a	n/a			12	8		
UART0_Tx			n/a	n/a	12	8		
UART1_RTS [UART1_DTR]			n/a	n/a	12	8		
UART1_DSR [UART1_CTS]	n/a	n/a			n/a	n/a		
UART1_Rx	n/a	n/a			n/a	n/a		
UART1_Tx			n/a	n/a	12	8		
UARTSerClk	n/a	n/a			n/a	n/a		
Interrupts Interface								
IRQ0:6[GPIO17:23]					12	8		
JTAG Interface								
TCK					n/a	n/a		async
TDI					n/a	n/a		async
TDO					12	8		async
TMS					n/a	n/a		async
TRST					n/a	n/a		async
System Interface								
DrvrInh1:2	dc	dc	n/a	n/a	n/a	n/a		
GPIO1[TS1E] GPIO2[TS2E] GPIO3[TS1O] GPIO4[TS2O] GPIO5[TS3] GPIO6[TS4] GPIO7[TS5] GPIO8[TS6] GPIO9[TrcClk]					12	8		
Halt	dc	dc	n/a	n/a	n/a	n/a		async
RcvrInh	dc	dc	n/a	n/a	n/a	n/a		
SysClk			n/a	n/a	n/a	n/a		
SysErr			n/a	n/a	12	8		async
SysReset					12	8		async
TestEn	dc	dc	n/a	n/a	n/a	n/a		async
TmrClk	dc	dc	n/a	n/a	n/a	n/a		async

I/O Specifications—200MHz

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
SDRAM Interface								
BA1:0	n/a	n/a	7.5	1	19	12	SysClk	1, 2
$\overline{\text{BankSel3:0}}$	n/a	n/a	6.2	1	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	7.5	1	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	5.2	1	40	25	SysClk	2
DQM3:0	n/a	n/a	6.1	1	19	12	SysClk	2
DQMCB	n/a	n/a	6.2	1	19	12	SysClk	2
ECC7:0	2	1	6.2	1	19	12	SysClk	2
MemAddr12:0	n/a	n/a	7.6	1	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0	-1	19	12	SysClk	2, 3
MemData31:0	2	1	6.3	1	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	7.5	1	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	7.5	1	19	12	SysClk	1, 2
External SLAVE Peripheral Interface								
DMAAck0:3	n/a	n/a	8	0	12	8	PerClk	
DMAReq0:3	dc	dc	n/a	n/a	n/a	n/a	PerClk	
EOT0:3[TC0:3]	dc	dc	8	0	12	8	PerClk	
PerAddr0:31	4	1	10	0	19	12	PerClk	
$\overline{\text{PerBLast}}$	4	1	8	0	12	8	PerClk	
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1:7}}$[GPIO10:16]	n/a	n/a	8	0	12	8	PerClk	
PerData0:31	6	1	10	0	19	12	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	8	0	12	8	PerClk	
PerPar0:3	4	1	10	0	19	12	PerClk	
PerR/$\overline{\text{W}}$	4	1	8	0	12	8	PerClk	
PerReady	9	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	3	1	8	0	12	8	PerClk	
External MASTER Peripheral Interface								
BusReq	n/a	n/a	8	0	12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	7	0	12	8	PerClk	
$\overline{\text{ExtReq}}$	5	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	8	0	19	12	PerClk	
HoldAck	n/a	n/a	8	0	12	8	PerClk	
HoldPri	4	1	n/a	n/a	n/a	n/a	PerClk	
HoldReq	5	1	n/a	n/a	n/a	n/a	PerClk	
PerClk	n/a	n/a	0.9	0.7	19	12	PLB Clk	4
PerErr	3	1	n/a	n/a	n/a	n/a	PerClk	

I/O Specifications—266MHz (Preliminary)

Notes:

1. The two-cycle SDRAM command interface is driven in cycle 1 and used in cycle 2. Output times in table are in cycle 1.
2. SDRAM output timing is relative to the rising edge of the internal PLB clock, which is an integral multiple of and rising-edge aligned with SysClk. Therefore, SDRAM output timings in the table are shown relative to SysClk. Timings shown are for a lumped 50pF load, however the interface has been verified for PC100-compliant operation using transmission line circuit analysis.
3. SDRAM CLK0:1 rising edge at package pin precedes the internal PLB clock by approximately 0.5ns for a typical clock network or a lumped 10pF load.
4. PerClk rising edge at package pin with a 10pF load trails the internal PLB clock by approximately 0.8ns.

Signal	Input (ns)		Output (ns)		Output Current (mA)		Clock	Notes
	Setup Time (minimum)	Hold Time (minimum)	Valid Delay (maximum) 50pF load	Hold Time (minimum) 50pF load	I/O H (maximum)	I/O L (minimum)		
SDRAM Interface								
BA1:0	n/a	n/a	5.7	1	19	12	SysClk	1, 2
$\overline{\text{BankSe3:0}}$	n/a	n/a	4.8	1	19	12	SysClk	2
$\overline{\text{CAS}}$	n/a	n/a	5.7	1	19	12	SysClk	1, 2
ClkEn0:1	n/a	n/a	4.2	1	40	25	SysClk	2
DQM3:0	n/a	n/a	4.8	1	19	12	SysClk	2
DQMCB	n/a	n/a	4.8	1	19	12	SysClk	2
ECC7:0	1.5	1	4.8	1	19	12	SysClk	2
MemAddr12:0	n/a	n/a	5.7	1	19	12	SysClk	1, 2
MemClkOut0:1	n/a	n/a	0	-1	19	12	SysClk	2, 3
MemData31:0	1.5	1	4.9	1	19	12	SysClk	2
$\overline{\text{RAS}}$	n/a	n/a	5.7	1	19	12	SysClk	1, 2
$\overline{\text{WE}}$	n/a	n/a	5.7	1	19	12	SysClk	1, 2
External SLAVE Peripheral Interface								
DMAAck0:3	n/a	n/a	6	0	12	8	PerClk	
DMAReq0:3	dc	dc	n/a	n/a	n/a	n/a	PerClk	
EOT0:3[TC0:3]	dc	dc	6	0	12	8	PerClk	
PerAddr0:31	3	1	7.2	0	19	12	PerClk	
$\overline{\text{PerBLast}}$	3	1	6	0	12	8	PerClk	
$\overline{\text{PerCS0}}$ $\overline{\text{PerCS1:7}}$[GPIO10:16]	n/a	n/a	6	0	12	8	PerClk	
PerData0:31	5	1	7.2	0	19	12	PerClk	
$\overline{\text{PerOE}}$	n/a	n/a	6	0	12	8	PerClk	
PerPar0:3	3	1	7.2	0	19	12	PerClk	
PerR/$\overline{\text{W}}$	4	1	6	0	12	8	PerClk	
PerReady	6.5	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{PerWBE0:3}}$	3	1	6	0	12	8	PerClk	
External MASTER Peripheral Interface								
BusReq	n/a	n/a	6	0	12	8	PerClk	
$\overline{\text{ExtAck}}$	n/a	n/a	6	0	12	8	PerClk	
$\overline{\text{ExtReq}}$	4	1	n/a	n/a	n/a	n/a	PerClk	
$\overline{\text{ExtReset}}$	n/a	n/a	6	0	19	12	PerClk	
HoldAck	n/a	n/a	6	0	12	8	PerClk	
HoldPri	3	1	n/a	n/a	n/a	n/a	PerClk	
HoldReq	4	1	n/a	n/a	n/a	n/a	PerClk	
PerClk	n/a	n/a	0.9	0.7	19	12	PLB Clk	4
PerErr	3	1	n/a	n/a	n/a	n/a	PerClk	

Strapping

While the SysReset input pin is low (system reset), the state of certain I/O pins is read to enable default initial conditions prior to PPC405GP start-up. The actual capture instant is the nearest reference clock edge before the deassertion of reset. These pins must be strapped using external pull-up (logical 1) or pull-down (logical 0) resistors to select the desired default conditions. These pins are use for strap functions only during reset. They are used for other signals during normal operation. The following table lists the strapping pins along with their functions and strapping options. The pin for the 456-ball package is listed first (for example, AF3), followed by the corresponding pin for the 413-ball package (for example, U8), which appears as AF3/U8.

Strapping Pin Assignments

Function	Option	Ball Strapping		
PLL Tuning for $6 \le M \le 7$ use choice 3 for $7 < M \le 12$ use choice 5 for $12 < M \le 32$ use choice 6 See Note.		**AF3/U8**	**AF2/T8**	**AD16/AB15**
	Choice 1; TUNE[5:0] = 010001	0	0	0
	Choice 2; TUNE[5:0] = 010010	0	0	1
	Choice 3; TUNE[5:0] = 010011	0	1	0
	Choice 4; TUNE[5:0] = 010100	0	1	1
	Choice 5; TUNE[5:0] = 010101	1	0	0
	Choice 6; TUNE[5:0] = 010110	1	0	1
	Choice 7; TUNE[5:0] = 010111	1	1	0
	Choice 8; TUNE[5:0] = 100100	1	1	1
PLL Forward Divider		**D16/A17**	**B15/B14**	
	Bypass mode	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 6	1	1	
PLL Feedback Divider		**B14/A15**	**C12/A8**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
PLB Divider from CPU		**P25/R23**	**L24/J22**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
OPB Divider from PLB		**L25/K21**	**J26/F22**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	

Strapping Pin Assignments (Continued)

Function	Option	Ball Strapping		
PCI Divider from PLB		**D18/A20**	**C20/C19**	
	Divide by 1	0	0	
	Divide by 2	0	1	
	Divide by 3	1	0	
	Divide by 4	1	1	
External Bus Divider from PLB		**K25/K20**	**K23/J21**	
	Divide by 2	0	0	
	Divide by 3	0	1	
	Divide by 4	1	0	
	Divide by 5	1	1	
ROM Width		**AC2/N3**	**AD2/N7**	
	8-bit ROM	0	0	
	16-bit ROM	0	1	
	32-bit ROM	1	0	
	Reserved	1	1	
ROM Location		**U2/P4**		
	PPC405GP Peripheral Attach	0		
	PPC405GP PCI Attach	1		
PCI Asynchronous Mode Enable		**Y3/U4**		
	Synchronous PCI Mode	0		
	Asynchronous Mode	1		
PCI Arbiter Enable		**AF18/AB18**		
	Internal Arbiter Disabled	0		
	Internal Arbiter Enabled	1		

Note: The tune bits adjust parameters that control PLL jitter. The recommended values minimize jitter for the PLL implemented in the PPC405GP. These bits are shown for information only; and do not require modification except in special clocking circumstances such as spread spectrum clocking. For details on the use of Spread Spectrum Clock Generators (SSCGs) with the PPC405GP, visit the technical documents area of the IBM PowerPC web site.

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