

F10402

16 x 4-Bit Register File (RAM)

F10K ECL Product

Description

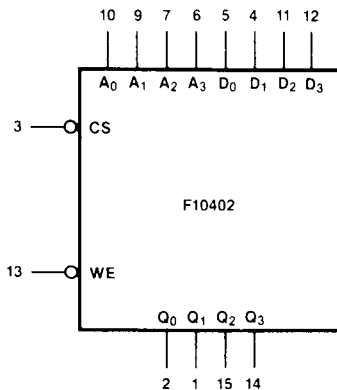
The F10402 is a high-speed 64-bit Random Access Memory (RAM) organized as a 16-word by 4-bit array. External logic requirements are minimized by internal address decoding, while memory expansion and data busing are facilitated by the output disabling features of the Chip Select (\overline{CS}) and Write Enable (\overline{WE}) inputs.

A HIGH signal on \overline{CS} prevents read and write operations and forces the outputs to the LOW state. When \overline{CS} is LOW, the \overline{WE} input controls chip operations. A HIGH signal on \overline{WE} disables the Data input (D_n) buffers and enables readout from the memory location determined by the Address (A_n) inputs. A LOW signal on \overline{WE} forces the Q_n outputs LOW and allows data on the D_n inputs to be stored in the addressed location. Data exists in the same logical sense as presented at the data inputs, *i.e.*, the memory is non-inverting.

Pin Names

| | |
|-----------------|--------------------|
| \overline{CS} | Chip Select Input |
| $A_0 - A_3$ | Address Inputs |
| $D_0 - D_3$ | Data Inputs |
| \overline{WE} | Write Enable Input |
| $Q_0 - Q_3$ | Data Outputs |

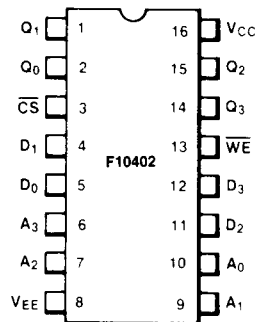
Logic Symbol



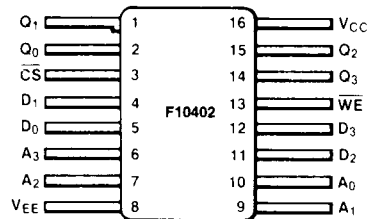
V_{CC} = Pin 16
 V_{EE} = Pin 8

Connection Diagrams

16-Pin DIP (Top View)



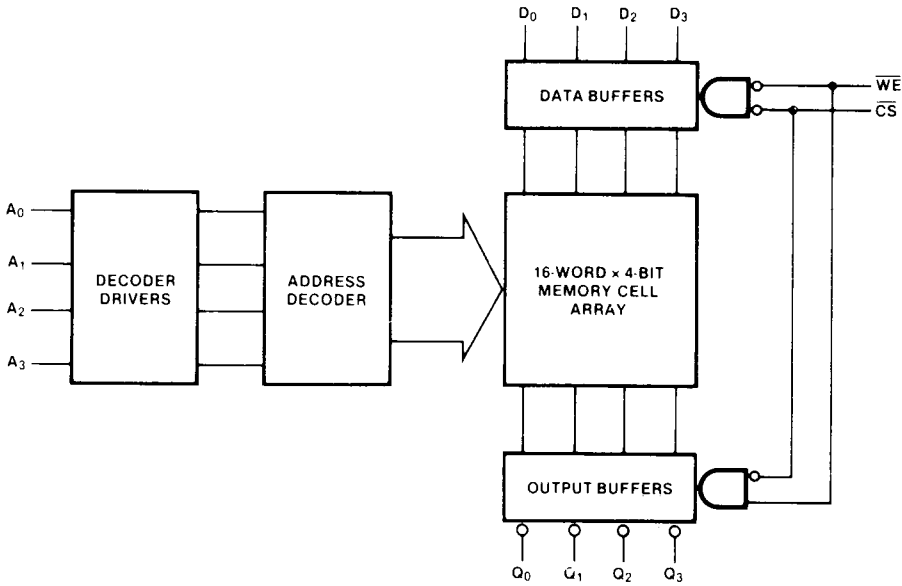
16-Pin Flatpak (Top View)



Ordering Information

| Package | Outline | Order Code |
|-------------|---------|------------|
| Ceramic DIP | 4J | DC |
| Flatpak | 3L | FC |

Logic Diagram



4

DC Performance Characteristics: $V_{EE} = -5.2\text{ V}$, $V_{CC} = V_{CCA} = \text{GND}$, $T_C = 0^\circ\text{C}$ to $+75^\circ\text{C}$
 unless otherwise specified*

| Symbol | Characteristic | Min | Typ | Max | Unit | Condition |
|----------|----------------------------------|------|------|-----|---------------|------------------------|
| I_{IH} | Input HIGH Current All Inputs | | | 300 | μA | $V_{IN} = V_{IH(max)}$ |
| I_{EE} | Power Supply Current | -170 | -110 | -70 | mA | Inputs Open |

*See Family Characteristic for other dc specifications

AC Performance Characteristics: $V_{EE} = -5.2 \text{ V} \pm 5\%$, $V_{CC} = \text{GND}$, Applies to Flatpack and DIP Packages

| Symbol | Characteristic | $T_C = 0^\circ \text{C}$ | | $T_C = 25^\circ \text{C}$ | | $T_C = 75^\circ \text{C}$ | | Unit | Condition |
|-------------------------------|--------------------------------|--------------------------|------|---------------------------|------|---------------------------|------|------|-----------------------------------------|
| | | Min | Max | Min | Max | Min | Max | | |
| Access/Recovery Timing | | | | | | | | | |
| t_{ACS} | Chip Select Access | | 3.30 | | 3.50 | | 3.80 | ns | Figures 1 and 4 |
| t_{RCS} | Chip Select Recovery | | 3.30 | | 3.50 | | 3.80 | ns | |
| t_{AA} | Address Access ¹ | | 5.00 | | 5.30 | | 6.00 | ns | |
| Write Timing, Setup | | | | | | | | | |
| t_{WSD} | Data | 0.50 | | 0.50 | | 0.80 | | ns | Figures 1 and 3 $T_W = 6 \text{ ns}$ |
| t_{WSCS} | Chip Select | 1.50 | | 1.50 | | 1.50 | | ns | |
| t_{WSA} | Address | 1.00 | | 1.00 | | 1.00 | | ns | |
| Write Timing, Hold | | | | | | | | | |
| t_{WHD} | Data | 0.50 | | 0.50 | | 0.50 | | ns | Figures 1 and 3 $T_W = 6 \text{ ns}$ |
| t_{WHCS} | Chip Select | 0.50 | | 0.50 | | 0.50 | | ns | |
| t_{WHA} | Address | 2.50 | | 2.50 | | 2.50 | | ns | |
| t_{WR} | Write Recovery Time | | 4.00 | | 4.00 | | 4.50 | ns | Figures 1 and 4 |
| t_{WS} | Write Disable Time | | 3.00 | | 3.00 | | 3.50 | ns | |
| t_W | Write Pulse Width, (LOW) | 2.50 | | 2.50 | | 3.00 | | ns | Figures 1 and 3 |
| t_{CS} | Chip Select Pulse Width, (LOW) | 2.50 | | 2.50 | | 3.00 | | ns | |
| t_{TLH} | Transition Time | | | | | | | | Figures 1 and 4 |
| t_{THL} | 20% to 80%, 80% to 20% | 0.50 | 1.70 | 0.50 | 1.70 | 0.50 | 1.70 | ns | |

1. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudo random testing pattern.

Fig. 1 AC Test Circuit

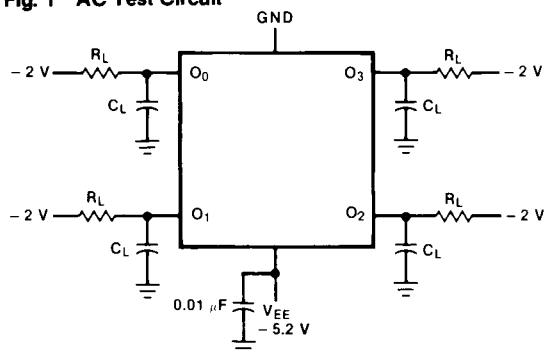
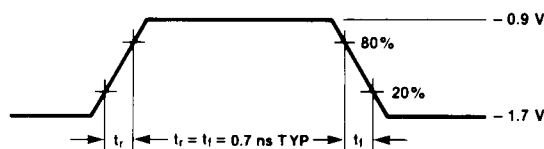


Fig. 2 Input Levels



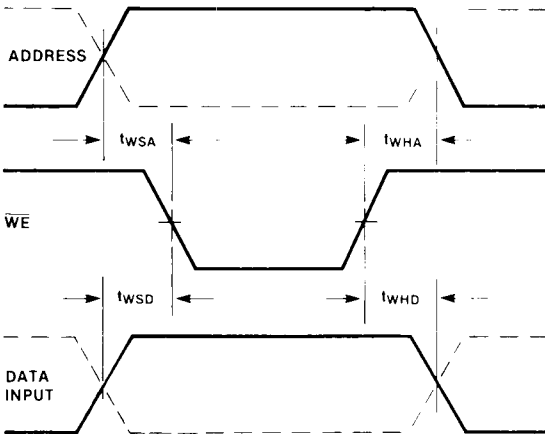
Notes

- All Timing Measurements Referenced to 50% of Input Levels
- $C_L = 3 \text{ pF}$ including Fixture and Stray Capacitance
- $R_L = 50 \Omega$ to -2.0 V

Fig. 3 Write Modes

Write Enable Strobe

ADDRESS AND DATA INPUT SET-UP AND HOLD TIMES
(CS = LOW)



CHIP SELECT SET-UP AND HOLD TIMES

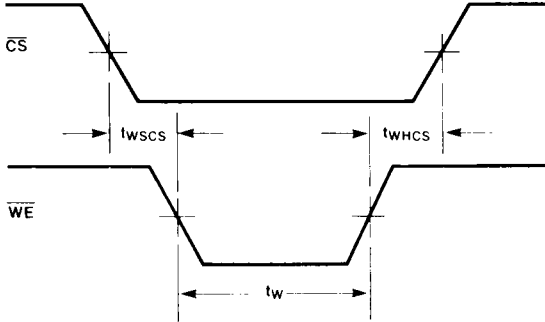
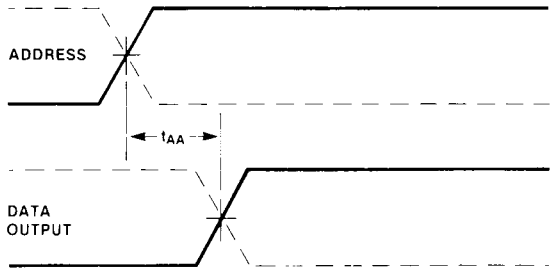


Fig. 4 Read Modes

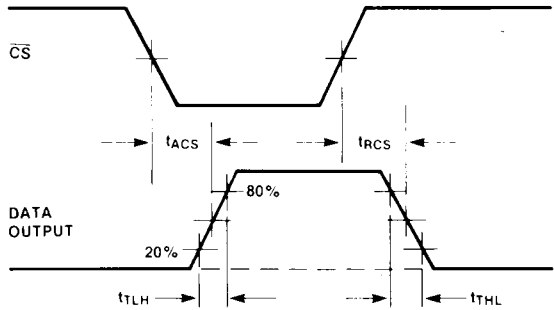
Address Input to Data Output ($\overline{WE} = \text{HIGH}$, $\overline{CS} = \text{LOW}$)

ADDRESS ACCESS TIME



Chip Select Input to Data Output ($\overline{WE} = \text{HIGH}$)

CHIP SELECT ACCESS AND RECOVERY TIMES



Write Enable Input to Data Output ($\overline{CS} = \text{LOW}$)

WRITE RECOVERY, DISABLE TIMES

