Document Title

2Mx16 bit Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial Draft - Design target	October 10, 2002	Advance
0.1	Revised - Changed Power Up Sequence - Changed Package Type from 48 TBGA into 48 FBGA 6.0 x 8.0 - Changed Standby Current($I_{SB}1$) from 70µA to 80µA - Added Operation Current : I_{CC1} 5mA, I_{CC2} 30mA	May 29, 2003	Advance

2M x 16 bit Uni-Transistor CMOS RAM

FEATURES

- Process Technology: CMOS
- Organization: 2M x16 bit
- Power Supply Voltage: 1.7V~2.1V
- Three State Outputs
- Compatible with Low Power SRAM
- Deep Power Down: Memory cell data holds invalid
- Package Type: 48-FBGA 6.0 x 8.0

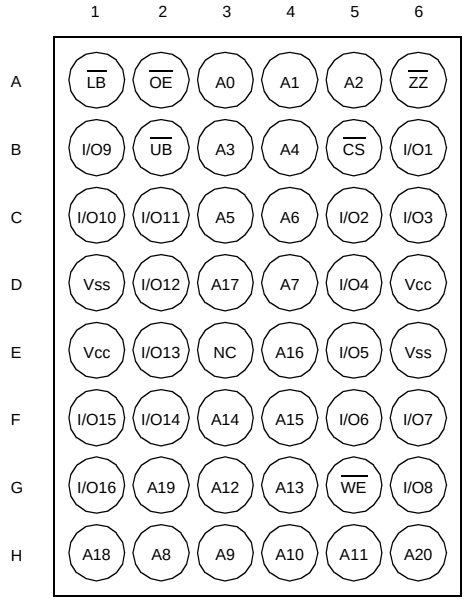
GENERAL DESCRIPTION

The K1S3216B5C is fabricated by SAMSUNG′s advanced CMOS technology using one transistor memory cell. The device supports industrial temperature range and 48 ball Chip Scale Package for user flexibility of system design. The device also supports DPD(Deep Power Down) mode.

PRODUCT FAMILY

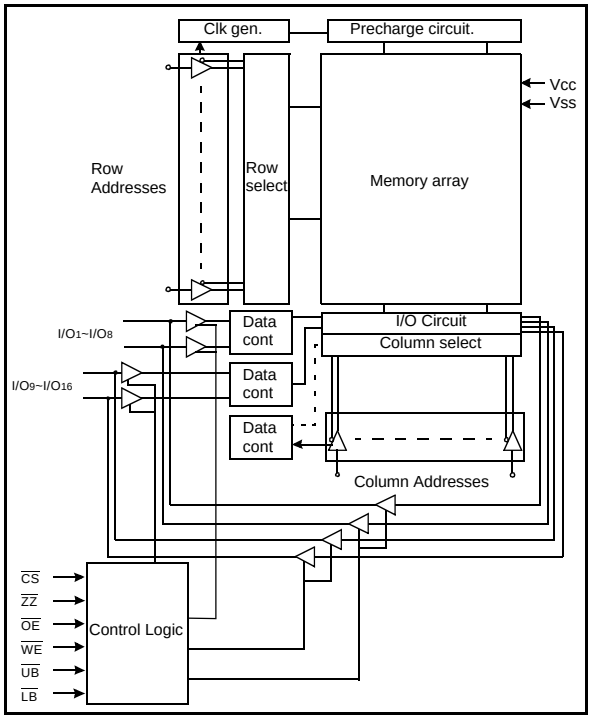
Product Family	Operating Temp.	Vcc Range	Speed (t_{RC})	Power Dissipation			PKG Type
				Standby (I_{SB1}, Max.)	Deep power down(I_{SBD}, Max.)	Operating (I_{CC2}, Max.)	
K1S3216B5C-I	Industrial(-40~85°C)	1.7V~2.1V	70/85ns	80µA	10µA	30mA	48-FBGA 6.0 x 8.0

PIN DESCRIPTION



48-FBGA: Top View(Ball Down)

FUNCTIONAL BLOCK DIAGRAM



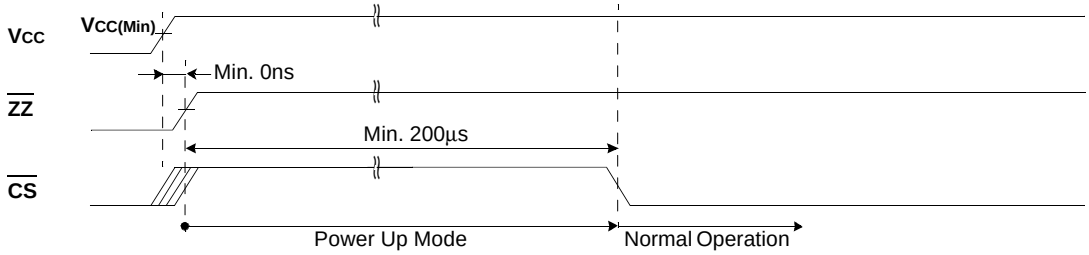
Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	Vcc	Power
$\overline{ZZ}$	Deep Power Down	Vss	Ground
$\overline{OE}$	Output Enable Input	$\overline{UB}$	Upper Byte($I/O_{9\sim16}$)
$\overline{WE}$	Write Enable Input	$\overline{LB}$	Lower Byte($I/O_{1\sim8}$)
A_0~A_{20}	Address Inputs	NC	Not Connected[1)]
I/O_1~I/O_{16}	Data Inputs/Outputs		

1) Reserved for future use.

POWER UP SEQUENCE

1. Apply power.
2. Maintain stable power(Vcc min.=1.7V) for a minimum 200µs with $\overline{CS}$ and $\overline{ZZ}$ high.

TIMING WAVEFORM OF POWER UP



(POWER UP)

1. After V_{CC} reaches V_{CC}(Min.), wait 200µs with $\overline{CS}$ and $\overline{ZZ}$ high. Then you get into the normal operation.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{ZZ}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
X[1)]	L	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Deep Power Down
L	H	X[1)]	X[1)]	H	H	High-Z	High-Z	Deselected	Standby
L	H	H	H	L	X[1)]	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X[1)]	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	H	L	H	L	L	Dout	Dout	Word Read	Active
L	H	X[1)]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	H	X[1)]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	H	X[1)]	L	L	L	Din	Din	Word Write	Active

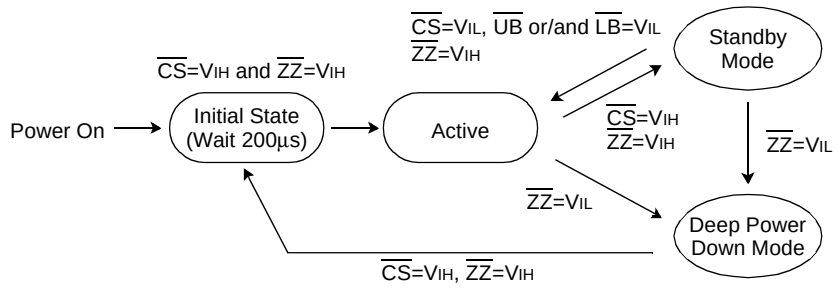
1. X means don't care.(Must be low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CC}+0.3V	V
Voltage on Vcc supply relative to Vss	V_{CC}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

STANDBY MODE STATE MACHINES



STANDBY MODE CHARACTERISTIC

Power Mode	Memory Cell Data	Standby Current(mA)	Wait Time(ms)
Standby	Valid	80	0
Deep Power Down	Invaild	10	200

PRODUCT LIST

Industrial Temperature Products(-40~85°C)	
Part Name	**Function**
K1S3216B5C-FI70 K1S3216B5C-FI85	48-FBGA, 70ns, 1.8V/2.0V 48-FBGA, 85ns, 1.8V/2.0V

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	Vcc	1.7	1.8/2.0	2.1	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	1.4	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	-0.3[3)]	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: Vcc+1.0V in case of pulse width ≤20ns.
3. Undershoot: -1.0V in case of pulse width ≤20ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)](f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested.

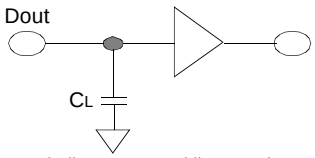
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc	-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{ZZ}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc	-1	-	1	µA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS}$≤0.2V, $\overline{ZZ}$≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥V_{CC}-0.2V	-	-	5	mA
	I_{CC2}	Cycle time=Min, I_{IO}=0mA, 100% duty, $\overline{CS}$=V_{IL}, $\overline{ZZ}$=V_{IH}, V_{IN}=V_{IL} or V_{IH}	-	-	30	mA
Output low voltage	V_{OL}	I_{OL}=0.1mA	-	-	0.2	V
Output high voltage	V_{OH}	I_{OH}=-0.1mA	1.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1)]	$\overline{CS}$≥Vcc-0.2V, $\overline{ZZ}$≥Vcc-0.2V, Other inputs=Vss to Vcc	-	-	80	µA
Deep Power Down	I_{SBD}	$\overline{ZZ}$≤0.2V, Other inputs=Vss to Vcc	-	-	10	µA

AC OPERATING CONDITIONS

TEST CONDITIONS(Test Load and Test Input/Output Reference)

Input pulse level: 0.2V to Vcc-0.2V
Input rising and falling time: 5ns
Input and output reference voltage: 0.5 x V_{CC}
Output load: C_L=50pF



1. Including scope and jig capacitance

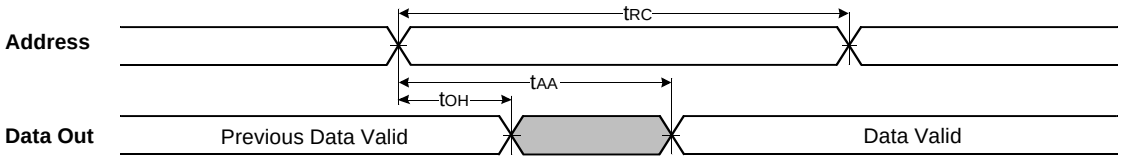
AC CHARACTERISTICS(V_{CC}=1.7~2.1V, T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t_{RC}	70	-	85	-	ns
	Address Access Time	t_{AA}	-	70	-	85	ns
	Chip Select to Output	t_{CO}	-	70	-	85	ns
	Output Enable to Valid Output	t_{OE}	-	35	-	40	ns
	$\overline{UB}$, $\overline{LB}$ Access Time	t_{BA}	-	70	-	85	ns
	Chip Select to Low-Z Output	t_{LZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output	t_{BLZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t_{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t_{HZ}	0	25	0	25	ns
	$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output	t_{BHZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t_{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t_{OH}	5	-	5	-	ns
Write	Write Cycle Time	t_{WC}	70	-	85	-	ns
	Chip Select to End of Write	t_{CW}	60	-	70	-	ns
	Address Set-up Time	t_{AS}	0	-	0	-	ns
	Address Valid to End of Write	t_{AW}	60	-	70	-	ns
	$\overline{UB}$, $\overline{LB}$ Valid to End of Write	t_{BW}	60	-	70	-	ns
	Write Pulse Width	t_{WP}	55[1)]	-	60[1)]	-	ns
	Write Recovery Time	t_{WR}	0	-	0	-	ns
	Write to Output High-Z	t_{WHZ}	0	25	0	25	ns
	Data to Write Time Overlap	t_{DW}	30	-	35	-	ns
	Data Hold from Write Time	t_{DH}	0	-	0	-	ns
	End Write to Output Low-Z	t_{OW}	5	-	5	-	ns

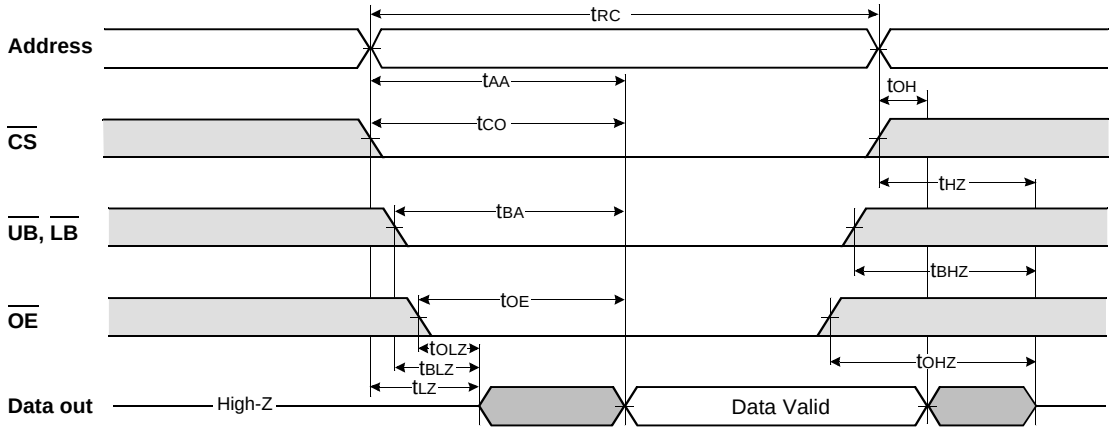
1. t_{WP}(min)=70ns for continuous write operation over 50 times.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1)(Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{ZZ}$=$\overline{WE}$=V_{IH}, $\overline{UB}$ or $\overline{LB}$=V_{IL})



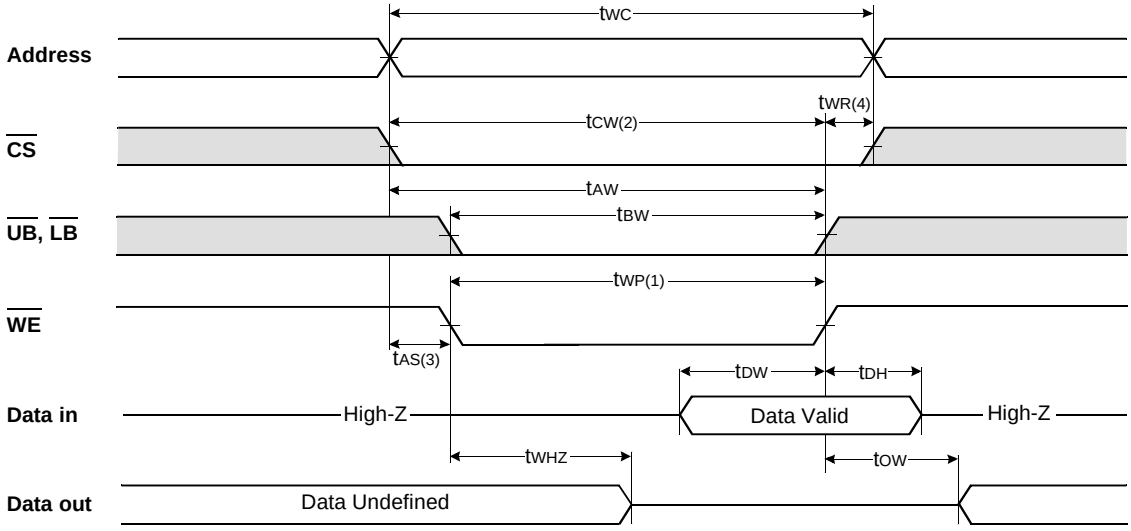
TIMING WAVEFORM OF READ CYCLE(2)($\overline{ZZ}$=$\overline{WE}$=V_{IH})



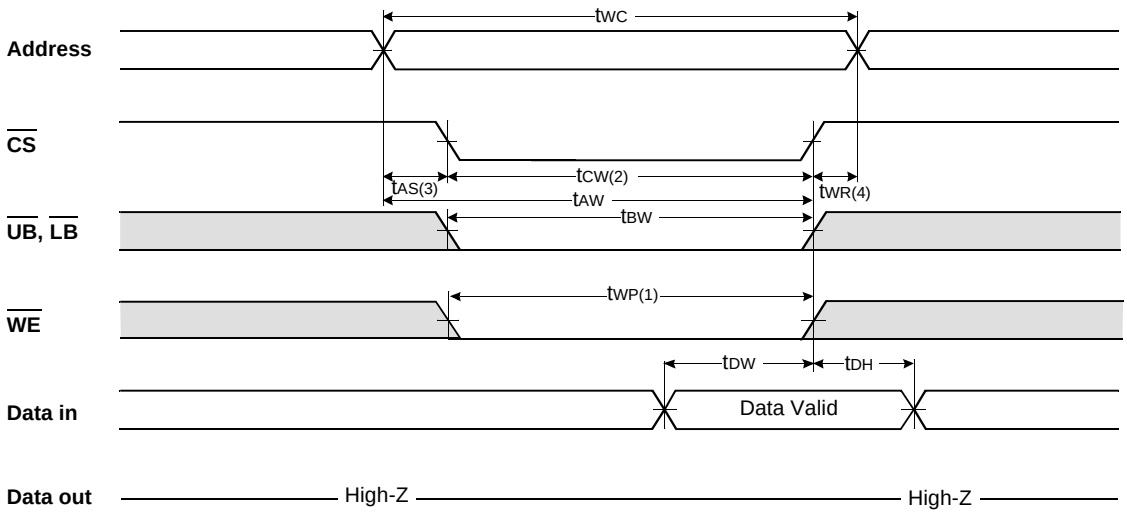
(READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
3. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
4. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 4us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 4us.

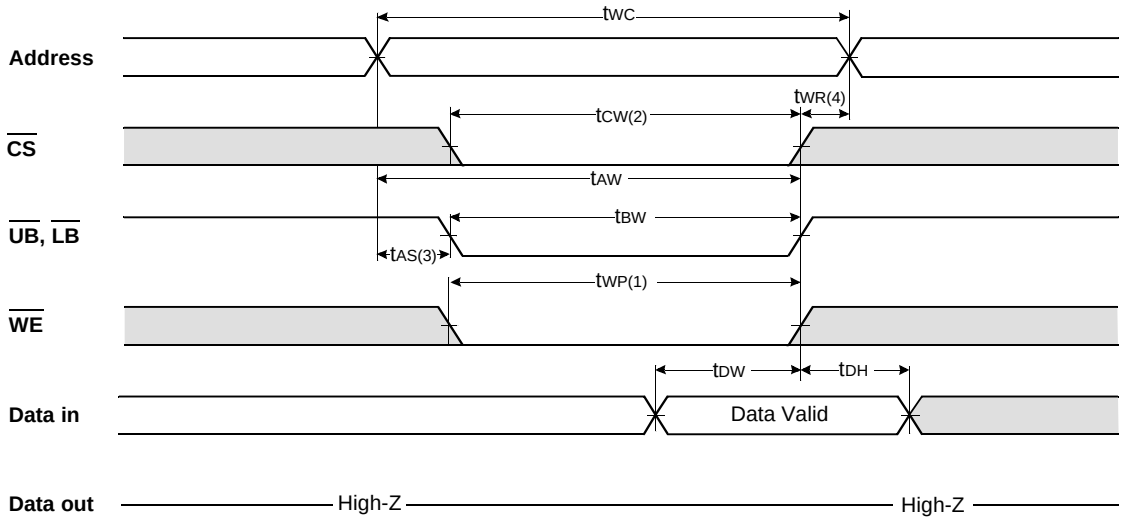
TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled, $\overline{ZZ}$=V_{IH})



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled, $\overline{ZZ}$=V_{IH})



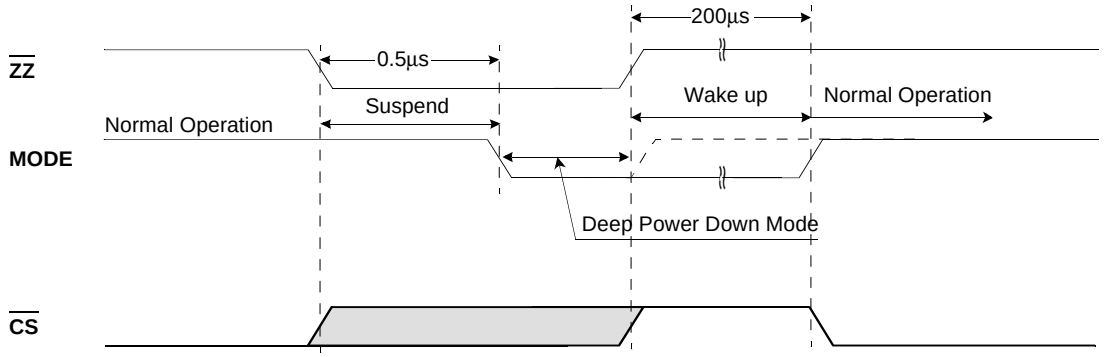
TIMING WAVEFORM OF WRITE CYCLE(3)($\overline{UB}$, $\overline{LB}$ Controlled, $\overline{ZZ}$=V_{IH})



(WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

TIMING WAVEFORM OF DEEP POWER DOWN MODE ENTRY AND EXIT



(DEEP POWER DOWN MODE)

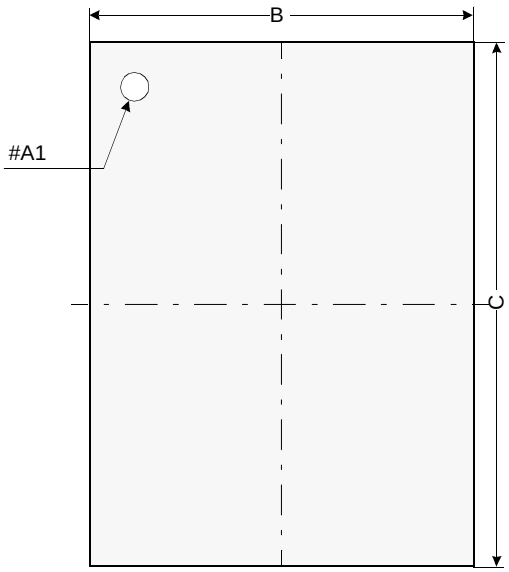
1. When you toggle $\overline{ZZ}$ pin low, the device gets into the Deep Power Down mode after 0.5µs suspend period.
2. To return to normal operation, the device needs Wake Up period.
3. Wake Up sequence is just the same as Power Up sequence.

PACKAGE DIMENSION

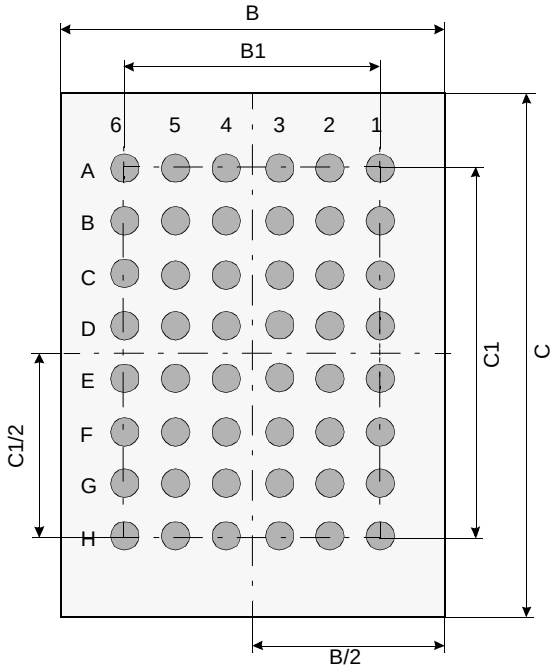
Unit: millimeters

48 FINE PITCH BALL GRID ARRAY(0.75mm ball pitch)

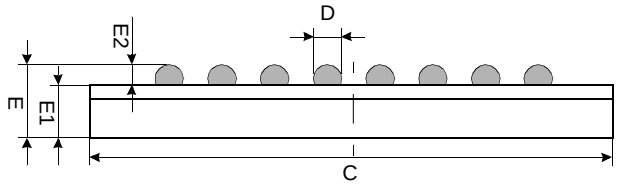
Top View



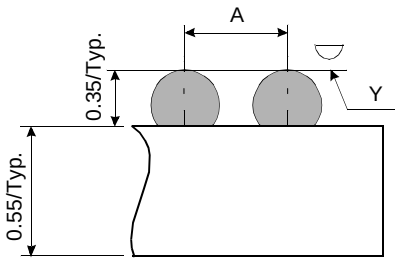
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	7.90	8.00	8.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)