IS24C128-2/3
IS24C256-2/3

262,144-bit/131,072-bit 2-WIRE SERIAL CMOS EEPROM

PRELIMINARY INFORMATION
NOVEMBER 2001

FEATURES

- Low Power CMOS Technology
  - Standby Current less than 10 µA (5.5V)
  - Read Current (typical) less than 1 mA (5.5V)
  - Write Current (typical) less than 3 mA (5.5V)
- Low Voltage Operation
  - IS24C256-2 & IS24C128-2: Vcc = 1.8V to 5.5V
  - IS24C256-3 & IS24C128-3: Vcc = 2.5V to 5.5V
- 100 KHz (1.8V) and 400 KHz (5V) Compatibility
- Hardware Data Protection
  - Write Protect Pin
- Sequential Read Feature
- Filtered Inputs for Noise Suppression
- 8-pin PDIP,8-pin SOIC, and 8-ball BGA
- Self time write cycle with auto clear
  - 5 ms @ 2.5V
- Organization:
  - IS24C256-2 and IS24C256-3: 32,768x8
  - IS24C128-2 and IS24C128-3: 16,384x8
- 64-Byte Page Write Buffer
- Two-Wire Serial Interface
  - Bi-directional data transfer protocol
- High Reliability
  - Endurance: 1,000,000 Cycles
  - Data Retention: 100 Years
- Commercial and Industrial temperature ranges

PRODUCT OFFERING OVERVIEW

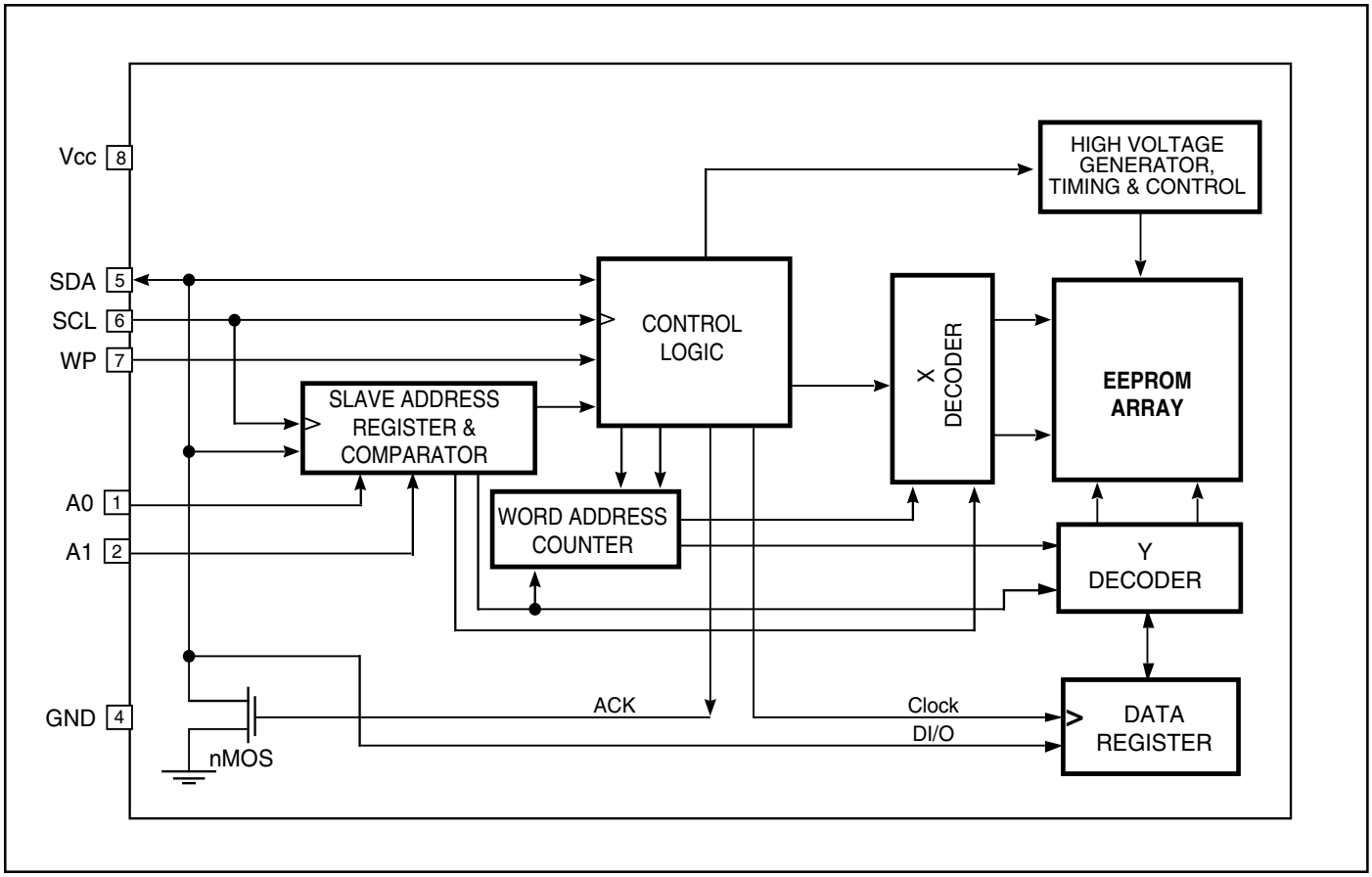
Part No	Voltage	Speed	Standby ICC	Read ICC	Write ICC	Temperature
IS24C256-2	1.8V-5.5V	100 KHz	< 5 µA	1 mA	3 mA	C,I
IS24C256-3	2.5V-5.5V	400 KHz	< 10 µA	1 mA	3 mA	C,I
IS24C128-2	1.8V-5.5V	100 KHz	< 5 µA	1 mA	3 mA	C,I
IS24C128-3	2.5V-5.5V	400 KHz	< 10 µA	1 mA	3 mA	C,I

DESCRIPTION

The IS24C128-2 is a 1.8V (1.8V-5.5V) 128K-bit (16384 x 8) Electrically Erasable PROM, IS24C128-3 is a 2.5V (2.5V-5.5V) 128K-bit (16384 x 8) Electrically Erasable PROM, IS24C256-2 is a 1.8V (1.8V-5.5V) 256K-bit (32768 x 8) Electrically Erasable PROM and the IS24C256-3 is a 2.5V (2.5V-5.5V) 256K-bit (32768 x 8) Electrically Erasable PROM.

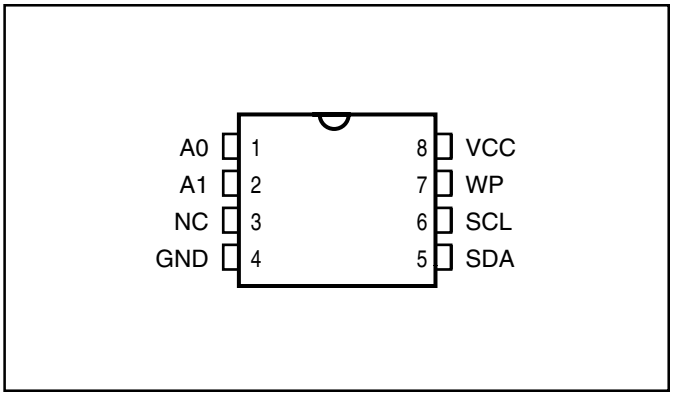
The IS24CXXX (IS24C128-2, IS24C128-3, IS24C256-2 and IS24C1256-3) family is a low-cost and low voltage 2-wire Serial EEPROM. It is fabricated using ISSI's advanced CMOS EEPROM technology and provides a low power and low voltage operation. The IS24CXXX family features a write protection feature, and is available in 8-pin DIP, 8-pin SOIC, and 8-ball BGA packages.

FUNCTIONAL BLOCK DIAGRAM

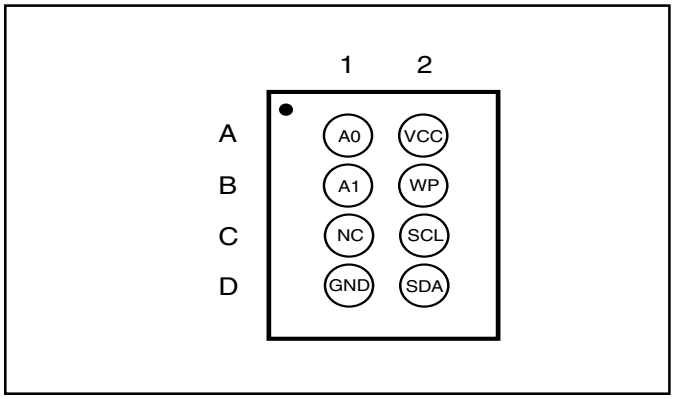


PIN CONFIGURATION

8-Pin DIP and SOIC



8-Ball BGA (Top View)



PIN DESCRIPTIONS

A0-A1	Address Inputs
SDA	Serial Address/Data I/O
SCL	Serial Clock Input
WP	Write Protect Input
Vcc	Power Supply
GND	Ground

SCL

This input clock pin is used to synchronize the data transfer to and from the device.

SDA

The SDA is a Bi-directional pin used to transfer addresses and data into and out of the device. The SDA pin is an open drain output and can be wire-Ored with other open drain or open collector outputs. The SDA bus *requires* a pullup resistor to Vcc.

A0, A1

The A0, and A1 are the device address inputs that are hardwired or left not connected for hardware compatibility with the 24C32/64. When pins are hardwired, as many as four 128K/265K devices may be addressed on a single bus system. When the pins are not hardwired, the default A0 and A1 are zero.

WP

WP is the Write Protect pin. If the WP pin is tied to Vcc the entire array becomes Write Protected (Read only). When WP is tied to GND or left floating normal read/write operations are allowed to the device.

DEVICE OPERATION

The IS24CXXX family features a serial communication and supports a bi-directional 2-wire bus transmission protocol.

2-WIRE BUS

The two-wire bus is defined as a Serial Data line (SDA), and a Serial Clock Line (SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as a receiver. The bus is controlled by MASTER device which generates the SCL, controls the bus access and generates the STOP and START conditions. The IS24CXXX is the SLAVE device on the bus.

The Bus Protocol:

– Data transfer may be initiated only when the bus is not busy

– During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

The state of the data line represents valid data when after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the SDA line may be changed during the LOW period of the clock signal. There is one clock pulse per bit of data. Each data transfer is initiated with a START condition and terminated with a STOP condition.

START Condition

The START condition precedes all commands to the device and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The IS24CXXX monitors the SDA and SCL lines and will not respond until the START condition is met.

STOP Condition

The STOP condition is defined as a LOW to HIGH transition of SDA when SCL is HIGH. All operations must end with a STOP condition.

ACKnowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line.

DEVICE ADDRESSING

The MASTER begins a transmission by sending a START condition. The MASTER then sends the address of the particular slave devices it is requesting. The SLAVE (Fig. 5) address is 8 bits.

The four most significant bits of the address are fixed as 1010 for the IS24CXXX.

The 128K/256K uses the two device address bits A1 and A0 to allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the MASTER sends a START condition and the SLAVE address byte, the IS24CXXX monitors the bus and responds with an Acknowledge (on the SDA line) when its address matches the transmitted slave address. The IS24CXXX pulls down the SDA line during the ninth clock cycle, signaling that it received the eight bits of data. The IS24CXXX then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

WRITE OPERATION

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ set to Zero) to the Slave device. After the Slave generates an acknowledge, the Master sends two byte addresses that are to be written into the address pointer of the IS24CXXX. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the address memory location. The IS24CXXX acknowledges once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The IS24CXXX is capable of 64-byte page-WRITE operation. A page-WRITE is initiated in the same manner as a byte write, but instead of terminating the internal write cycle after the first data word is transferred, the master device can transmit up to 63 more bytes. After the receipt of each data word, the IS24CXXX responds immediately with an ACKnowledge on SDA line, and the six lower order data word address bits are internally incremented by one, while the higher order bits of the data word address remain constant. If the master device should transmit more than 64 words, prior to issuing the STOP condition, the address counter will “roll over,” and the previously written data will be overwritten. Once all 64 bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point, all received data is written to the IS24CXXX in a single write cycle. All inputs are disabled until completion of the internal WRITE cycle.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the IS24CXXX initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the IS24CXXX is still busy with the write operation, no ACK will be returned. If the IS24CXXX has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATION

READ operations are initiated in the same manner as WRITE operations, except that the read/write bit of the slave address is set to “1”. There are three READ operation options: current address read, random address read and sequential read.

Current Address Read

The IS24CXXX contains an internal address counter which maintains the address of the last byte accessed, incremented by one. For example, if the previous operation is either a read or write operation addressed to the address location n, the internal address counter would increment to address location n+1. When the IS24CXXX receives the Device Addressing Byte with a READ operation (read/write bit set to “1”), it will respond an ACKnowledge and transmit the 8-bit data word stored at address location n+1. The master will not acknowledge the transfer but does generate a STOP condition and the IS24CXXX discontinues transmission. If 'n' is the last byte of the memory, then the data from location '0' will be transmitted. (Refer to Figure 8. Current Address Read Diagram.)

Random Access Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and word address of the location it wishes to read. After the IS24CXXX acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The IS24CXXX then responds with its acknowledge and sends the data requested. The master device does not send an acknowledge but will generate a STOP condition. (Refer to Figure 9. Random Address Read Diagram.)

Sequential Read

Sequential Reads can be initiated as either a Current Address Read or Random Address Read. After the IS24CXXX sends initial byte sequence, the master device now responds with an ACKnowledge indicating it requires additional data from the IS24CXXX. The IS24CXXX continues to output data for each ACKnowledge received. The master device terminates the sequential READ operation by pulling SDA HIGH (no ACKnowledge) indicating the last data word to be read, followed by a STOP condition.

The data output is sequential, with the data from address n followed by the data from address n+1, ... etc. The address counter increments by one automatically, allowing the entire memory contents to be serially read during sequential read operation. When the memory address boundary (32767 for IS24C256-2 and IS24C256-3; 16383 for IS24C128-2 and IS24C128-3) is reached, the address counter “rolls over” to address 0, and the IS24CXXX-2 continues to output data for each ACKnowledge received. (Refer to Figure 10. Sequential Read Operation Starting with a Random Address READ Diagram.)

Figure 1. Typical System Bus Configuration

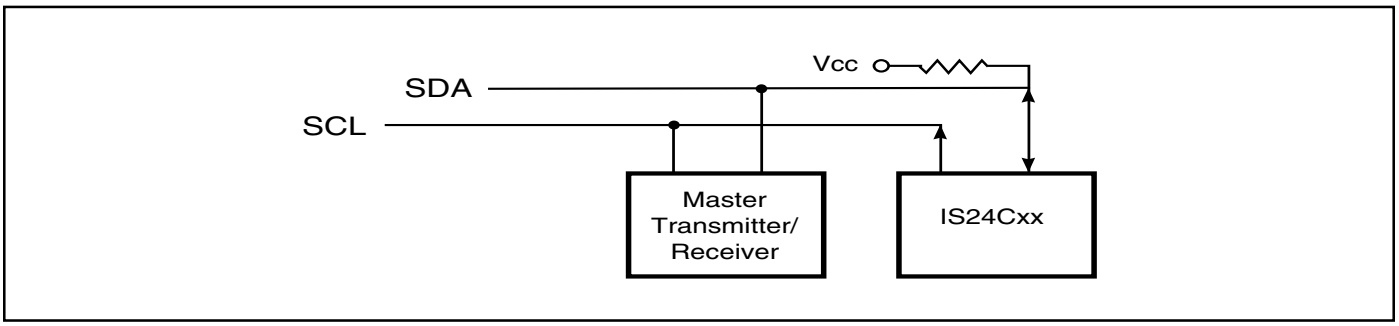


Figure 2. Output Acknowledge

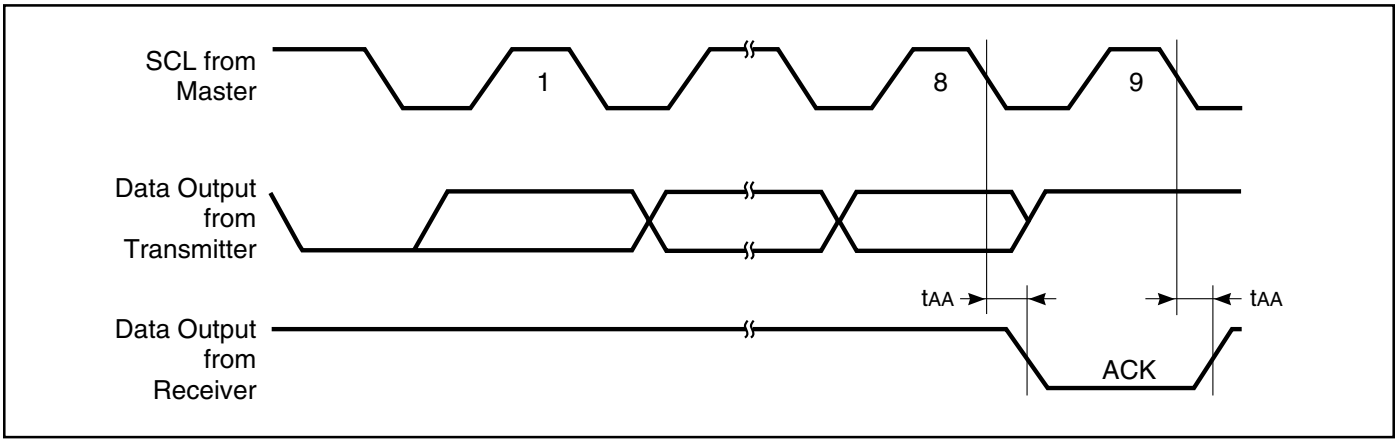


Figure 3. START and STOP Conditions

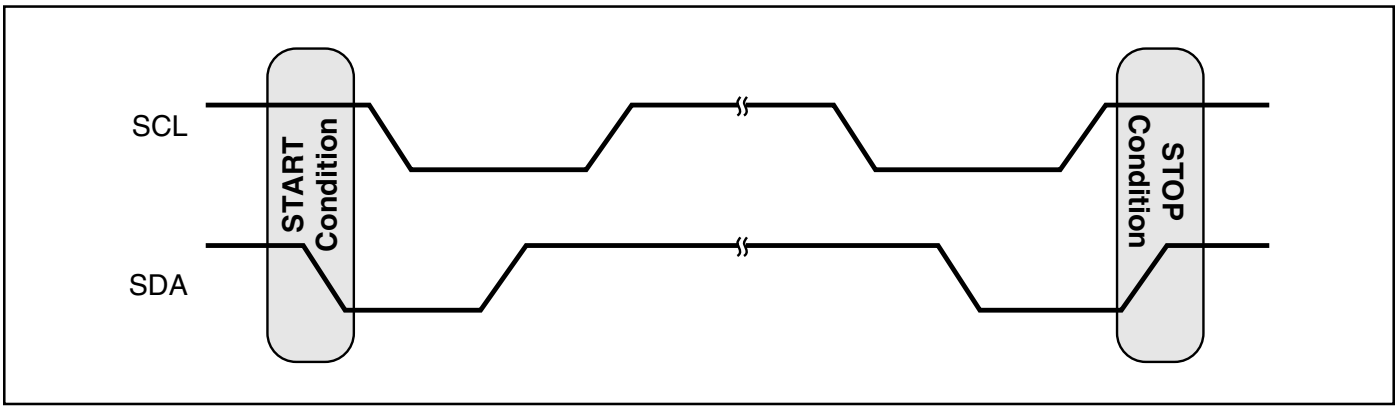


Figure 4. Data Validity Protocol

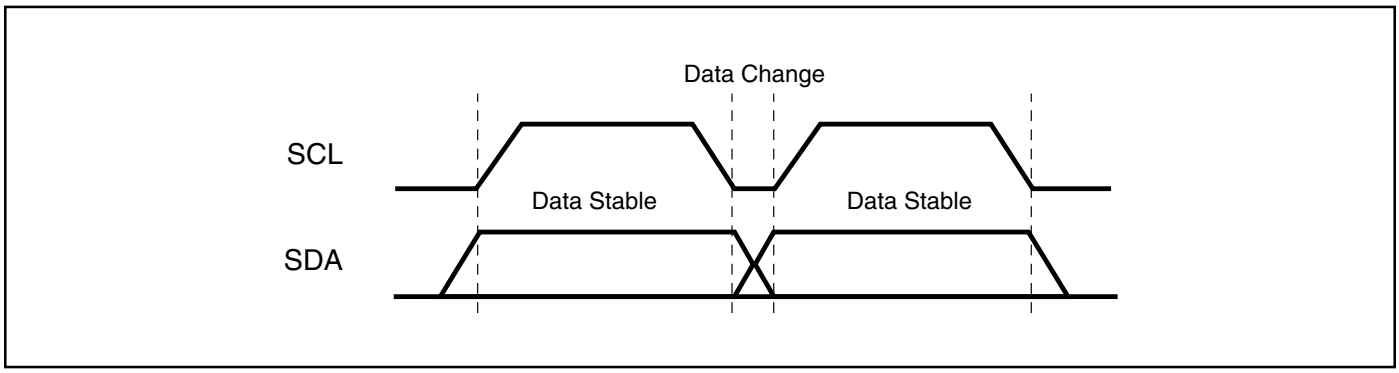


Figure 5. Slave Address

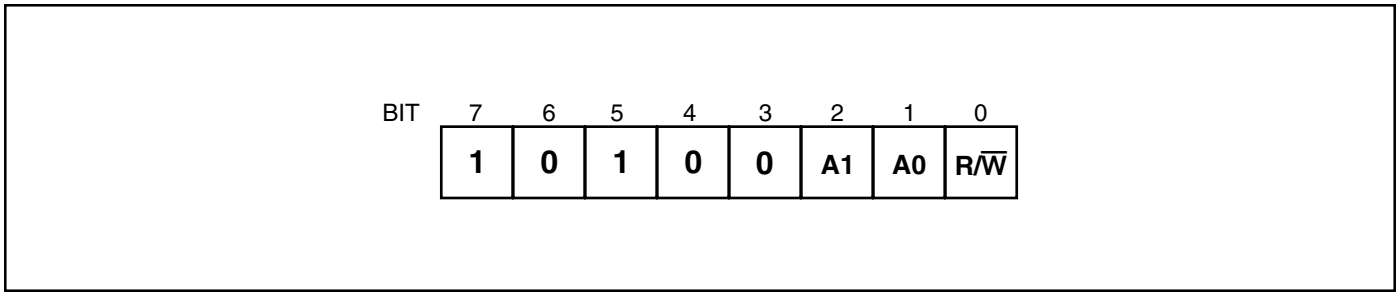


Figure 6. Byte Write

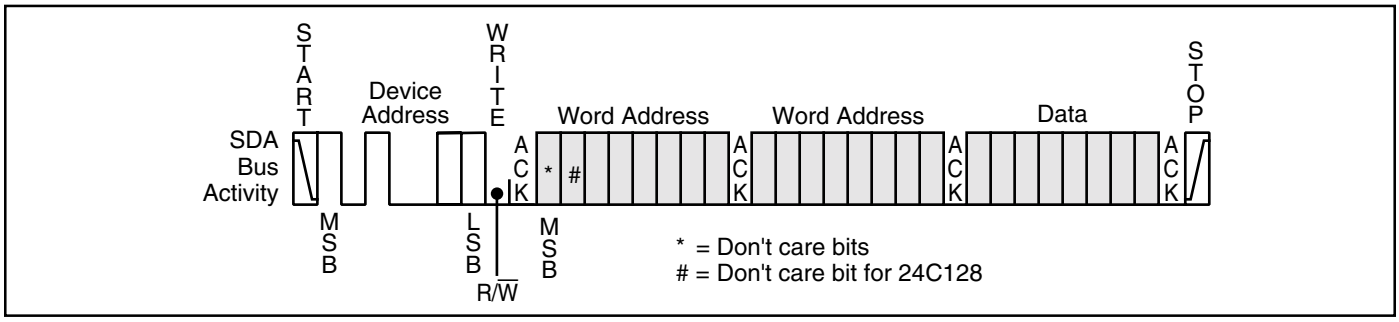


Figure 7. Page Write

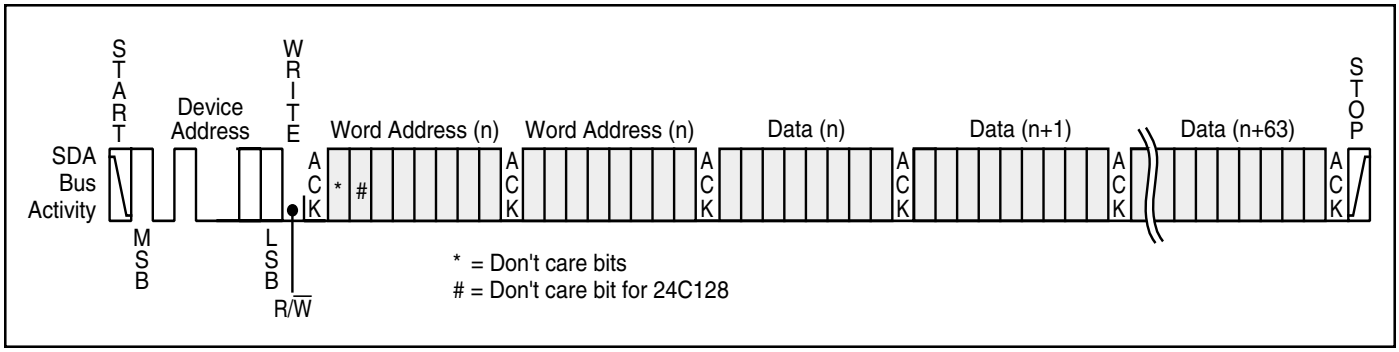


Figure 8. Current Address Read

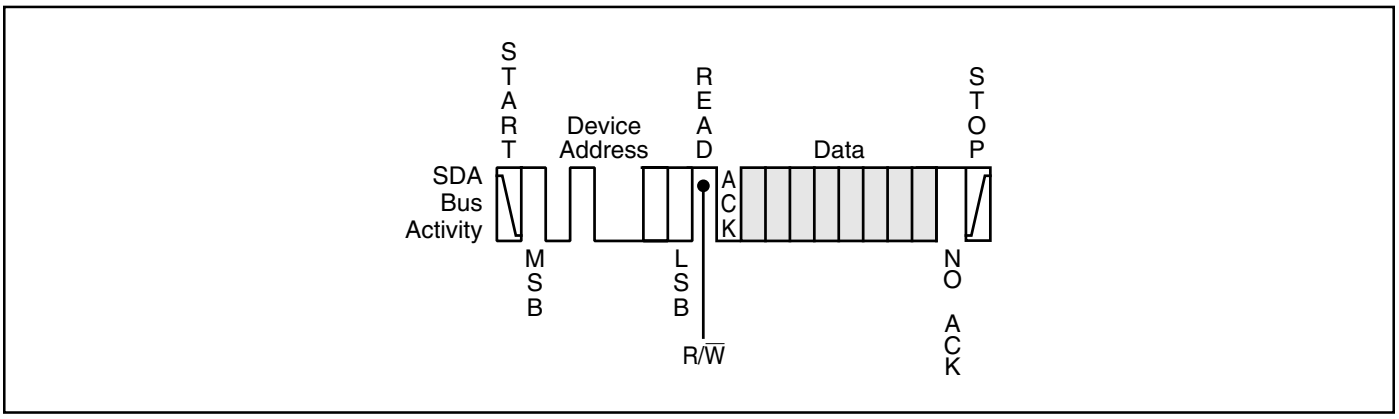


Figure 9. Random Access Read

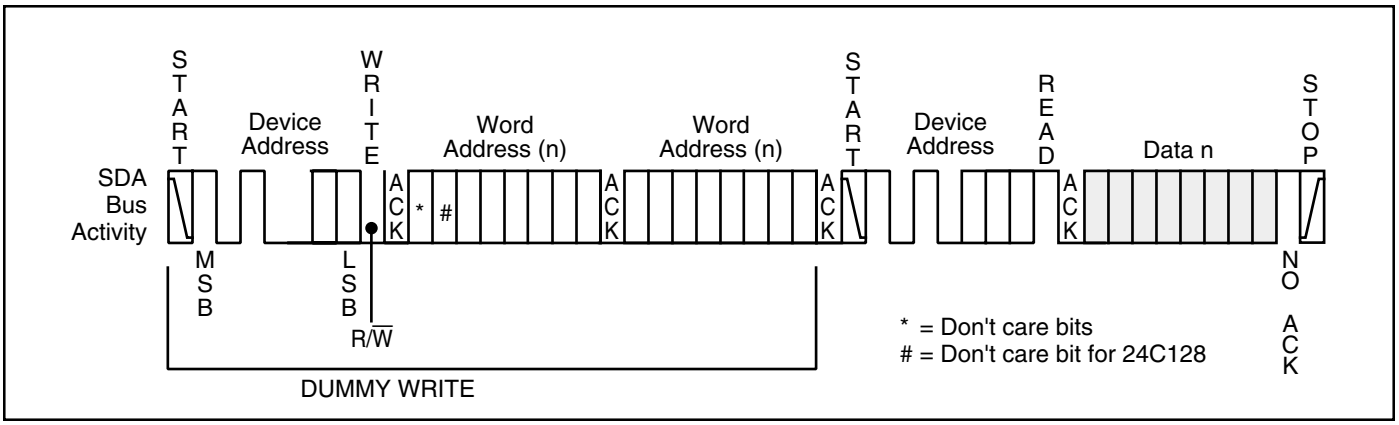
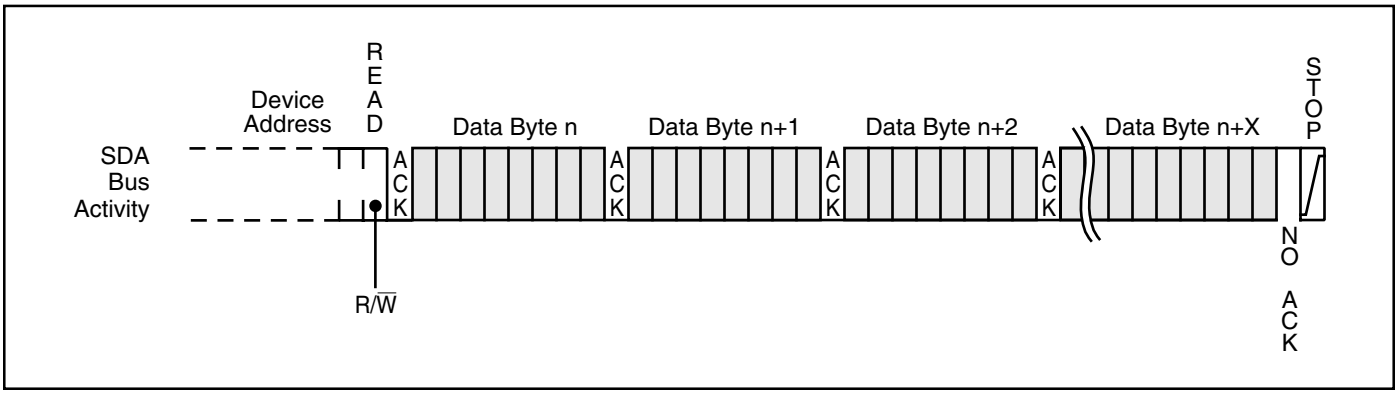


Figure 10. Sequential Read



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	0.5 to +6.25	V
V_P	Voltage on Any Pin	–0.5 to Vcc + 0.5	V
T_{BIAS}	Temperature Under Bias	–40 to +85	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Output Current	5	mA

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING RANGE (IS24C256-2 and IS24C128-2)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	1.8V to 5.5V
Industrial	–40°C to +85°C	1.8V to 5.5V

OPERATING RANGE (IS24C256-3 and IS24C128-3)

Range	Ambient Temperature	Vcc
Commercial	0°C to +70°C	2.5V to 5.5V
Industrial	–40°C to +85°C	2.5V to 5.5V

CAPACITANCE(1,2)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 5.0V.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OL1}	Output LOW Voltage	V_{CC} = 1.8V, I_{OL} = 0.15 mA	—	0.2	V
V_{OL2}	Output LOW Voltage	V_{CC} = 2.5V, I_{OL} = 1.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} x 0.7	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–1.0	V_{CC} x 0.3	V
I_{LI}	Input Leakage Current	V_{IN} = V_{CC} max.	—	3	µA
I_{LO}	Output Leakage Current		—	3	µA

Notes: V_{IL} min and V_{IH} max are reference only and are not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{CC1}	Vcc Operating Current	READ at 100 KHz (Vcc = 5V)	—	1.0	mA
I_{CC2}	Vcc Operating Current	WRITE at 100 KHz (Vcc = 5V)	—	3.0	mA
I_{SB1}	Standby Current	Vcc = 1.8V, Vcc = 2.5V	—	1	µA
I_{SB2}	Standby Current	Vcc = 5.5V	—	6	µA

AC ELECTRICAL CHARACTERISTICS

		1.8V		2.5V		5.0V		
Symbol	Parameter(Test Conditions)	Min.	Max.	Min.	Max.	Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	100	0	400	0	1000	KHz
T	Noise Suppression Time(1)	—	100	—	50	—	50	ns
t_{LOW}	Clock LOW Period	4.7	—	1.2	—	0.6	—	µs
t_{HIGH}	Clock HIGH Period	4	—	0.6	—	0.4	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)	4.7	—	1.2	—	0.5	—	µs
$t_{SU:STA}$	Start Condition Setup Time	4.7	—	0.6	—	0.25	—	µs
$t_{SU:STO}$	Stop Condition Setup Time	4.7	—	0.6	—	0.25	—	µs
$t_{HD:STA}$	Start Condition Hold Time	4	—	0.6	—	0.25	—	µs
$t_{HD:STO}$	Stop Condition Hold Time	4	—	0.6	—	0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time	200	—	100	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time	0	—	0	—	0	—	ns
t_{DH}	Data Out Hold Time (SCL LOW to SDA Data Out Change)	100	—	50	—	50	—	ns
t_{AA}	Clock to Output (SCL LOW to SDA Data Out Valid)	0.1	4.5	0.1	0.9	0.1	0.55	µs
t_R	SCL and SDA Rise Time(1)	—	1000	—	300	—	300	ns
t_F	SCL and SDA Fall Time(1)	—	300	—	300	—	100	ns
t_{WR}	Write Cycle Time	—	10	—	5	—	5	ms

Note:
1. This parameter is characterized but not 100% tested.

AC WAVEFORMS

Figure 11. Bus Timing

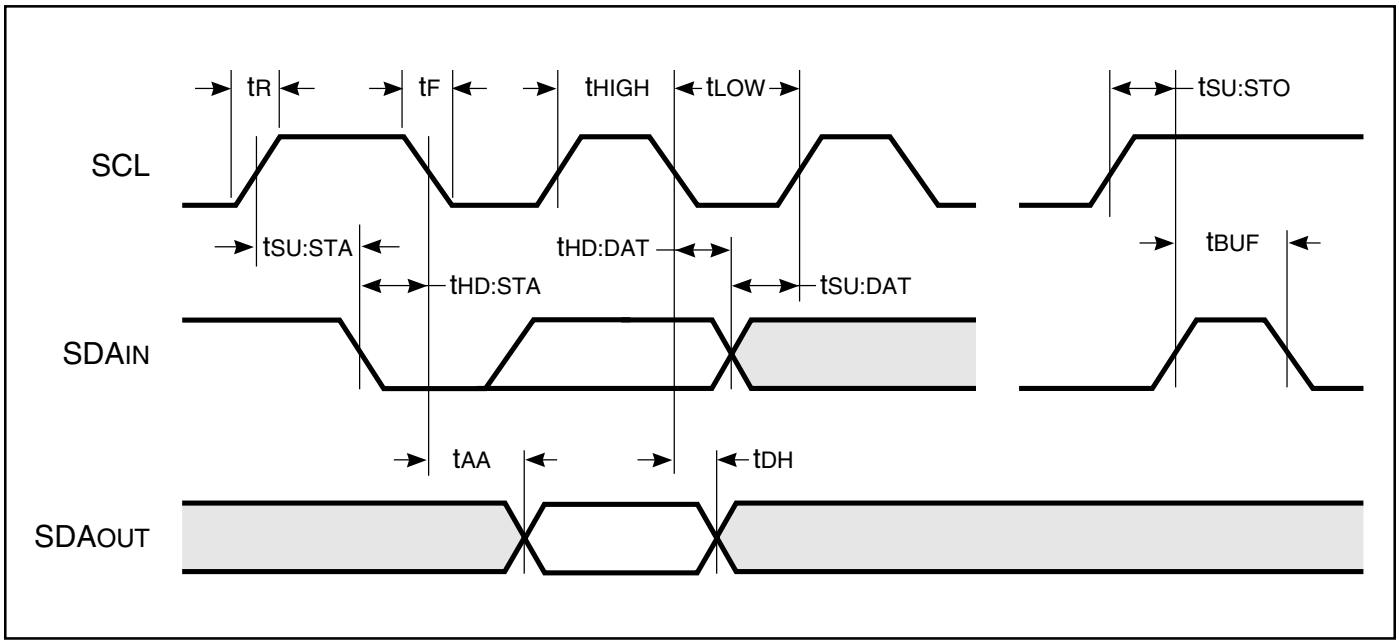
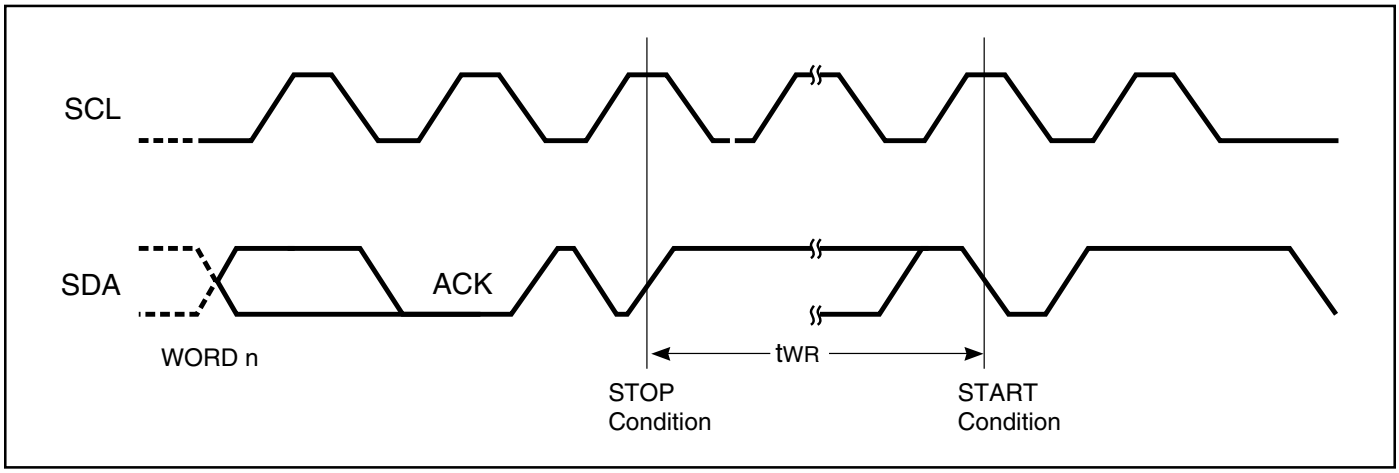


Figure 12. Write Cycle Timing



ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Voltage Range	Part Number	Package
100 KHz	1.8V to 5.5V	IS24C128-2P	300-mil Plastic DIP
		IS24C128-2G	Small Outline (JEDEC STD)
		IS24C128-2B	BGA
100 KHz	1.8V to 5.5V	IS24C256-2P	300-mil Plastic DIP
		IS24C256-2G	Small Outline (JEDEC STD)
		IS24C256-2B	BGA
400 KHz	2.5V to 5.5V	IS24C128-3P	300-mil Plastic DIP
		IS24C128-3G	Small Outline (JEDEC STD)
		IS24C128-3B	BGA
400 KHz	2.5V to 5.5V	IS24C256-3P	300-mil Plastic DIP
		IS24C256-3G	Small Outline (JEDEC STD)
		IS24C256-3B	BGA

ORDERING INFORMATION

Industrial Range: –40°C to +85°C

Frequency	Voltage Range	Part Number	Package
100 KHz	1.8V to 5.5V	IS24C128-2PI	300-mil Plastic DIP
		IS24C128-2GI	Small Outline (JEDEC STD)
		IS24C128-2BI	BGA
100 KHz	1.8V to 5.5V	IS24C256-2PI	300-mil Plastic DIP
		IS24C256-2GI	Small Outline (JEDEC STD)
		IS24C256-2BI	BGA
400 KHz	2.5V to 5.5V	IS24C128-3PI	300-mil Plastic DIP
		IS24C128-3GI	Small Outline (JEDEC STD)
		IS24C128-3BI	BGA
400 KHz	2.5V to 5.5V	IS24C256-3PI	300-mil Plastic DIP
		IS24C256-3GI	Small Outline (JEDEC STD)
		IS24C256-3BI	BGA

Integrated Silicon Solution, Inc.
2231 Lawson Lane
Santa Clara, CA 95054
Tel: 1-800-379-4774
Fax: (408) 588-0806
E-mail: sales@issi.com
www.issi.com