



**CY7C194  
CY7C195  
CY7C196**

**64K x 4 Static RAM**

**Features**

- High speed  
— 12 ns
- Output enable ( $\overline{OE}$ ) feature (7C195 and 7C196)
- CMOS for optimum speed/power
- Low active power  
— 880 mW
- Low standby power  
— 220 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

**Functional Description**

The CY7C194, CY7C195, and CY7C196 are high-performance CMOS static RAMs organized as 65,536 by 4 bits. Easy memory expansion is provided by active LOW chip enable(s) ( $\overline{CE}$  on the CY7C194 and CY7C195,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

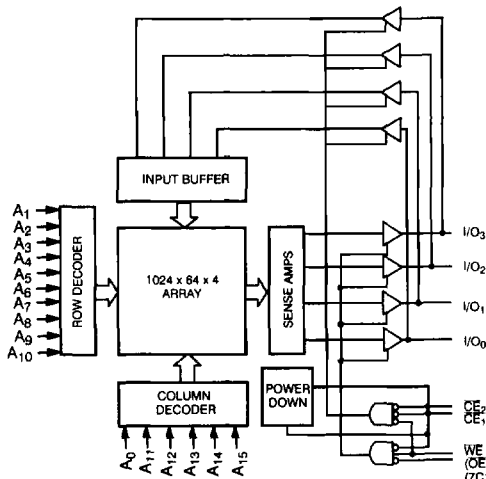
Writing to the device is accomplished when the chip enable(s) ( $\overline{CE}$  on the CY7C194 and CY7C195,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) and

write enable ( $\overline{WE}$ ) inputs are both LOW. Data on the four input pins ( $I/O_0$  through  $I/O_3$ ) is written into the memory location, specified on the address pins ( $A_0$  through  $A_{15}$ ).

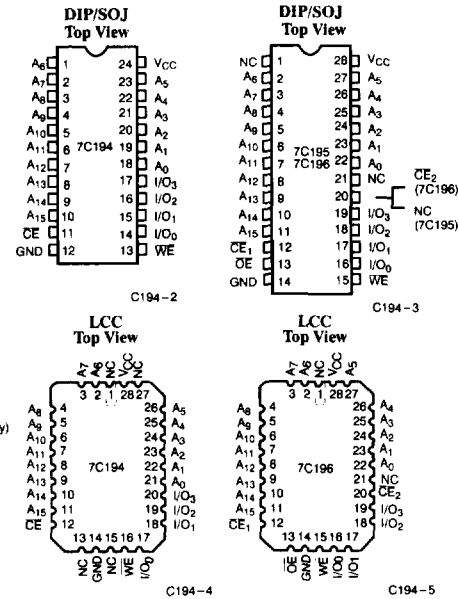
Reading the device is accomplished by taking the chip enable(s) ( $\overline{CE}$  on the CY7C194 and CY7C195,  $\overline{CE}_1$ ,  $\overline{CE}_2$  on the CY7C196) LOW, while write enable ( $\overline{WE}$ ) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

A die coat is used to ensure alpha immunity.

**Logic Block Diagram**



**Pin Configurations**



**Selection Guide**

	7C194-12 7C195-12 7C196-12	7C194-15 7C195-15 7C196-15	7C194-20 7C195-20 7C196-20	7C194-25 7C195-25 7C196-25	7C194-35 7C195-35 7C196-35	7C194-45 7C196-45
Maximum Access Time (ns)	12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	155	145	135	115	
	Military		160	150	125	125
Maximum Standby Current (mA)	30	30	30	30	30	30

Shaded area contains preliminary information.



**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied ..... -55°C to +125°C  
 Supply Voltage to Ground Potential ..... -0.5V to +7.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 DC Input Voltage<sup>[1]</sup> ..... -0.5V to V<sub>CC</sub> + 0.5V  
 Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

**Operating Range**

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0°C to +70°C	5V ± 10%
Military <sup>[2]</sup>	-55°C to +125°C	5V ± 10%

**Electrical Characteristics Over the Operating Range<sup>[3]</sup>**

Parameter	Description	Test Conditions	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		Unit
			Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V
V <sub>IL</sub> <sup>[1]</sup>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V
I <sub>IX</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/τ <sub>RC</sub>	Com'l	155		145	mA
			Mil			160	
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current —TTL Inputs <sup>[5]</sup>	Max. V <sub>CC</sub> , $\overline{CE}_{1,2} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30	mA
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current —CMOS Inputs <sup>[5]</sup>	Max. V <sub>CC</sub> , $\overline{CE}_{1,2} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0	Com'l	10		10	mA
			Mil			15	

Shaded area contains preliminary information.

**Notes:**

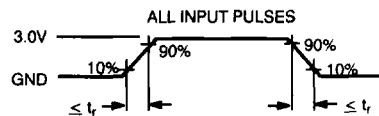
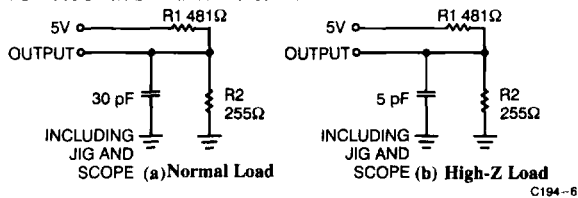
- Minimum voltage is equal to -2.0V for pulse durations of less than 20 ns.
- T<sub>A</sub> is the "instant on" case temperature.
- See the last page of this specification for Group A subgroup testing information.
- Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
- A pull-up resistor to V<sub>CC</sub> on the  $\overline{CE}$  input is required to keep the device deselected during V<sub>CC</sub> power-up, otherwise I<sub>SB</sub> will exceed values given.

**Electrical Characteristics Over the Operating Range<sup>[3]</sup> (continued)**

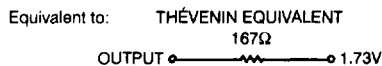
Parameter	Description	Test Conditions	7C194-20 7C195-20 7C196-20		7C194-25, 35, 45 7C195-25, 35 7C196-25, 35, 45		Unit	
			Min.	Max.	Min.	Max.		
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min., I <sub>OH</sub> = -4.0 mA	2.4		2.4		V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min., I <sub>OL</sub> = 8.0 mA		0.4		0.4	V	
V <sub>IH</sub>	Input HIGH Voltage		2.2	V <sub>CC</sub> + 0.3V	2.2	V <sub>CC</sub> + 0.3V	V	
V <sub>IL</sub>	Input LOW Voltage		-0.5	0.8	-0.5	0.8	V	
I <sub>Ix</sub>	Input Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-5	+5	-5	+5	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-5	+5	-5	+5	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[4]</sup>	V <sub>CC</sub> = Max., V <sub>OUT</sub> = GND		-300		-300	mA	
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max., I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/trc	Com'l		135		115	mA
			Mil		150		125	
I <sub>SB1</sub>	Automatic $\overline{CE}$ Power-Down Current -TTL Inputs <sup>[5]</sup>	Max. V <sub>CC</sub> , $\overline{CE}_{1,2} \geq V_{IH}$ , V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> , f = f <sub>MAX</sub>		30		30	mA	
I <sub>SB2</sub>	Automatic $\overline{CE}$ Power-Down Current -CMOS Inputs <sup>[5]</sup>	Max. V <sub>CC</sub> , $\overline{CE}_{1,2} \geq V_{CC} - 0.3V$ , V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.3V or V <sub>IN</sub> ≤ 0.3V, f = 0		15		15	mA	

**Capacitance<sup>[6]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = 5.0V	8	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**AC Test Loads and Waveforms<sup>[7]</sup>**


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**Notes:**

- Tested initially and after any design or process changes that may affect these parameters.
- t<sub>r</sub> = ≤ 3 ns for the -12 and -15 speeds. t<sub>r</sub> = ≤ 5 ns for the -20 and slower speeds.



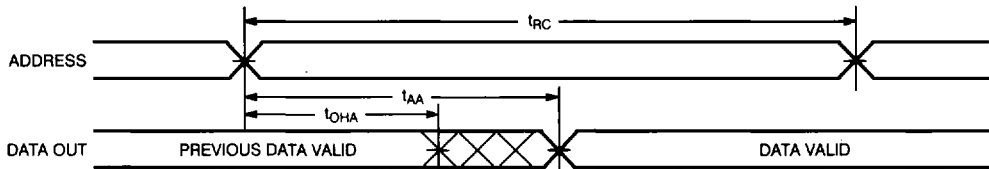
Switching Characteristics Over the Operating Range<sup>[3, 8]</sup>

Parameter	Description	7C194-12 7C195-12 7C196-12		7C194-15 7C195-15 7C196-15		7C194-20 7C195-20 7C196-20		7C194-25 7C195-25 7C196-25		7C194-35 7C195-35 7C196-35		7C194-45 7C196-45		Unit		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.			
<b>READ CYCLE</b>																
t <sub>RC</sub>	Read Cycle Time	12		15		20		25		35		45		ns		
t <sub>AA</sub>	Address to Data Valid		12		15		20		25		35		45	ns		
t <sub>OHA</sub>	Output Hold from Address Change	3		3		3		3		3		3		ns		
t <sub>ACE1</sub> , t <sub>ACE2</sub>	CE LOW to Data Valid		12		15		20		25		35		45	ns		
t <sub>DOE</sub>	OE LOW to Data Valid		5		7		9		10		16		16	ns		
t <sub>LZOE</sub>	OE LOW to Low Z		0		0		0		3		3		3	ns		
t <sub>HZOE</sub>	OE HIGH to High Z <sup>[10]</sup>		5		7		9		11		15		15	ns		
t <sub>LZCE1</sub> , t <sub>LZCE2</sub>	CE LOW to Low Z <sup>[9]</sup>	3		3		3		3		3		3		ns		
t <sub>HZCE1</sub> , t <sub>HZCE2</sub>	CE HIGH to High Z <sup>[9,10]</sup>		5		7		9		11		15		15	ns		
t <sub>PU</sub>	CE LOW to Power-Up	0		0		0		0		0		0		ns		
t <sub>PD</sub>	CE HIGH to Power-Down		12		15		20		25		35		45	ns		
<b>WRITE CYCLE<sup>[11]</sup></b>																
t <sub>WC</sub>	Write Cycle Time	12		15		20		25		35		45		ns		
t <sub>SCE</sub>	CE LOW to Write End	9		10		15		18		22		22		ns		
t <sub>AW</sub>	Address Set-Up to Write End	9		10		15		20		25		35		ns		
t <sub>HA</sub>	Address Hold from Write End	0		0		0		0		0		0		ns		
t <sub>SA</sub>	Address Set-Up to Write Start	0		0		0		0		0		0		ns		
t <sub>PWE</sub>	WE Pulse Width	8		9		15		18		22		22		ns		
t <sub>SD</sub>	Data Set-Up to Write End	8		9		10		10		15		15		ns		
t <sub>HD</sub>	Data Hold from Write End	0		0		0		0		0		0		ns		
t <sub>LZWE</sub>	WE HIGH to Low Z <sup>[9]</sup>	3		3		3		3		3		3		ns		
t <sub>HZWE</sub>	WE LOW to High Z <sup>[9, 8]</sup>		7		7		10		0	13		0	15	0	20	ns

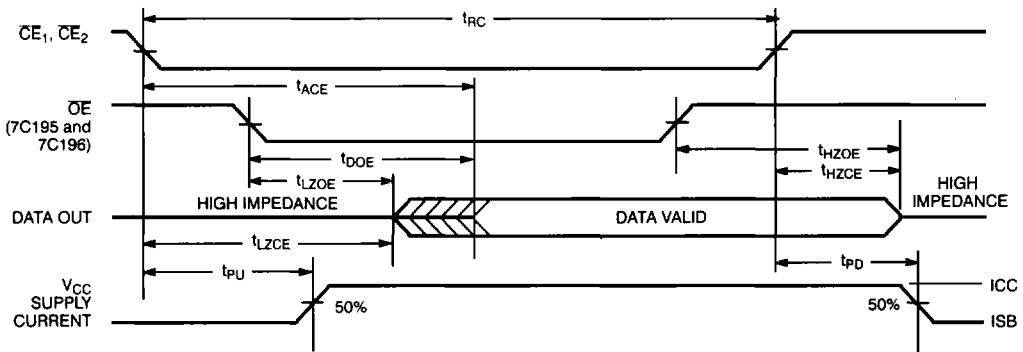
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Notes:

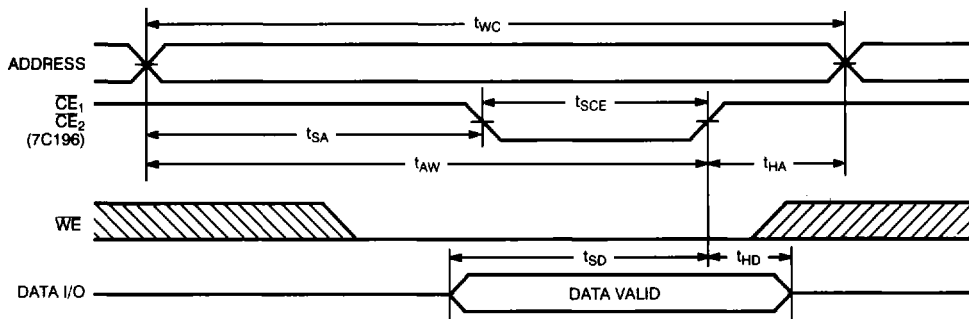
- Test conditions assume signal transition time of 3 ns or less for -12 and -15 speeds and 5 ns or less for -20 and slower speeds, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and 30-pF load capacitance.
- At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub> and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any given device.
- t<sub>HZOE</sub>, t<sub>HZCE</sub>, and t<sub>HZWE</sub> are specified with C<sub>L</sub> = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- The internal write time of the memory is defined by the overlap of CE<sub>1</sub> LOW, CE<sub>2</sub> LOW, and WE LOW. All signals must be LOW to initiate a write and any signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

**Switching Waveforms**
**Read Cycle No. 1<sup>[12, 13]</sup>**


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**Read Cycle No. 2<sup>[12, 14]</sup>**


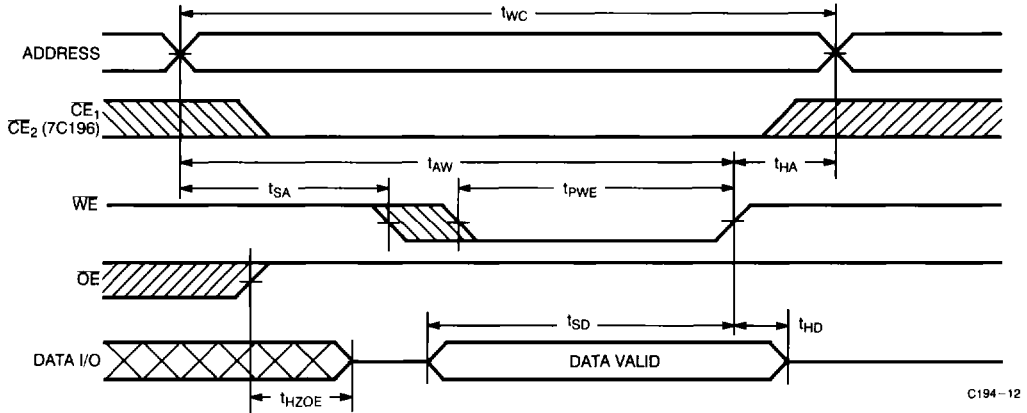
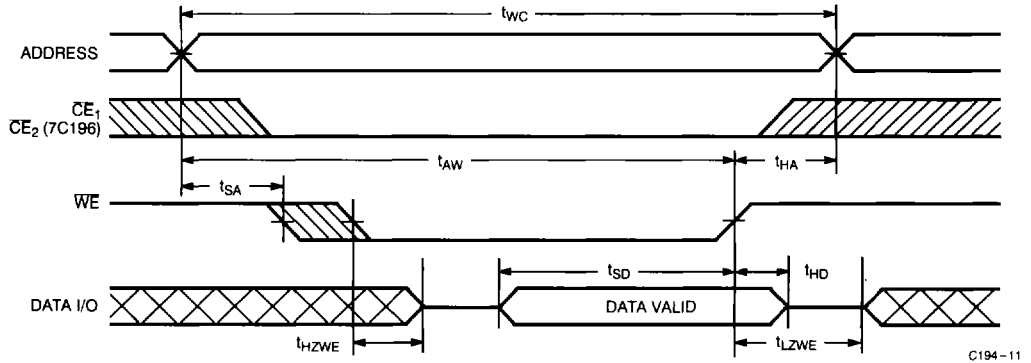
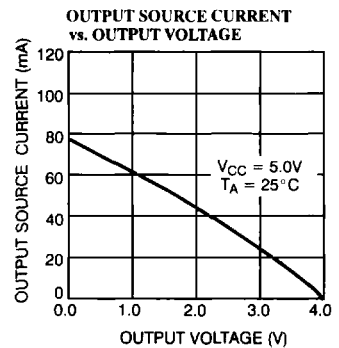
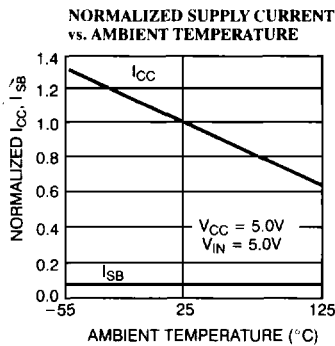
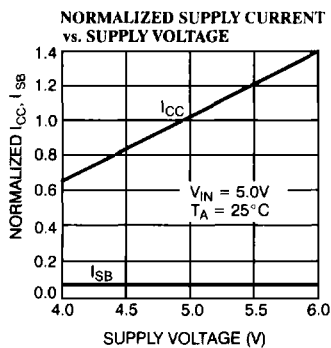
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**Write Cycle No. 1 (CE Controlled)<sup>[11, 15, 16]</sup>**


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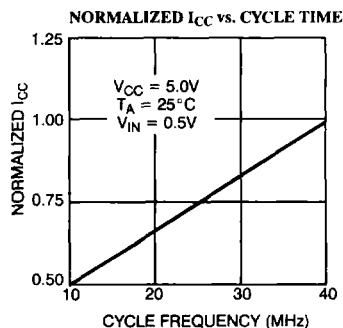
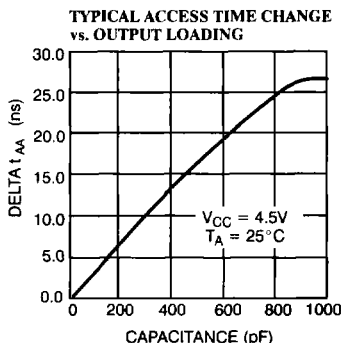
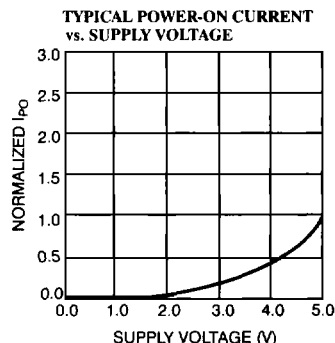
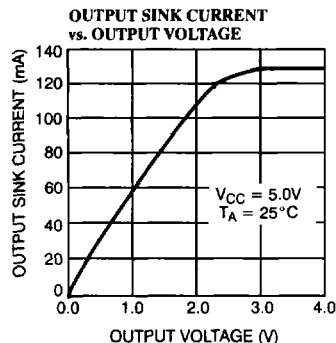
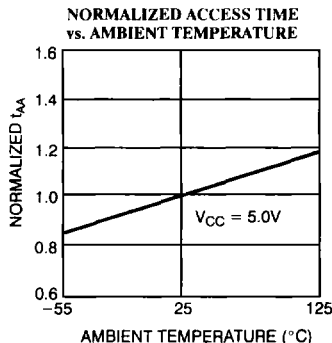
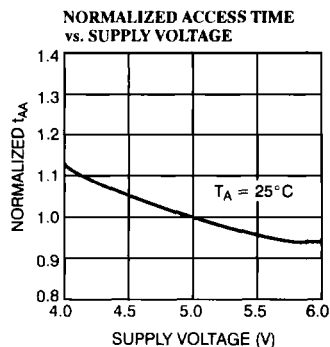
**Notes:**

12. **WE** is HIGH for read cycle.
13. Device is continuously selected:  $\overline{CE}_1 = V_{IL}$ ,  $\overline{CE}_2 = V_{IL}$  (7C196), and  $\overline{OE} = V_{IL}$  (7C195 and 7C196).
14. Address valid prior to or coincident with  $\overline{CE}_1$  and  $\overline{CE}_2$  transition LOW.
15. Data I/O will be high impedance if  $\overline{OE} = V_{IH}$  (7C195 and 7C196).
16. If any CE goes HIGH simultaneously with **WE** HIGH, the output remains in a high-impedance state.
17. The minimum write cycle time for Write Cycle No. 3 (**WE** controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

**Switching Waveforms (continued)**
**Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write for 7C195 and 7C196 only)<sup>[11, 15, 16]</sup>**

**Write Cycle No. 3 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16, 17]</sup>**

**Typical DC and AC Characteristics**




Typical DC and AC Characteristics (continued)



7C194 Truth Table

CE	WE	Data I/O	Mode	Power
H	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	Data Out	Read	Active ( $I_{CC}$ )
L	L	Data In	Write	Active ( $I_{CC}$ )

7C195 Truth Table

CE <sub>1</sub>	WE	OE	Data I/O	Mode	Power
H	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect	Active ( $I_{CC}$ )

7C196 Truth Table

CE <sub>1</sub>	CE <sub>2</sub>	WE	OE	Data I/O	Mode	Power
H	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	H	X	X			
L	L	H	L	Data Out	Read	Active ( $I_{CC}$ )
L	L	L	X	Data In	Write	Active ( $I_{CC}$ )
L	L	H	H	High Z	Deselect	Active ( $I_{CC}$ )



**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C194-12PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-12VC	V13	24-Lead Molded SOJ	
15	CY7C194-15PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-15VC	V13	24-Lead Molded SOJ	
	CY7C194-15DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
20	CY7C194-20PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-20VC	V13	24-Lead Molded SOJ	
	CY7C194-20DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
25	CY7C194-25PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-25VC	V13	24-Lead Molded SOJ	
	CY7C194-25DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
35	CY7C194-35PC	P13	24-Lead (300-Mil) Molded DIP	Commercial
	CY7C194-35VC	V13	24-Lead Molded SOJ	
	CY7C194-35DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	
45	CY7C194-45DMB	D14	24-Lead (300-Mil) CerDIP	Military
	CY7C194-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C195-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-12VC	V21	28-Lead Molded SOJ	
15	CY7C195-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-15VC	V21	28-Lead Molded SOJ	
20	CY7C195-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-20VC	V21	28-Lead Molded SOJ	
25	CY7C195-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-25VC	V21	28-Lead Molded SOJ	
35	CY7C195-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C195-35VC	V21	28-Lead Molded SOJ	

Shaded areas contain preliminary information.





**Ordering Information** (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C196-12PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-12VC	V21	28-Lead Molded SOJ	
15	CY7C196-15PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-15VC	V21	28-Lead Molded SOJ	
	CY7C196-15LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
20	CY7C196-20PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-20VC	V21	28-Lead Molded SOJ	
	CY7C196-20LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
25	CY7C196-25PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-25VC	V21	28-Lead Molded SOJ	
	CY7C196-25LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
35	CY7C196-35PC	P21	28-Lead (300-Mil) Molded DIP	Commercial
	CY7C196-35VC	V21	28-Lead Molded SOJ	
	CY7C196-35LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military
45	CY7C196-45LMB	L54	28-Pin Rectangular Leadless Chip Carrier	Military

Shaded area contains preliminary information.

**MILITARY SPECIFICATIONS**

**Group A Subgroup Testing**

**DC Characteristics**

Parameter	Subgroups
V <sub>OH</sub>	1, 2, 3
V <sub>OL</sub>	1, 2, 3
V <sub>IH</sub>	1, 2, 3
V <sub>IL Max.</sub>	1, 2, 3
I <sub>Ix</sub>	1, 2, 3
I <sub>OZ</sub>	1, 2, 3
I <sub>OS</sub>	1, 2, 3
I <sub>CC</sub>	1, 2, 3
I <sub>SB1</sub>	1, 2, 3
I <sub>SB2</sub>	1, 2, 3

**Switching Characteristics**

Parameter	Subgroups
<b>READ CYCLE</b>	
t <sub>RC</sub>	7, 8, 9, 10, 11
t <sub>AA</sub>	7, 8, 9, 10, 11
t <sub>OHA</sub>	7, 8, 9, 10, 11
t <sub>ACE, ACE2</sub>	7, 8, 9, 10, 11
t <sub>DOE</sub> <sup>[18]</sup>	7, 8, 9, 10, 11
<b>WRITE CYCLE</b>	
t <sub>WC</sub>	7, 8, 9, 10, 11
t <sub>SCE</sub>	7, 8, 9, 10, 11
t <sub>AW</sub>	7, 8, 9, 10, 11
t <sub>HA</sub>	7, 8, 9, 10, 11
t <sub>SA</sub>	7, 8, 9, 10, 11
t <sub>PWE</sub>	7, 8, 9, 10, 11
t <sub>SD</sub>	7, 8, 9, 10, 11
t <sub>HD</sub>	7, 8, 9, 10, 11

Note:

18. 7C195 and 7C196 only.

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