1M x 36 DRAM Module

Features

- 72-Pin JEDEC Standard Single-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	$\overline{RAS}$ Access Time	60ns	70ns
t_{CAC}	$\overline{CAS}$ Access Time	20ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

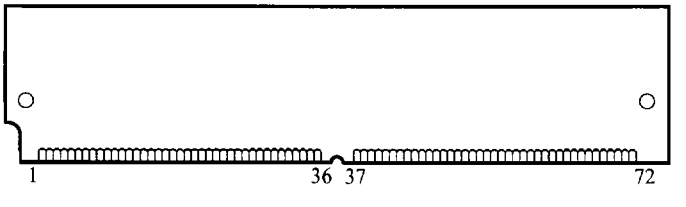
- High Performance CMOS process
- Single 5V, ± 0.5V Power Supply
- Low active current dissipation
- All inputs & outputs are fully TTL & CMOS compatible
- Fast Page Mode access cycle
- Refresh Modes: $\overline{RAS}$-Only and CBR
- 1024 refresh cycles distributed across 16ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write parity applications
- Au and Sn/Pb versions available

Description

The IBM11D1360BD is a 4MB industry standard 72-pin 4-byte single in-line memory module (SIMM). The module is organized as a 1Mx36 high speed memory array that is intended for use in 18, 36, and 72 bit parity applications. It is manufactured with 8 1Mx4 devices, each in a 300mil package, and 4 1Mx1 devices in a 300mil package. The module is compatible with the JEDEC 72-pin SIMM standard.

The IBM 72-Pin SIMMs provide a high performance, flexible 4-byte interface in a 4.25" long footprint. Related products include the 1Mx32 non-parity SIMM, IBM11D1320B, as well as higher density and ECC-optimized SIMMs.

Card Outline



Pin Description

$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
PQ8, 17, 26, 35	Parity Input/output
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connect
PD1 - PD4	Presence Detects

Pinout

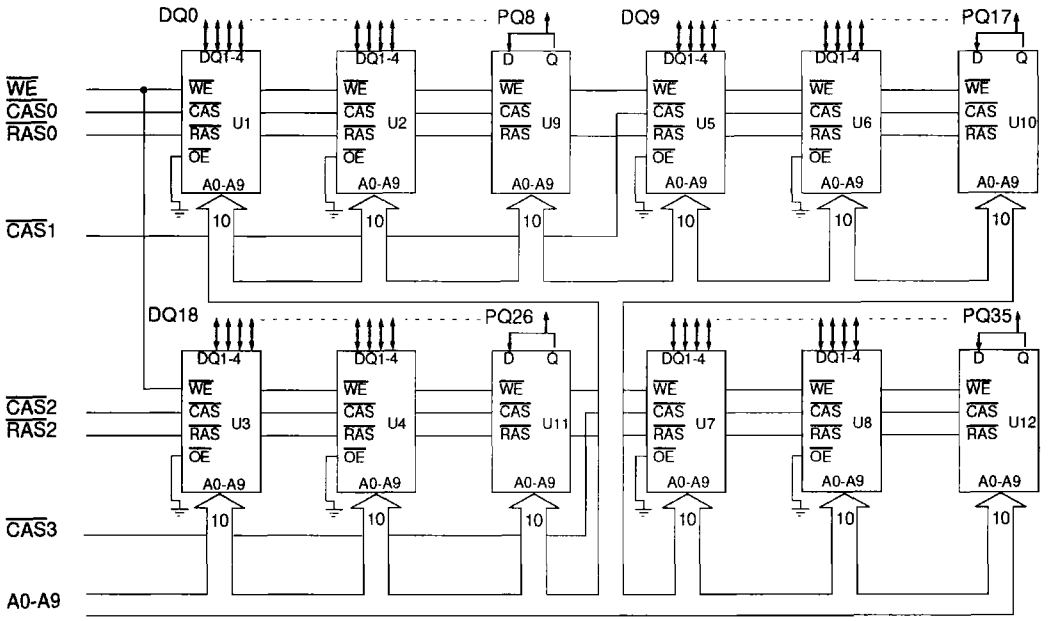
Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ24	37	PQ17	49	DQ9	61	DQ14
2	DQ0	14	A2	26	DQ7	38	PQ35	50	DQ27	62	DQ33
3	DQ18	15	A3	27	DQ25	39	V_{SS}	51	DQ10	63	DQ15
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ28	64	DQ34
5	DQ19	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ11	65	DQ16
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ29	66	NC
7	DQ20	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ12	67	PD1
8	DQ3	20	DQ4	32	A9	44	$\overline{RAS0}$	56	DQ30	68	PD2
9	DQ21	21	DQ22	33	NC	45	NC	57	DQ13	69	PD3
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ31	70	PD4
11	NC	23	DQ23	35	PQ26	47	$\overline{WE}$	59	V_{CC}	71	NC
12	A0	24	DQ6	36	PQ8	48	NC	60	DQ32	72	V_{SS}

1. DQ numbering is compatible with non-parity (x32) version.

Ordering Information

Part Number	Organization	Speed	Leads	Dimensions	Notes
IBM11D1360BD-60	1M x 36	60ns	Sn/Pb	4.25" x 1" x .360"	
IBM11D1360BD-70	1M x 36	70ns	Sn/Pb	4.25" x 1" x .360"	
IBM11E1360BD-60	1M x 36	60ns	Au	4.25" x 1" x .360"	
IBM11E1360BD-70	1M x 36	70ns	Au	4.25" x 1" x .360"	

Block Diagram



Truth Table

Function	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	All DQ, PQ bits
Standby	H	X	X	X	X	High Impedance
Read	L	L	H	Row	Col	Valid Data Out
Early-Write	L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle	L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles	L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle	L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles	L	H→L	L	N/A	Col	Valid Data In
$\overline{RAS}$-Only Refresh	L	H	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh	H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	V_{SS}	V_{SS}
PD2	V_{SS}	V_{SS}
PD3	NC	V_{SS}
PD4	NC	NC

1. NC= OPEN, V_{SS} = GND

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-1.0 to +6.0	V	1
V_{OUT}	Output Voltage	-1.0 to +6.0	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +125	°C	1
P_D	Power Dissipation	5.72	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.4	—	Vcc + 0.5	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 0 to +70°C, V_{CC} = 5.0 ± 0.5V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	78	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$)	50	pF	
C_{I3}	Input Capacitance ($\overline{CAS}$)	27	pF	
C_{I4}	Input Capacitance ($\overline{WE}$)	94	pF	
$C_{I/O1}$	Output Capacitance (DQ0-DQ34)	13	pF	
$C_{I/O2}$	Output Capacitance (PQ8, 17, 26, 35)	18	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

Symbol	Parameter		Min	Max	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-60	—	1040	mA	1, 2, 3
		-70	—	900		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥V_{IH})		—	24	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥V_{IH}: t_{RC} = t_{RC} min)	-60	—	1040	mA	1, 3
		-70	—	900		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-60	—	800	mA	1, 2, 3
		-70	—	680		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)		—	12	mA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-60	—	1040	mA	1, 3
		-70	—	900		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} < 6.0V)) All Other Pins Not Under Test = 0V	$\overline{RAS}$	-60	+60	µA	
		$\overline{CAS}$	-30	+30		
		All others	-120	+120		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})		-10	+10	µA	
V_{OH}	Output High Level Output "H" Level Voltage (I_{OUT} = -5mA @ 2.4V)		2.4	—	V	
V_{OL}	Output Low Level Output "L" Level Voltage (I_{OUT} = +4.2mA @ 0.4V)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ = V_{IH}.

AC Characteristics (T_A = 0 to +70°C, V_{CC} = 5 ± 0.5V)

1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
3. AC measurements assume t_T = 5ns.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	16K	70	16K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	—	20	—	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	40	20	50	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	—	15	—	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	20	—	20	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	

1. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	50	—	55	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	20	—	20	ns	1, 2
t_{AA}	Access Time from Address	—	30	—	35	ns	1, 2
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	—	—	—	—	ns	4
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	
t_{OH}	Output Data Hold Time	0	—	0	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	20	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	0	20	0	20	ns	5

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
3. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	40	ns	1, 2

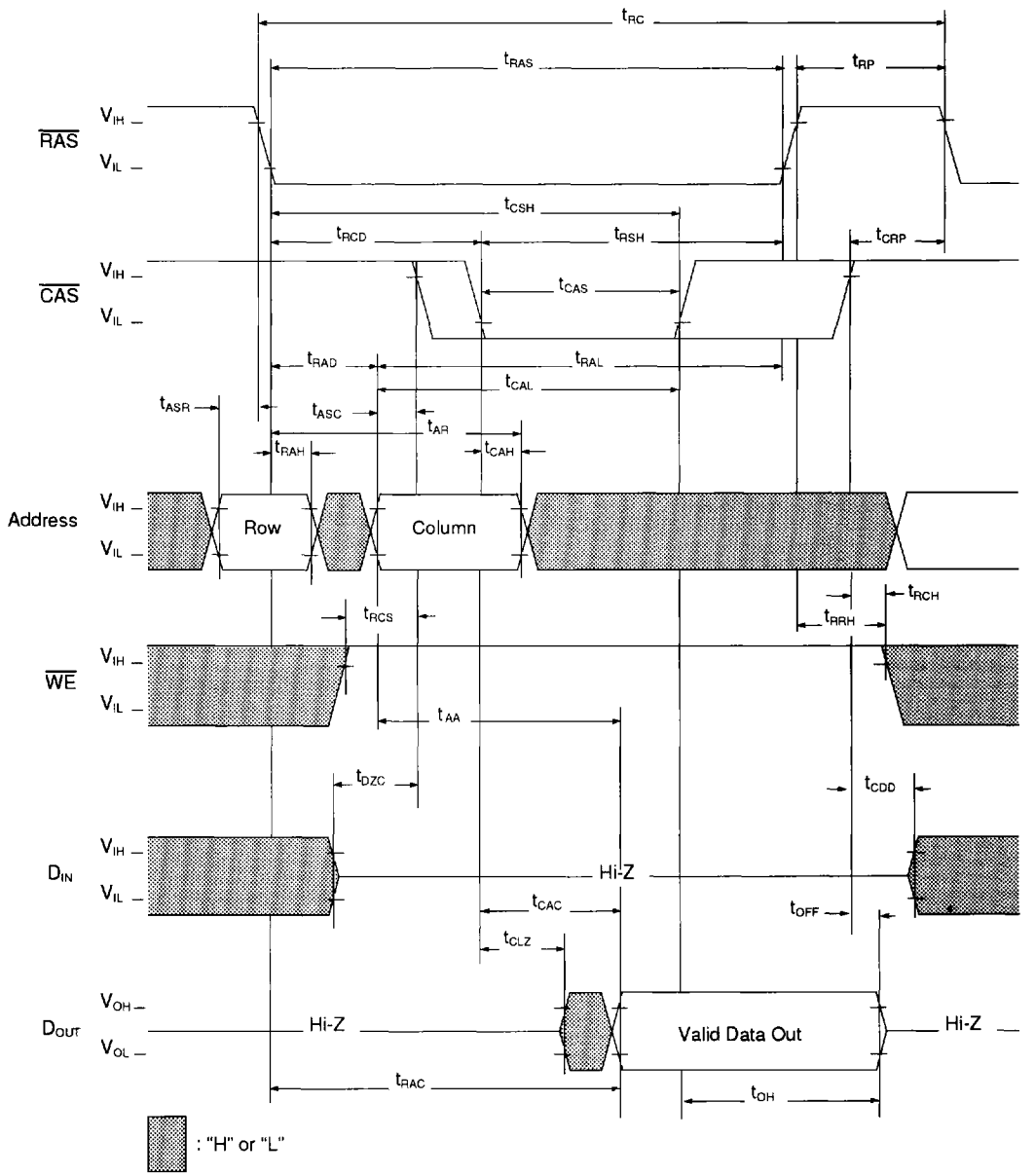
1. Access time is determined by the latter of t_{RAC}, t_{CAC}, t_{CPA}, t_{AA}.
2. Access time assumes a load of 100pF.

Refresh Cycle

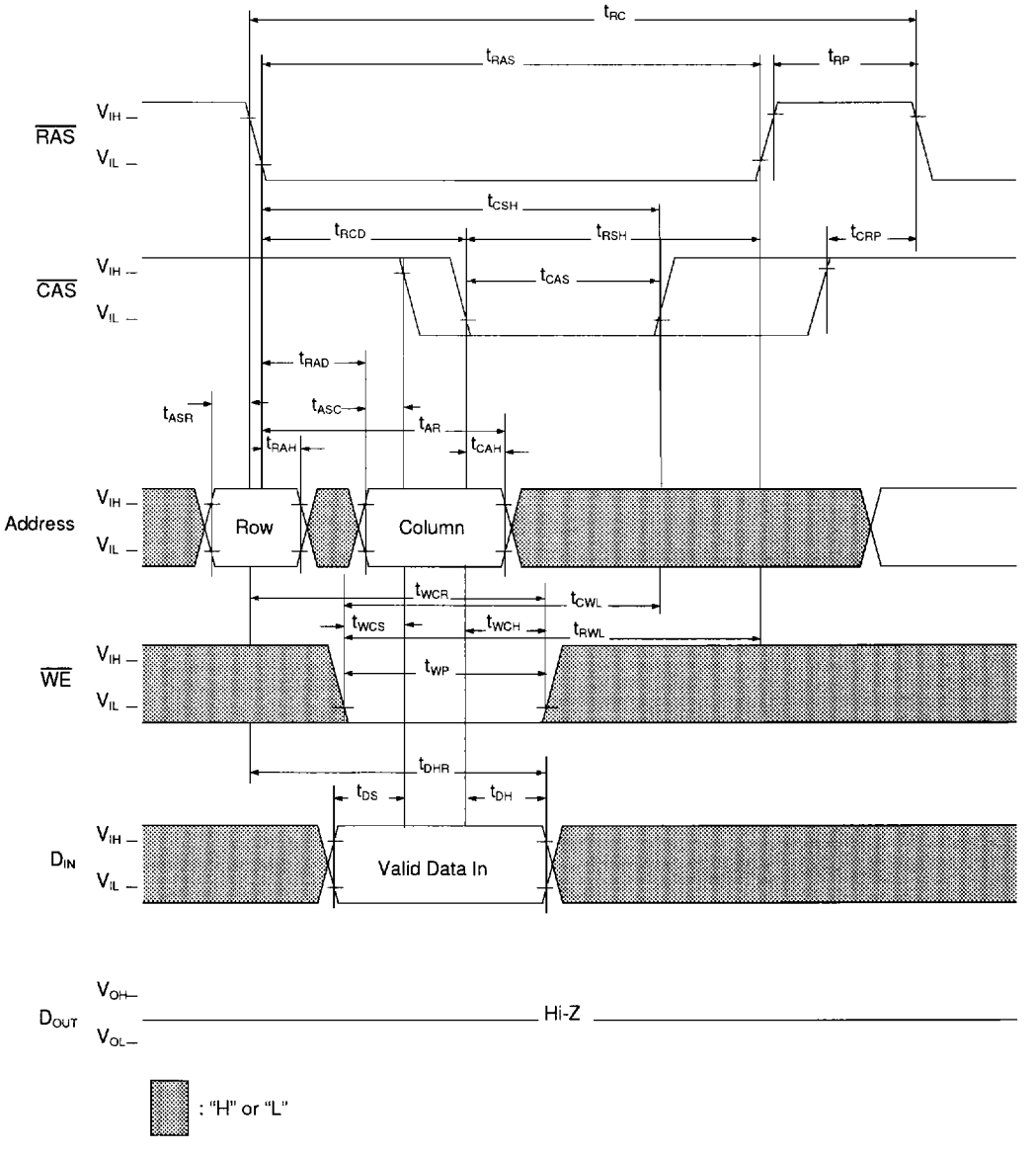
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	30	—	30	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	10	—	10	—	ns	
t_{REF}	Refresh Period	—	16	—	16	ms	1

1. 1024 refreshes are required every 16ms.

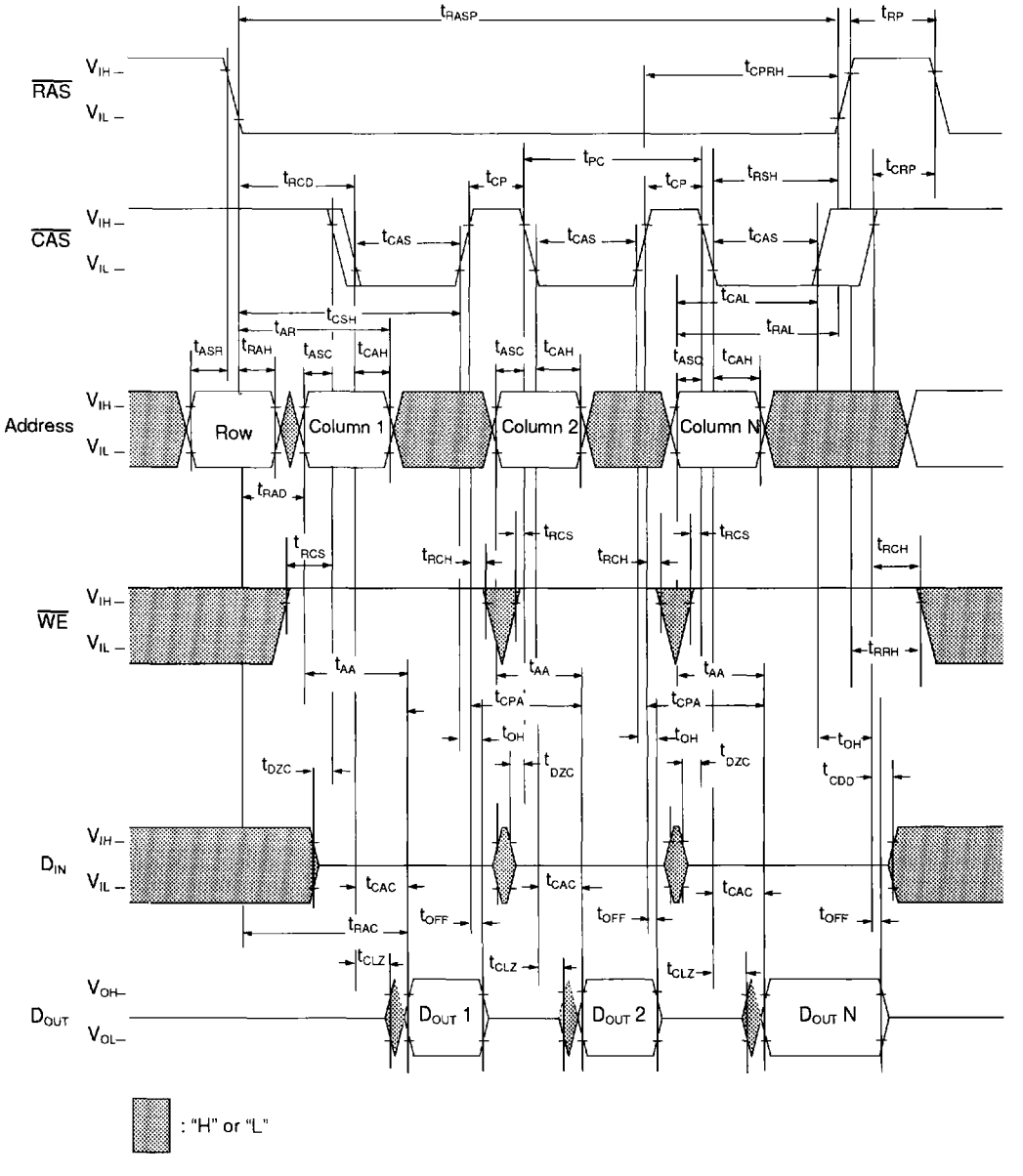
Read


tRC
tRAS
tRP
RAS
VIH
VIL
tCSH
tRCD
tRSH
tCRP
CAS
tCAS
tRAD
tRAL
tCAL
tASR
tASC
tAR
tRAH
tCAH
Address
Row
Column
tRCS
tRCH
tRRH
WE
tAA
tDZC
tCDD
DIN
Hi-Z
tCAC
tOFF
tCLZ
DOUT
VOH
VOL
Valid Data Out
tRAC
tOH
: "H" or "L"

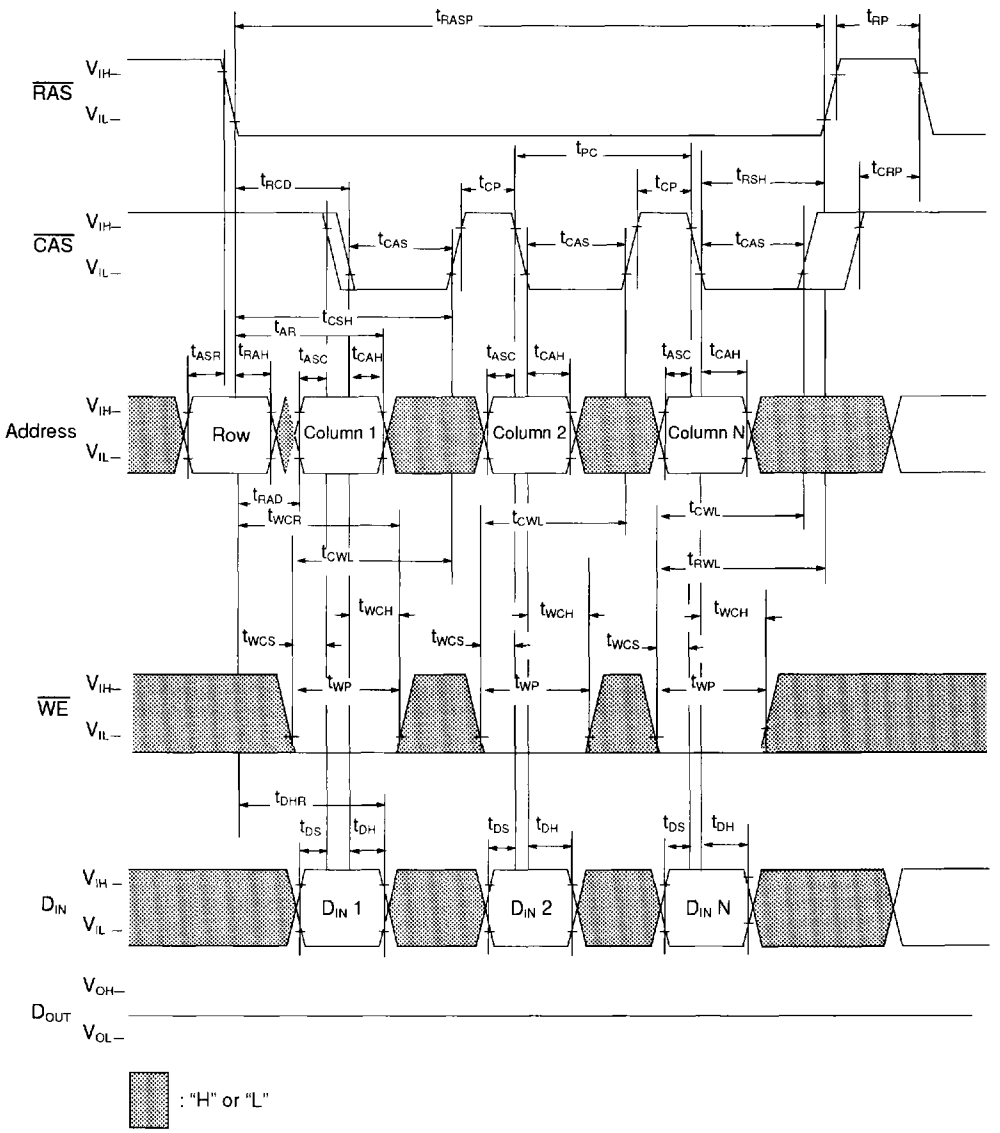
Write Cycle (Early Write)



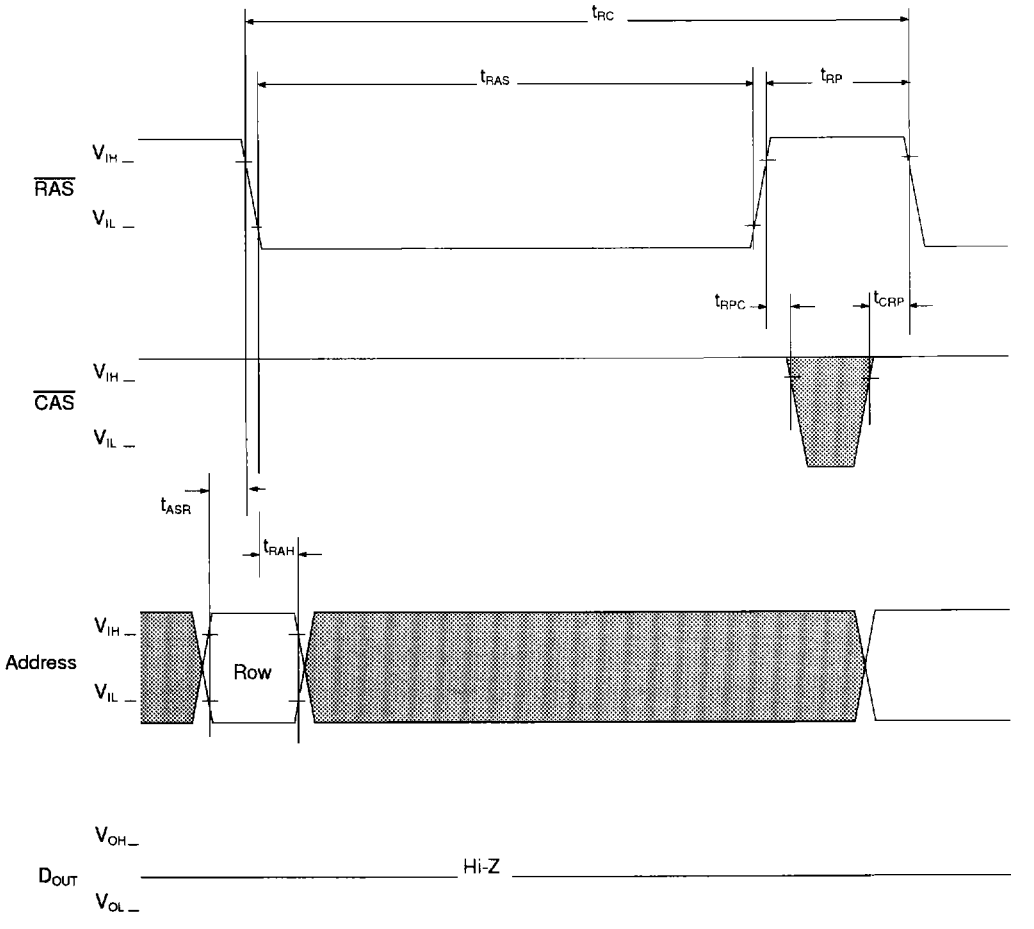
Fast Page Mode Read Cycle



Fast Page Mode Write Cycle

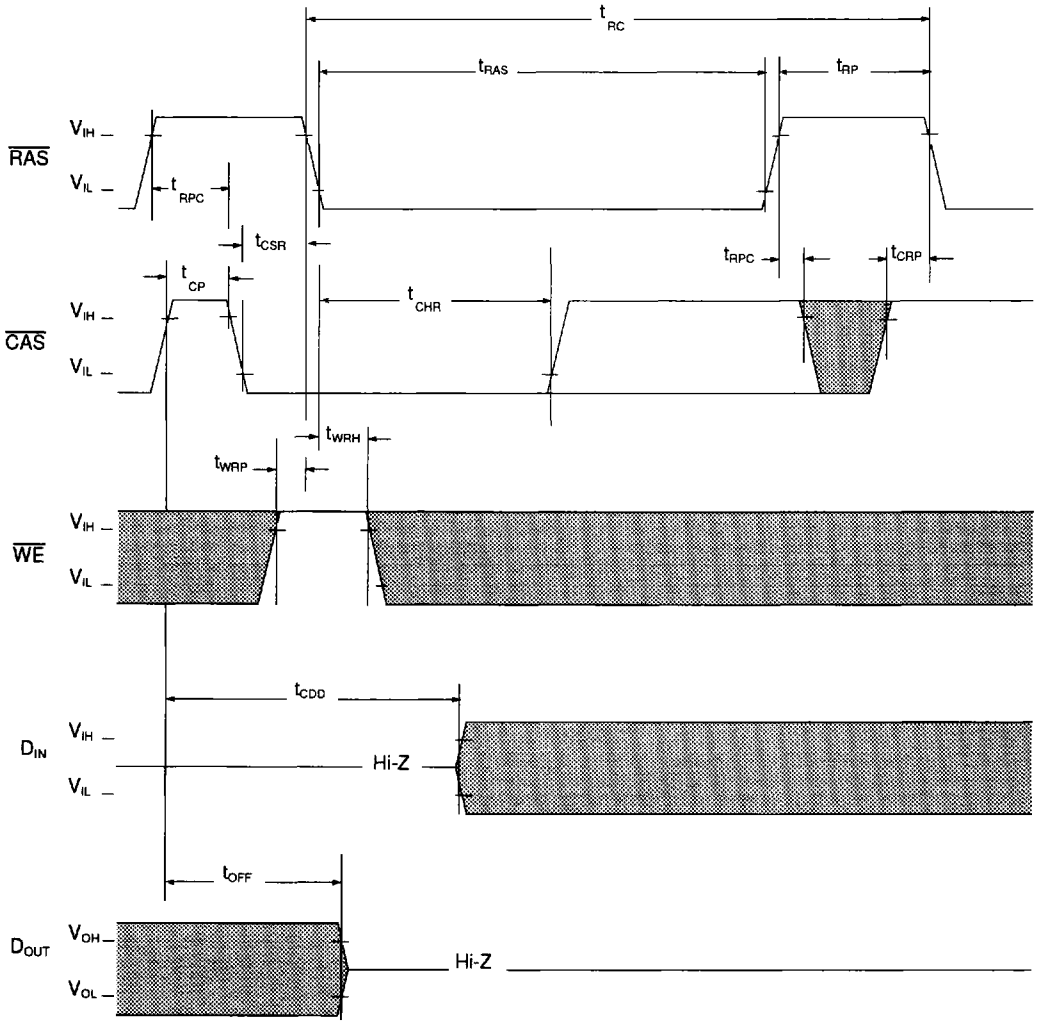


$\overline{RAS}$ Only Refresh Cycle



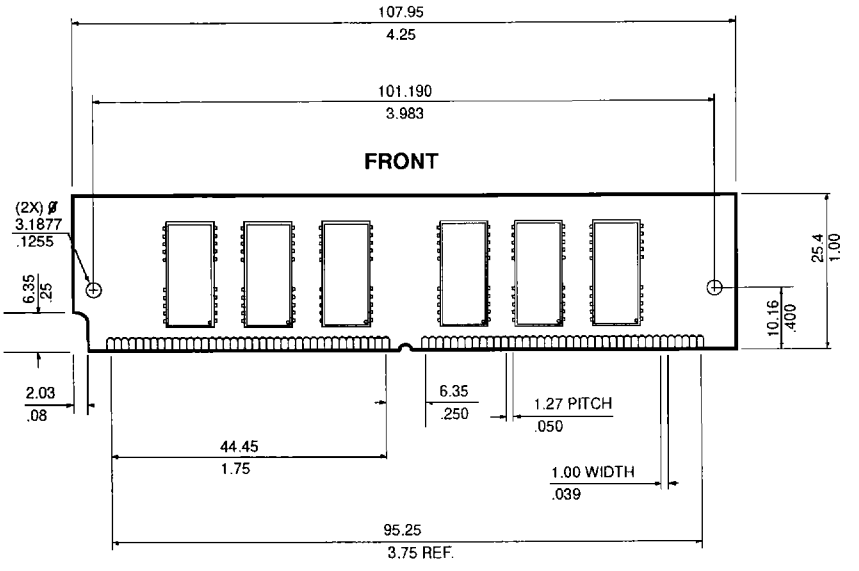
Note: $\overline{WE}$, D_{IN} are "H" or "L"

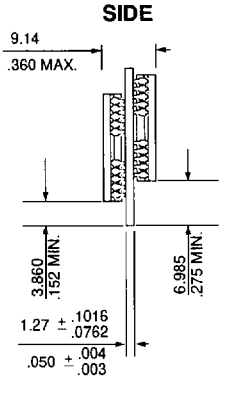
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing





NOTE: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES