2K Commercial / Industrial — **X2002 / X2002I** — **256 x 8 Bit**

Nonvolatile Static RAM

FEATURES

- **Nonvolatile Data Integrity**
- **Automatic Store Timing**
- **Store and Array Recall Combined on One Line ($\overline{NE}$)**
- **Enhanced Store Protection**
- **Infinite E^2PROM Array Recall, and RAM Read and Write Cycles**
- **Single 5V Supply**
- **100 Year Data Retention**
- **JEDEC Approved Pinout for Byte-Wide Memories**
- **Fast Access Time: 200ns Max.**
- **Automatic Recall on Power-Up**

DESCRIPTION

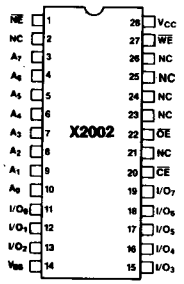
The Xicor X2002 is a byte-wide NOVRAM* featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile electrically erasable PROM (E^2PROM). The X2002 is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5 volt programmable nonvolatile memories. The X2002 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, EPROMs and E^2PROMs.

The NOVRAM design allows data to be easily transferred from RAM to E^2PROM (store) and E^2PROM to RAM (recall). With $\overline{NE}$ LOW, these functions are performed in the same manner as RAM read and write operations. The store operation is completed in 10ms or less and the recall operation is completed in 5μs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E^2PROM, and a minimum 100,000 store operations to the E^2PROM. Data retention is specified to be greater than 100 years.

*NOVRAM is Xicor's nonvolatile static RAM device.

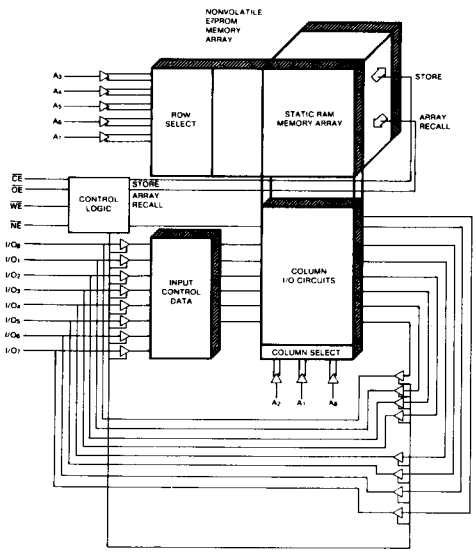
PIN CONFIGURATION



PIN NAMES

A_0–A_7	Address Inputs
I/O_0–I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{NE}$	Nonvolatile Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias X2002 ..... −10°C to +85°C
X2002I ..... −65°C to +135°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature (Soldering,
10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2002 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2002I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	X2002 Limits		X2002I Limits		Units	Test Conditions
		Min.	Max.	Min.	Max.		
I_{CC}	V_{CC} Current (Active)		90		110	mA	$\overline{CE}$ = V_{IL}, All Other Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{SB}	V_{CC} Current (Standby)		55		70	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Leakage Current		10		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	−1.0	0.8	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		2.4		V	I_{OH} = −400 µA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
$C_{I/O}$[1]	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}[1]	Input Capacitance	6	pF	V_{IN} = 0V

Note: (1) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0 to 3.0 Volts
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{WE}$	$\overline{NE}$	$\overline{OE}$	Mode	I/O	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	H	L	Read RAM	Output Data	Active
L	L	H	X	Write "1" RAM	Input Data High	Active
L	L	H	X	Write "0" RAM	Input Data Low	Active
L	H	L	L	Array Recall	Output High Z	Active
L	L	L	H	Nonvolatile Storing	Output High Z	Active
L	H	H	H	Output Disabled	Output High Z	Active
L	L	L	L	No Operation	Output High Z	Active
L	H	L	H	No Operation	Output High Z	Active

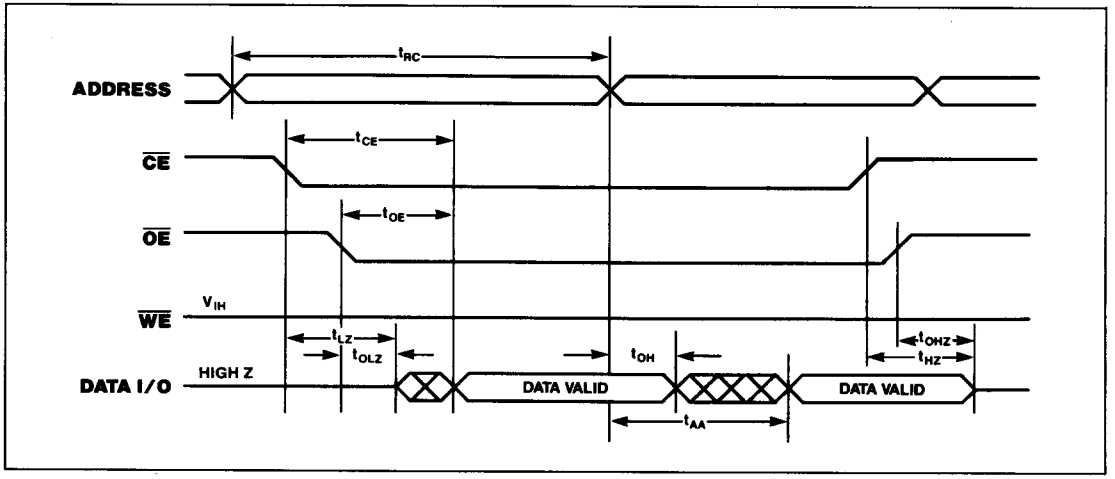
A.C. CHARACTERISTICS

X2002 T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2002I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2002-20 X2002I-20		X2002-25 X2002I-25		X2002 X2002I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	Chip Enable Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	Output Enable Access Time		70		100		150	ns
t_{LZ}	Chip Enable to Output in Low Z	10		10		10		ns
t_{HZ}	Chip Disable to Output in High Z	10	100	10	100	10	100	ns
t_{OLZ}	Output Enable to Output in Low Z	10		10		10		ns
t_{OHZ}	Output Disable to Output in High Z	10	100	10	100	10	100	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

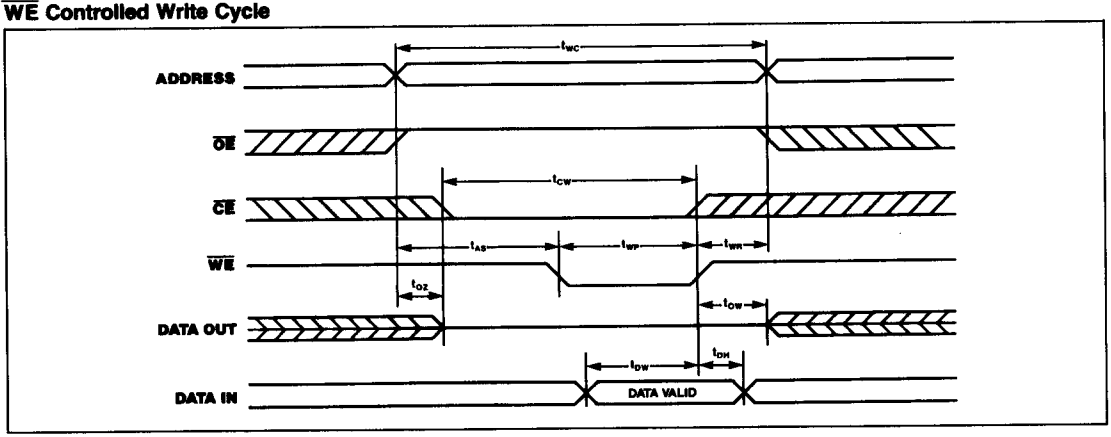
Read Cycle



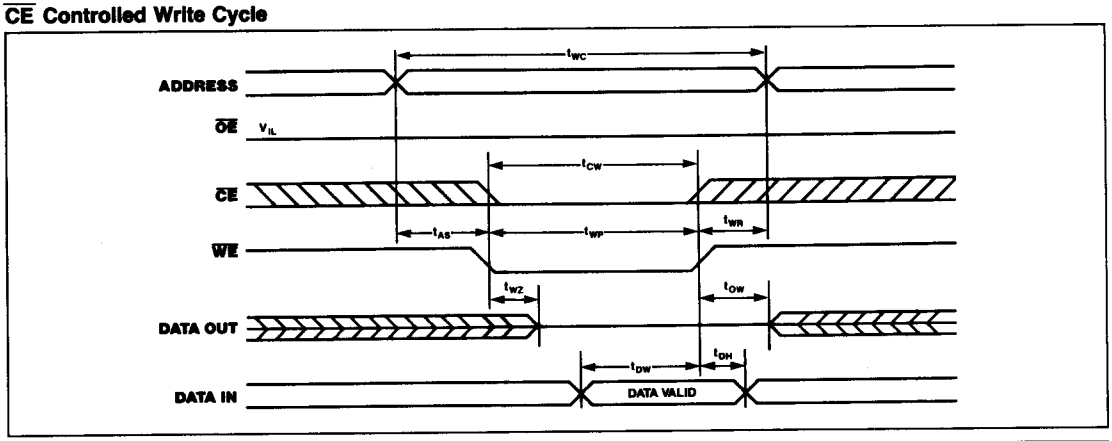
Write Cycle Limits

Symbol	Parameter	X2002-20 X2002I-20		X2002-25 X2002I-25		X2002 X2002I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	200		250		300		ns
t_{CW}	Chip Enable to End of Write Input	200		250		300		ns
t_{AS}	Address Set-Up Time	0		0		0		ns
t_{WP}	Write Pulse Width	120		150		200		ns
t_{WR}	Write Recovery Time	0		0		0		ns
t_{DW}	Data Valid to End of Write	120		150		200		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	10	100	10	100	ns
t_{OW}	Output Active from End of Write	10		10		10		ns
t_{OZ}	Output Enable to Output in High Z	10	100	10	100	10	100	ns

$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle

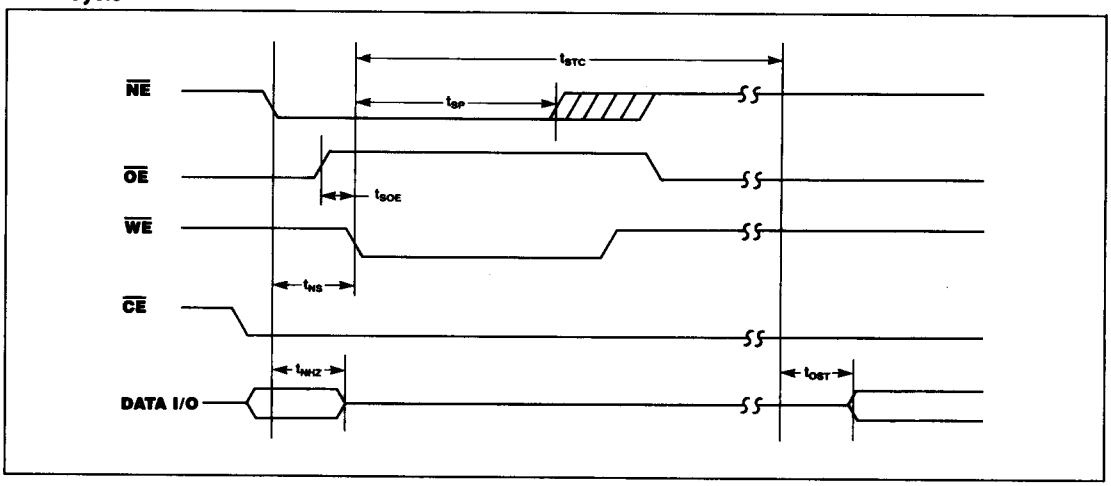


Store Cycle Limits

Symbol	Parameter	X2002-20 X2002I-20		X2002-25 X2002I-25		X2002 X2002I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{STC}	Store Cycle Time		10		10		10	ms
t_{SP}[2]	Store Pulse Width	120		150		200		ns
t_{NHZ}	Nonvolatile Enable to Output in High Z		100		100		100	ns
t_{OST}	Output Active from End of Store	10		10		10		ns
t_{SOE}	$\overline{OE}$ Disable to STORE Function	20		20		20		ns
t_{NS}	$\overline{NE}$ Setup Time from $\overline{WE}$	0		0		0		ns

Note: (2) Once t_{SP} has been satisfied by ($\overline{NE}$, $\overline{OE}$, $\overline{WE}$, $\overline{CE}$) the store cycle is completed automatically, while ignoring all inputs.

Store Cycle

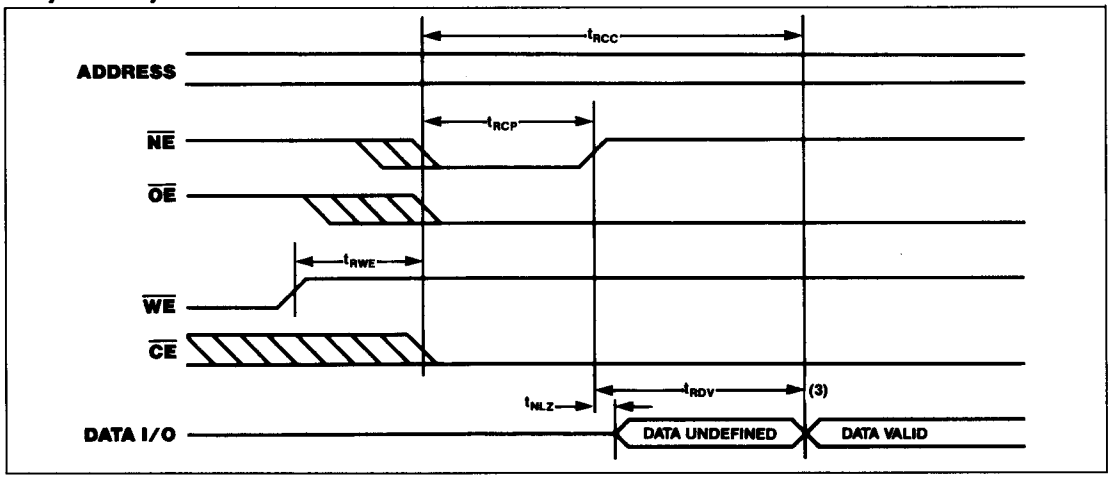


Array Recall Cycle Limits

Symbol	Parameter	X2002-20 X2002I-20		X2002-25 X2002I-25		X2002 X2002I		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCC}	Array Recall Cycle Time		5.0		5.0		5.0	µs
t_{RCP}(3)	Recall Pulse Width to Initiate Recall	120		150		200		ns
t_{NLZ}	Recall to Output in Low Z	0		0		0		ns
t_{RWE}	$\overline{WE}$ Setup Time to $\overline{NE}$	0		0		0		ns
t_{RDV}(3)	Recall to Data Valid	0.1	4.9	0.1	4.9	0.1	4.9	µs

Note: (3) The X2002 features internal control of the Recall Cycle time. t_{RCP} is the minimum input pulse width required to initiate a recall. Once initiated the Recall Cycle will have a completion time of t_{RDV} which varies. As t_{RCP} is increased above its minimum value, the cycle time t_{RCC} remains constant and t_{RDV} is reduced accordingly until reaching its minimum value. If t_{RCP} is increased further, t_{RDV} remains constant and the entire cycle time will increase.

Array Recall Cycle



PIN DESCRIPTIONS

Addresses (A_0–A_7)

The address inputs select an 8-bit word during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read and recall operations. Output Enable LOW disables a store operation regardless of the state of $\overline{CE}$, $\overline{WE}$ or $\overline{NE}$.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2002 through the I/O pins. The I/O pins are placed in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or when $\overline{NE}$ is LOW.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to both the static RAM and stores to the E^2PROM.

Nonvolatile Enable ($\overline{NE}$)

The Nonvolatile Enable input controls all accesses to the E^2PROM array (store and recall functions).

DEVICE OPERATION

The $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$ inputs control the X2002 operation. The X2002 byte-wide NOVRAM uses a 2-line control architecture to eliminate bus contention in a system environment. The I/O bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH, or when $\overline{NE}$ is LOW.

RAM OPERATIONS

RAM read and write operations are performed as they would be with any static RAM. A read operation requires $\overline{CE}$ and $\overline{OE}$ to be LOW with $\overline{WE}$ and $\overline{NE}$ HIGH. A write operation requires $\overline{CE}$ and $\overline{WE}$ to be LOW with $\overline{NE}$ HIGH. There is no limit to the number of read or write operations performed to the RAM portion of the X2002.

NONVOLATILE OPERATIONS

With $\overline{NE}$ LOW, recall and store operations are performed in the same manner as RAM read and write operations. A recall operation causes the entire contents of the E^2PROM to be written into the RAM array. The time required for the operation to complete is 5µs or less. A store operation causes the entire contents of the RAM array to be stored in the nonvolatile E^2PROM. The time for the operation to complete is 10ms or less, typically 5ms.

POWER-UP RECALL

Upon power-up (V_{CC}), the X2002 performs an automatic array recall. When V_{CC} minimum is reached, the recall is initiated, regardless of the state of $\overline{CE}$, $\overline{OE}$, $\overline{WE}$ and $\overline{NE}$.

WRITE PROTECTION

The X2002 has four write protect features that are employed to protect the contents of both the nonvolatile memory and the RAM.

- Noise Protection—A $\overline{WE}$ pulse of less than 20ns will *not* initiate a write cycle.
- Combined Signal Noise Protection—A combined $\overline{WE}$ and $\overline{NE}$ ($\overline{WE} \cdot \overline{NE}$) pulse of less than 20ns will *not* initiate a store cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$ 3v, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, $\overline{CE}$ HIGH or $\overline{NE}$ HIGH during power-up or power-down, will prevent an inadvertent store operation.

ENDURANCE

The endurance specification of a device is characterized by the predicted *first* bit failure to occur in the entire memory (device or system) array rather than the average or typical value for the array. Since endurance is limited by the number of electrons trapped in the oxide during data changes, Xicor NOVRAMs are designed to minimize the number of changes an E^2PROM bit cell undergoes during store operations. Only those bits in the E^2PROM that are different from their corresponding location in the RAM will be "cycled" during a nonvolatile store. This characteristic reduces unnecessary cycling of any of the rest of the bits in the array, thereby increasing the potential endurance of each bit and increasing the potential endurance of the entire array. Reliability data documented in RR504, the *Xicor Reliability Report on Endurance,* and additional reports are available from Xicor.

Part Number	Store Cycles	Data Changes Per Bit
X2002	100,000	10,000
X2002I	100,000	10,000