National Semiconductor

August 1998

100355
Low Power Quad Multiplexer/Latch

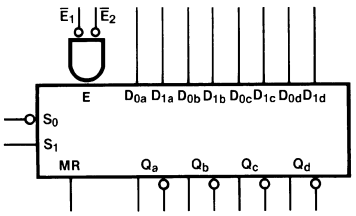
General Description

The 100355 contains four transparent latches, each of which can accept and store data from two sources. When both Enable ($\overline{E}_n$) inputs are LOW, the data that appears at an output is controlled by the Select (S_n) inputs, as shown in the Operating Mode table. In addition to routing data from either D_0 or D_1, the Select inputs can force the outputs LOW for the case where the latch is transparent (both Enables are LOW) and can steer a HIGH signal from either D_0 or D_1 to an output. The Select inputs can be tied together for applications requiring only that data be steered from either D_0 or D_1. A positive-going signal on either Enable input latches the outputs. A HIGH signal on the Master Reset (MR) input overrides all the other inputs and forces the Q outputs LOW. All inputs have 50 kΩ pulldown resistors.

Features

- Greater than 40% power reduction of the 100155
- 2000V ESD protection
- Pin/function compatible with 100155
- Voltage compensated operating range = −4.2V to −5.7V
- Standard Microcircuit Drawing (SMD) 5962-9165401

Logic Symbol

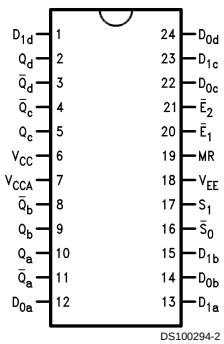


DS100294-1

Pin Names	Description
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)
$\overline{S}_0$, S_1	Select Inputs
MR	Master Reset
D_{na}–D_{nd}	Data Inputs
Q_a–Q_d	Data Outputs
$\overline{Q}_a$–$\overline{Q}_d$	Complementary Data Outputs

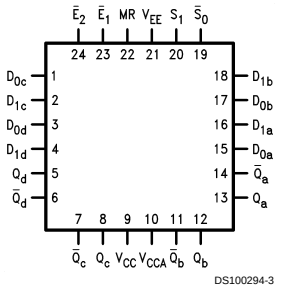
Connection Diagrams

24-Pin DIP



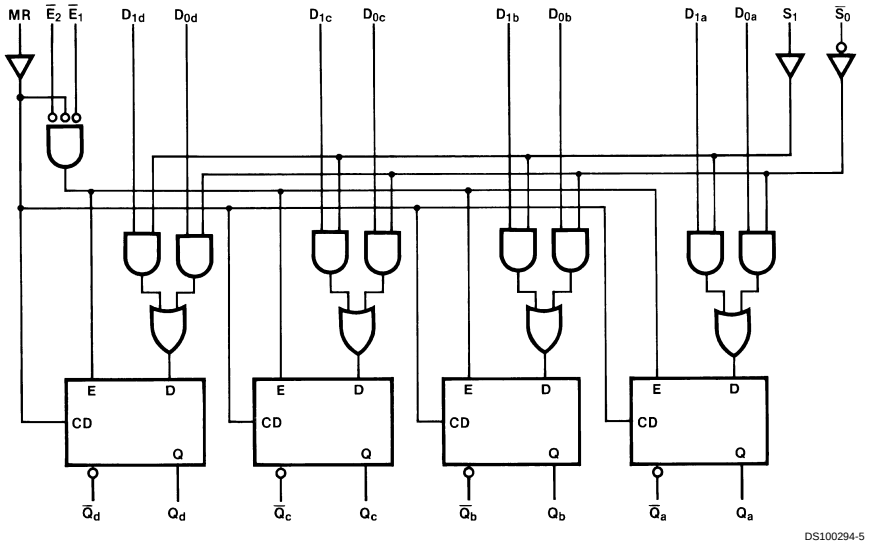
DS100294-2

24-Pin Quad Cerpak



DS100294-3

Logic Diagram



DS100294-5

Operating Mode Table

Controls				Outputs
$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	Q_n
H	X	X	X	Latched (Note 1)
X	H	X	X	Latched (Note 1)
L	L	L	L	D_{0x}
L	L	H	L	$D_{0x} + D_{1x}$
L	L	L	H	L
L	L	H	H	D_{1x}

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Note 1: Stores data present before $\overline{E}$ went HIGH

Truth Table

Inputs							Outputs	
MR	$\overline{E}_1$	$\overline{E}_2$	S_1	$\overline{S}_0$	D_{1x}	D_{0x}	$\overline{Q}_x$	Q_x
H	X	X	X	X	X	X	H	L
L	L	L	H	H	H	X	L	H
L	L	L	H	H	L	X	H	L
L	L	L	L	L	X	H	L	H
L	L	L	L	L	X	L	H	L
L	L	L	L	H	X	X	H	L
L	L	L	H	L	H	X	L	H
L	L	L	H	L	X	H	L	H
L	L	L	H	L	L	L	H	L
L	H	X	X	X	X	X	Latched (Note 1)	
L	X	H	X	X	X	X	Latched (Note 1)	

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications. Above which the useful life may be impaired.

Storage Temperature (T_{STG})	−65˚C to +150˚C
Maximum Junction Temperature (T_J)	
Ceramic	+175˚C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
Input Voltage (DC)	V_{EE} to +0.5V
Output Current (DC Output HIGH)	−50 mA
ESD (Note 3)	≥2000V

Recommended Operating Conditions

Case Temperature (T_C)	
Military	−55˚C to +125˚C
Supply Voltage (V_{EE})	−5.7V to −4.2V

Note 2: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: ESD testing conforms to MIL-STD-883, Method 3015.

Military Version DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55˚C to +125˚C

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (Max)}$ or $V_{IL\ (Min)}$	Loading with 50Ω to −2.0V	(Notes 4, 5, 6)
		−1085	−870	mV	−55˚C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0˚C to +125˚C			
		−1830	−1555	mV	−55˚C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0˚C to +125˚C	V_{IN} = $V_{IH\ (Min)}$ or $V_{IL\ (Max)}$	Loading with 50Ω to −2.0V	(Notes 4, 5, 6)
		−1085		mV	−55˚C			
V_{OLC}	Output LOW Voltage		−1610	mV	0˚C to +125˚C			
			−1555	mV	−55˚C			
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55˚C to +125˚C	Guaranteed HIGH Signal for ALL Inputs		(Notes 4, 5, 6, 7)
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55˚C to +125˚C	Guaranteed LOW Signal for ALL Inputs		(Notes 4, 5, 6, 7)
I_{IL}	Input LOW Current	0.50		µA	−55˚C to +125˚C	V_{EE} = −4.2V V_{IN} = $V_{IL\ (Min)}$		(Notes 4, 5, 6)
I_{IH}	Input HIGH Current							
	$\overline{S}_0$, S_1		220	µA	0˚C to +125˚C	V_{EE} = −5.7V V_{IN} = $V_{IH\ (Max)}$		(Notes 4, 5, 6)
	$\overline{E}_1$, $\overline{E}_2$		350					
	D_{na}–D_{nd}		340					
	MR		430					
	$\overline{S}_0$, S_1		320	µA	−55˚C			
	$\overline{E}_1$, $\overline{E}_2$		500					
	D_{na}–D_{nd}		490					
	MR		630					
I_{EE}	Power Supply Current	−95	−32	mA	−55˚C to +125˚C	Inputs Open		(Notes 4, 5, 6)

Note 4: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55˚C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 5: Screen tested 100% on each device at −55˚C, +25˚C, and +125˚C Temp., Subgroups 1, 2, 3, 7, and 8.

Note 6: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25˚, +125˚C, and −55˚C Temp., Subgroups 1, 2, 3, 7, and 8.

Note 7: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

Military Version
AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = +25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	Propagation Delay D_{na}–D_{nd} to Output (Transparent Mode)	0.40	2.30	0.50	2.20	0.50	2.60	ns	*Figures 1, 2*	(Notes 8, 9, 10)
t_{PLH} t_{PHL}	Propagation Delay $\overline{S}_0$, S_1 to Output (Transparent Mode)	0.60	3.00	0.80	2.70	0.80	3.20	ns		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$, $\overline{E}_2$ to Output	0.50	2.60	0.60	2.30	0.70	2.70	ns		
t_{PLH} t_{PHL}	Propagation Delay MR to Output	0.60	2.80	0.70	2.60	0.70	2.90	ns	*Figures 1, 3*	(Notes 8, 9, 10)
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.40	1.90	0.40	1.90	0.40	1.90	ns	*Figures 1, 2*	(Note 11)
t_S	Setup Time									
	D_{na}–D_{nd}	0.90		0.90		0.90		ns	*Figure 4*	(Note 11)
	$\overline{S}_0$, S_1	2.40		2.40		2.40				
	MR (Release Time)	1.50		1.50		1.50			*Figure 3*	
t_H	Hold Time									
	D_{na}–D_{nd}	0.40		0.40		0.40		ns	*Figure 4*	(Note 11)
	$\overline{S}_0$, S_1	0.00		0.00		0.00				
t_{pw} (L)	Pulse Width LOW $\overline{E}_1$, $\overline{E}_2$	2.00		2.00		2.00		ns	*Figure 2*	(Note 11)
t_{pw} (H)	Pulse Width HIGH MR	2.00		2.00		2.00		ns	*Figure 3*	(Note 11)

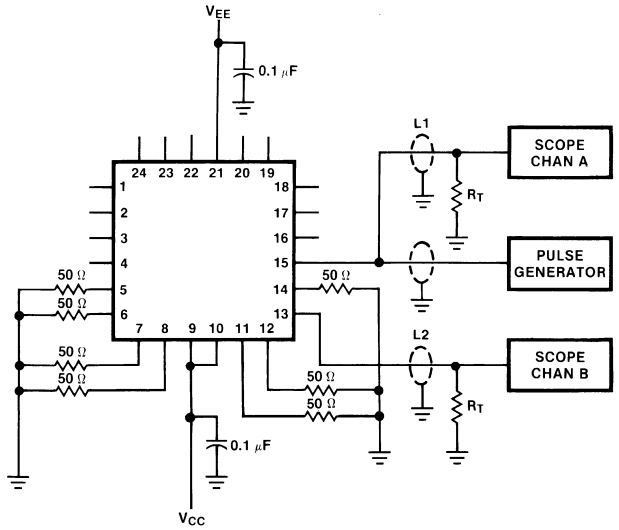
Note 8: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 9: Screen tested 100% on each device at +25°C, Temperature only, Subgroup A9.

Note 10: Sample tested (Method 5005, Table 1) on each Mfg. lot at +25°, Subgroup A9, and at +125°C, and −55°C Temp., Subgroups A10 & A11.

Note 11: Not tested at +25°C, +125°C and −55°C Temperature (design characterization data).

Test Circuit



Notes:

V_{CC}, V_{CCA} = +2V, V_{EE} = −2.5V
L1 and L2 = equal length 50Ω impedance lines
R_T = 50Ω terminator internal to scope
Decoupling 0.1 µF from GND to V_{CC} and V_{EE}
All unused outputs are loaded with 50Ω to GND
C_L = Fixture and stray capacitance ≤ 3 pF
Pin numbers shown are for flatpak; for DIP see logic symbol

FIGURE 1. AC Test Circuit (Using Quad Cerpak)

Switching Waveforms

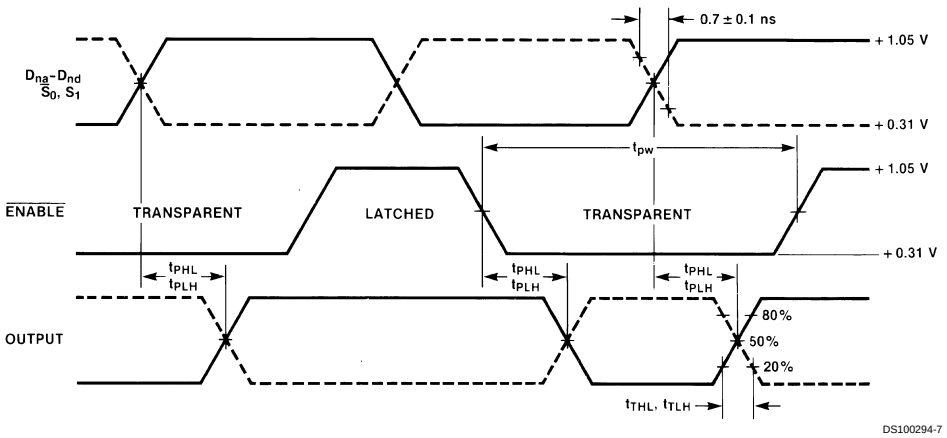


FIGURE 2. Enable Timing

Switching Waveforms (Continued)

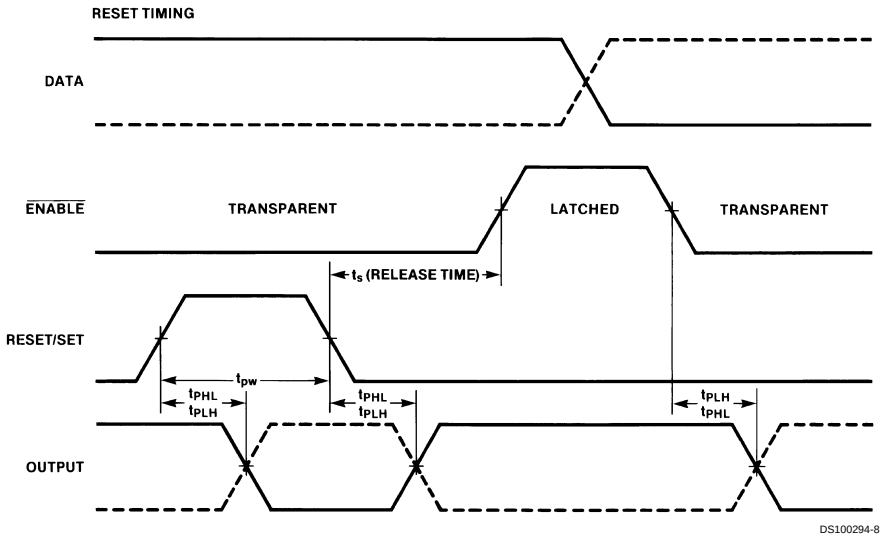
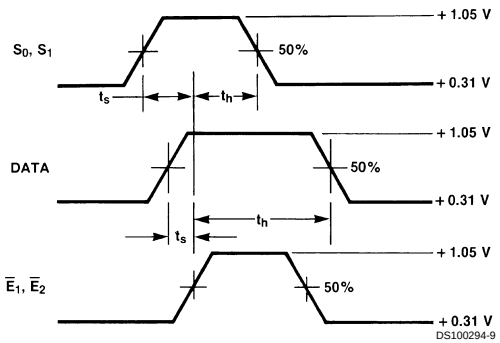


FIGURE 3. Reset Timing

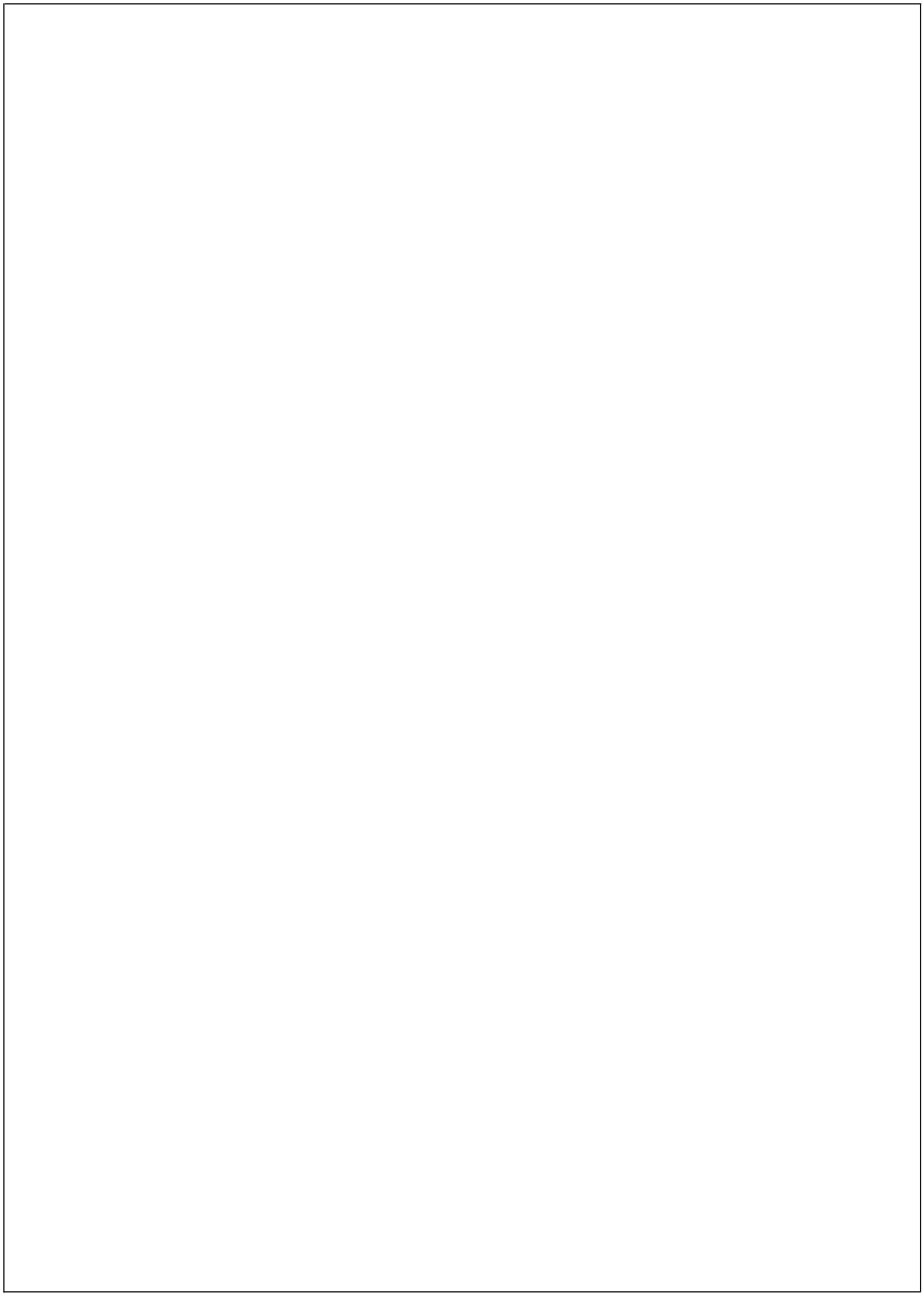


Notes:

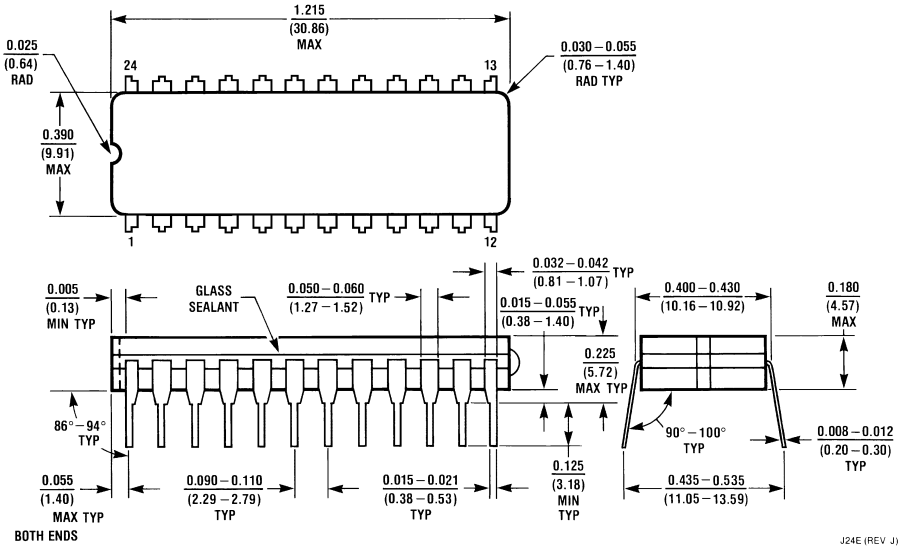
t_S is the minimum time before the transition of the enable that information must be present at the data input.

t_h is the minimum time after the transition of the enable that information must remain unchanged at the data input.

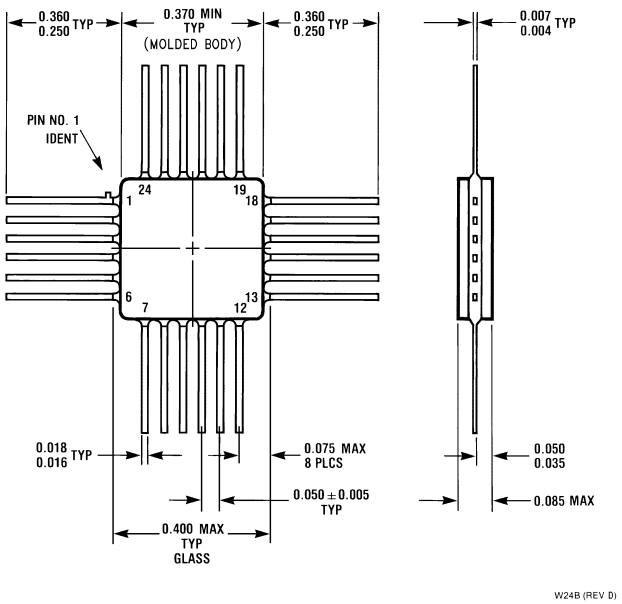
FIGURE 4. Data Setup and Hold Times



Physical Dimensions inches (millimeters) unless otherwise noted



24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24E



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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100355 Product Folder

Low Power Quad Multiplexer/Latch

General Description | Features | Datasheet | Package & Models | Samples & Pricing

Datasheet

Title	Size in Kbytes	Date	View Online	Download	Receive via Email
100355 Low Power Quad Multiplexer Latch	148 Kbytes	17-Aug-98	View Online	Download	Receive via Email
100355 Mil-Aero Datasheet MN100355-X	108 Kbytes		View Online	Download	Receive via Email

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Package Availability, Models, Samples & Pricing

Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	Pins	MSL		SPICE	IBIS		Qty	$US each		
5962-9165401MXA	CERDIP	24	MSL	Full production	N/A	N/A	Buy Now	50+	$40.8000	rail of 15	[logo]¢Z¢S¢4¢A$E 100355DMQB /Q 5962-9165401MXA
5962-9165401MYA	CERQUAD	24	MSL	Full production	N/A	N/A	Buy Now	50+	$43.2000	rail of 14	[logo]¢Z¢S¢4¢A Q$E 100355 FMQB 5962 -9165401 MYA
5962-9165401VXA	CERDIP	24	MSL	Full production	N/A	N/A		50+	$265.0000	rail of 15	[logo]¢Z¢S¢4¢A$E 100355J-QMLV 5962-9165401VXA
100355WFQMLV	CERQUAD	24	MSL	Preliminary	N/A	N/A				rail of N/A	[logo]¢Z¢S¢4¢A 100355WF QMLV 5962 F9165401 VYA $E
RM100355WFQMLV	CERQUAD	24	MSL	Preliminary	N/A	N/A				rail of N/A	[logo]¢Z¢S¢4¢A RM100355WF QMLV WFR# ¢R $E

5962-9165401VYA	CERQUAD	24	MSL	Full production	N/A	N/A		50+	$265.0000	rail of 14	[logo]¢Z¢S¢4¢A 100355W-QMLV 5962-9165401 VYA $E

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[Information as of 5-Aug-2002]