

# 30–36 GHz GaAs MMIC Power Amplifier



AA032P1-00

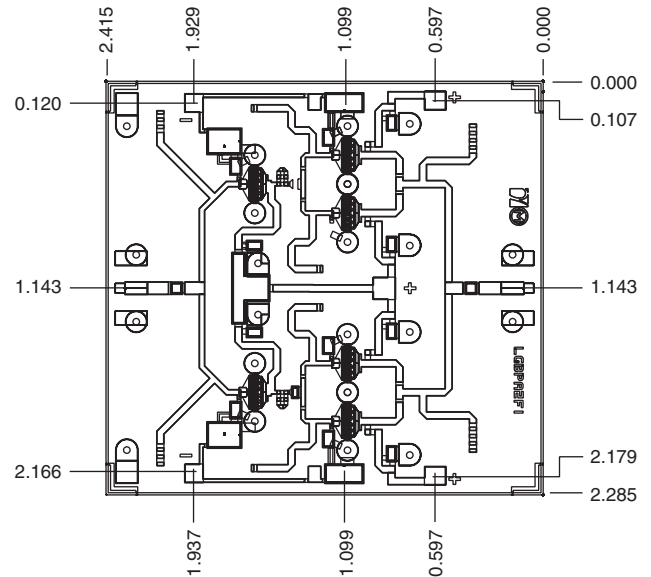
## Features

- Single Gate and Drain Biases
- 25 dBm Typical  $P_{1\text{ dB}}$  Output Power at 31 GHz
- 11 dB Typical Small Signal Gain
- 0.25  $\mu\text{m}$  Ti/Pd/Au Gates
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

## Description

Alpha's two-stage reactively-matched Ka band GaAs MMIC power amplifier has a typical  $P_{1\text{ dB}}$  of 25 dBm with 10 dB associated gain and 15% power added efficiency at 31 GHz. The chip uses Alpha's proven 0.25  $\mu\text{m}$  MESFET technology, and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate solder or epoxy die attach processes. Single gate and drain bias pads cover both stages, with the added convenience that the chip can be wire bonded from either side for either bias. All chips are screened for gain, output power, efficiency and S-parameters prior to shipment for guaranteed performance. A broad range of applications exist in both the military and commercial areas where high power and gain are required.

## Chip Outline



Dimensions indicated in mm.  
All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.  
Chip thickness = 0.1 mm.

## Absolute Maximum Ratings

| Characteristic                   | Value           |
|----------------------------------|-----------------|
| Operating Temperature ( $T_C$ )  | -55°C to +90°C  |
| Storage Temperature ( $T_{ST}$ ) | -65°C to +150°C |
| Bias Voltage ( $V_D$ )           | 7 $V_{DC}$      |
| Power In ( $P_{IN}$ )            | 22 dBm          |
| Junction Temperature ( $T_J$ )   | 175°C           |

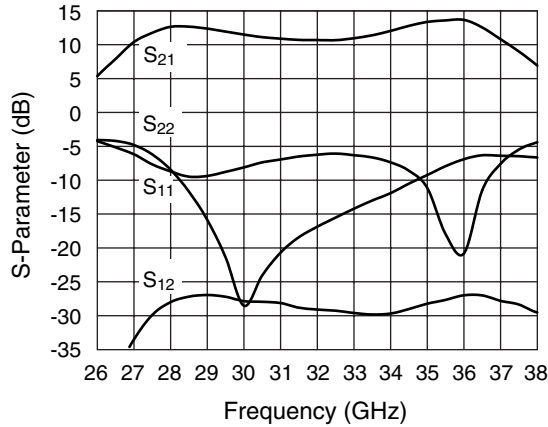
## Electrical Specifications at 25°C ( $V_{DS} = 6\text{ V}$ , $V_{GS} = -1\text{ V}$ )

| Parameter                             | Condition            | Symbol            | Min. | Typ. <sup>2</sup> | Max. | Unit |
|---------------------------------------|----------------------|-------------------|------|-------------------|------|------|
| Drain Current (at Saturation)         |                      | $I_{DS}$          |      | 400               | 450  | mA   |
| Small Signal Gain                     | F = 30–31, 34–36 GHz | G                 | 8    | 11                |      | dB   |
| Input Return Loss                     | F = 30–31, 34–36 GHz | $RL_I$            |      | -7                | -6   | dB   |
| Output Return Loss                    | F = 30–31, 34–36 GHz | $RL_O$            |      | -8                | -6   | dB   |
| Output Power at 1 dB Gain Compression | F = 31 GHz           | $P_{1\text{ dB}}$ | 24   | 25                |      | dBm  |
| Saturated Output Power                | F = 31 GHz           | $P_{SAT}$         | 25   | 27                |      | dBm  |
| Gain at Saturation                    | F = 31 GHz           | $G_{SAT}$         |      | 8                 |      | dB   |
| Thermal Resistance <sup>1</sup>       |                      | $\theta_{JC}$     |      | 42                |      | °C/W |

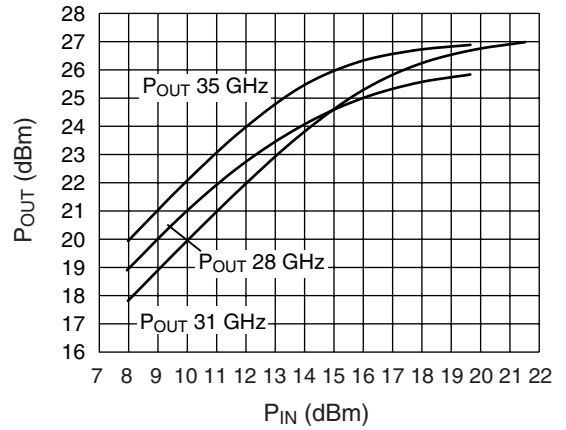
1. Calculated value based on measurement of discrete FET.

2. Typical represents the median parameter value across the specified frequency range for the median chip.

### Typical Performance Data

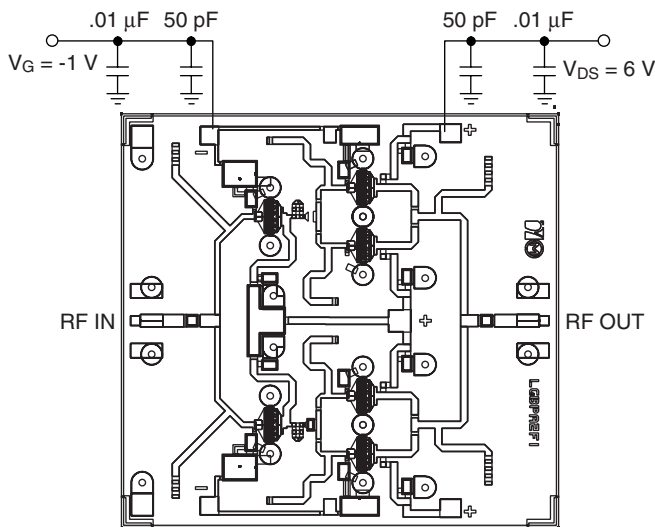


Typical Small Signal Performance S-Parameters ( $V_{DS} = 6\text{ V}$ )



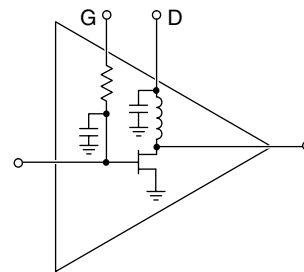
Typical Output Power Compression

### Bias Arrangement



The AA032P1-00 can be biased from either or both sides for both gate and drain biases. For biasing on, adjust  $V_{GS}$  from zero to approximately -1 V. Adjust  $V_{DS}$  from zero to the desired value (4 V–6 V recommended). Adjust  $V_{GS}$  to achieve the desired  $I_{DS}$  (400 mA recommended). For biasing off, reverse the biasing on procedure.

### Circuit Schematic



Detail A

