32Mb (2M x 16 bit) Multiplexed UtRAM

Document Title

2M x 16 bit Multiplexed Asynchronous Uni-Transistor Random Access Memory

Revision History

Revision No.	History	Draft Date	Remark
0.0	Initial - Design target	December 19, 2006	Preliminary

Table of Contents

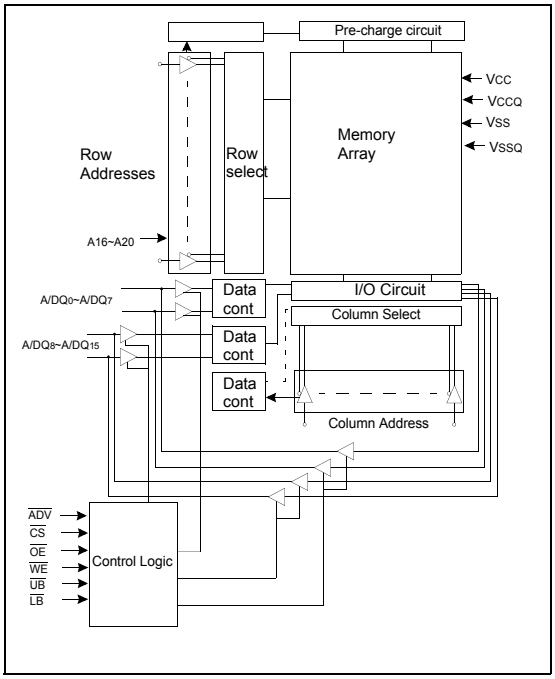
2M x 16 bit Multiplexed Asynchronous Uni-Transistor Random Access Memory

GENERAL DESCRIPTION

The K1S3216B9E is fabricated by SAMSUNG's advanced CMOS technology using one transistor memory cell. The device supports Industrial temperature range. The device supports internal TCSR(Temperature Compensated Self Refresh) for the standby power saving at room temperature range.

FEATURES & FUNCTION BLOCK DIAGRAM

- Process technology: CMOS
- Organization: 2M x 16 bit
- Power supply voltage: 1.7V~1.95V
- Three state outputs
- Supports power saving modes
  - Internal TCSR (Temperature Compensated Self Refresh)



PIN DESCRIPTIONS

Name	Function
$\overline{CS}$	Chip Select Inputs
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
$\overline{ADV}$	Address Valid
A/DQ0~A/DQ15	Address and Data Inputs/Outputs
A16~A20	Address Inputs
Vcc/VccQ	Power Supply(core / I/O)
Vss/VssQ	Ground
$\overline{UB}$	Upper Byte(I/O8~15)
$\overline{LB}$	Lower Byte(I/O0~7)
DNU	Do Not Use

PRODUCT FAMILY

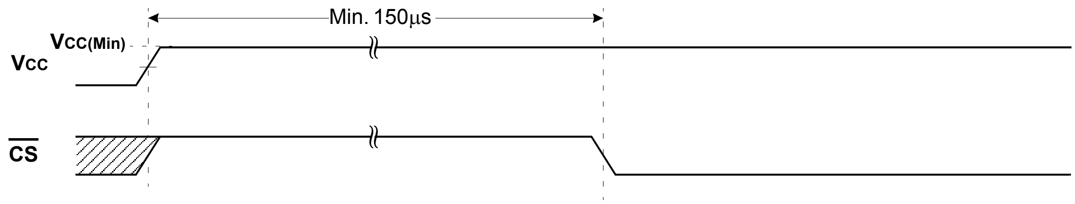
Product Family	Operating Temp.	Vcc / Vccq	Speed (tAA)	Current Consumption	
				Standby (I_{SB1}, Max.)	Operating (I_{CC2}, Max.)
K1S3216B9E-I	Industrial(-40~85°C)	1.7V~1.95V	70ns	TBD < 85°C TBD < 40°C	TBD

POWER UP SEQUENCE

During the Power Up mode, the standby current can not be guaranteed. To get the stable standby current level, at least one cycle of active operation should be implemented regardless of wait time duration. To get the appropriate device operation, be sure to keep the following power up sequence.

1. Apply power.
2. Maintain stable power(Vcc min.=1.7V) for a minimum 150µs with $\overline{CS}$=high.

TIMING WAVEFORM OF POWER UP



FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	$\overline{ADV}$	A/DQ0~15	A16 ~ A21	Mode	Power
H	X[1]	X[1]	X[1]	X[1]	X[1]	High-Z	X[1]	Deselected	Standby
L	H	H	X[1]	X[1]	H	High-Z	X[1]	Output Disabled	Active
L	H	H	X[1]	X[1]	ˉ|_|ˉ	Add. Input	Add. Input	Address Input	Active
L	L	H	L	H	H	Dout	X[1]	Lower Byte Read	Active
L	L	H	H	L	H	Dout	X[1]	Upper Byte Read	Active
L	L	H	L	L	H	Dout	X[1]	Word Read	Active
L	H	L	L	H	H	Din	X[1]	Lower Byte Write	Active
L	H	L	H	L	H	Din	X[1]	Upper Byte Write	Active
L	H	L	L	L	H	Din	X[1]	Word Write	Active

1) X means don't care. (Must be V_{IL} or V_{IH})

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.2 to V_{CCQ}+0.3V	V
Power supply voltage relative to Vss	V_{CC}, V_{CCQ}	-0.2 to 2.5V	V
Power Dissipation	P_D	1.0	W
Storage temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_A	-40 to 85	°C

1) Stresses greater than "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to be used under recommended operating condition. Exposure to absolute maximum rating conditions longer than 1 second may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	Min	Typ	Max	Unit
Power supply voltage(Core, I/O)	V_{CC}, V_{CCQ}	1.7	1.8	1.95	V
Ground(Core, I/O)	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	VCCQ-0.4	-	VCCQ+0.2[2)]	V
Input low voltage	V_{IL}	-0.2[3)]	-	0.4	V

1. T_A=-40 to 85°C, otherwise specified.
2. Overshoot: V_{CCQ} +1.0V in case of pulse width ≤20ns. Overshoot is sampled, not 100% tested.
3. Undershoot: -1.0V in case of pulse width ≤20ns. Undershoot is sampled, not 100% tested.

CAPACITANCE

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Freq.=1MHz, T_A=25°C
2. Capacitance is sampled, not 100% tested.

DC AND OPERATING CHARACTERISTICS

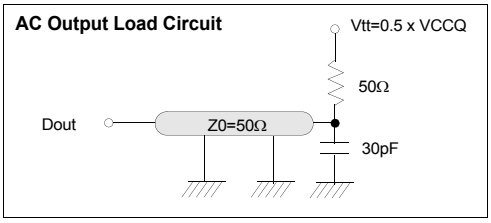
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=VSS to V_{CCQ}		-1	-	1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH}, $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, VIO=V_{SS} to V_{CCQ}		-1	-	1	μA
Average Operating Current	I_{CC2}	Cycle time=70ns, I_{IO}=0mA[2)], 100% duty, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}		-	-	TBD	mA
Output Low Voltage	V_{OL}	I_{OL}=0.2mA		-	-	0.2	V
Output High Voltage	V_{OH}	I_{OH}=-0.2mA		1.4	-	-	V
Standby Current(CMOS)	I_{SB1}[1)]	$\overline{CS}$ and $\overline{ADV}$=V_{CCQ}, Other inputs=0V or V_{CCQ} (Toggle is not allowed)	< 40°C	-	-	TBD	μA
			< 85°C	-	-	TBD	μA

1. Internal TCSR (Temperature Compensated Self Refresh) is used to optimize Refresh cycle below 40°C.
2. I_{IO}=0mA; This parameter is specified with the outputs disabled to avoid external loading effects.

AC OPERATING CONDITIONS

TEST CONDITIONS

(Test Load and Test Input/Output Reference)
Input pulse level: 0.2 to V_{CCQ}-0.2V
Input rising and falling time: 3ns
Input and output reference voltage: 0.5 x V_{CCQ}
Output load: C_L=30pF
V_{CC}:1.7V~1.95V
T_A: -40°C~85°C



TIMING REQUIREMENTS

READ Cycle Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes
Address access time	tAA		70	ns	
$\overline{ADV}$ access time	tAADV		70	ns	
Address setup to $\overline{ADV}$ HIGH	tAVS	5		ns	
Address hold from $\overline{ADV}$ HIGH	tAVH	2		ns	
$\overline{LB}$/$\overline{UB}$ access time	tBA		70	ns	
$\overline{LB}$/$\overline{UB}$ disable to DQ High-Z output	tBHZ		8	ns	1
$\overline{CS}$ HIGH between subsequent Async Operations	tCPH	5		ns	
Chip select access time	tCO		70	ns	
$\overline{CS}$ LOW to $\overline{ADV}$ HIGH	tCVS	7		ns	
Output enable to valid output	tOE		20	ns	
Output disable to DQ High-Z output	tOHZ		8	ns	1
Chip disable to DQ High-Z output	tHZ		8	ns	1
Output ebable to Low-Z output	tOLZ	5		ns	2
READ cycle time	tRC	80		ns	
$\overline{ADV}$ pulse width LOW	tVP	5		ns	
$\overline{ADV}$ HIGH to $\overline{OE}$ LOW	tADVOE	5		ns	
$\overline{OE}$ HIGH to ADV LOW	tOEADV	8		ns	

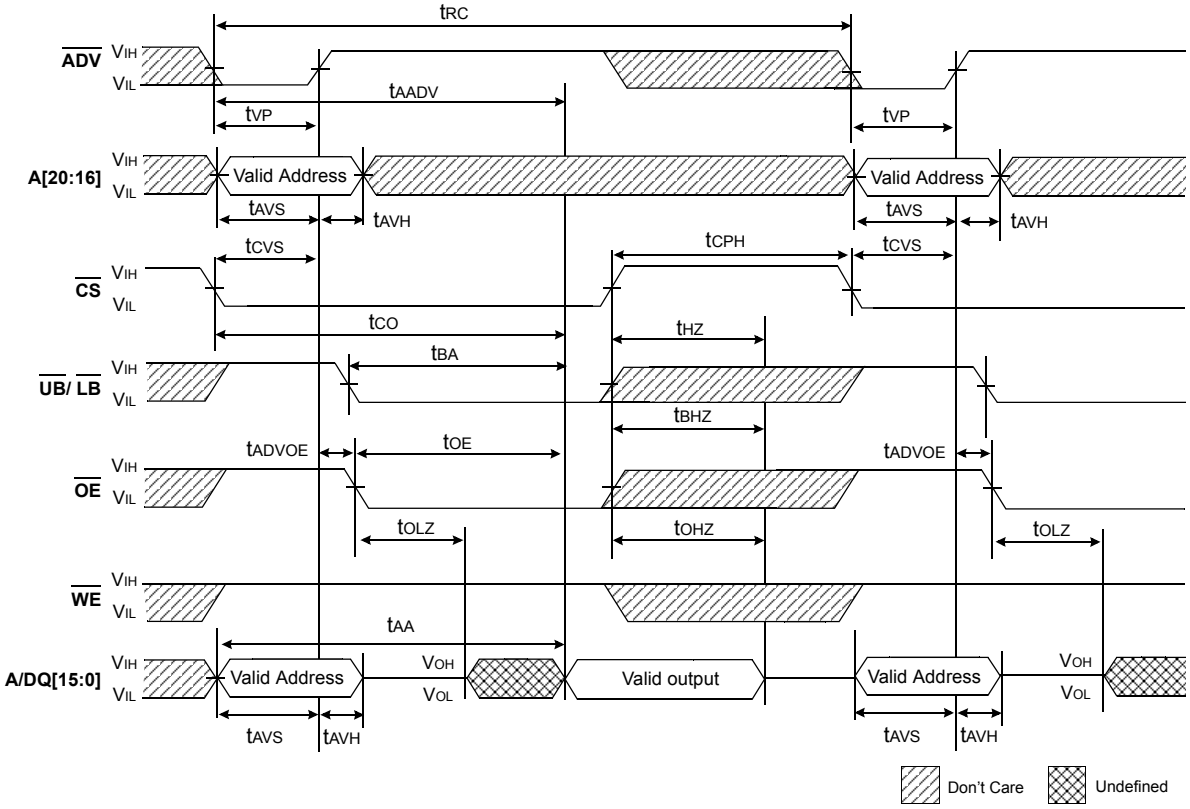
WRITE Cycle Timing Requirements

Parameter	Symbol	Min	Max	Unit	Notes
Address setup to $\overline{ADV}$ going HIGH	tAVS	5		ns	
Address hold from $\overline{ADV}$ HIGH	tAVH	2		ns	
Address valid to end of WRITE	tAW	70		ns	
$\overline{LB}$/$\overline{UB}$ select to end of WRITE	tBW	70		ns	
$\overline{CS}$ HIGH between subsequent async operations	tCPH	5		ns	1
$\overline{CS}$ LOW to $\overline{ADV}$ HIGH	tCVS	7		ns	2
Chip enable to end of WRITE	tCW	70		ns	3
Data HOLD from WRITE time	tDH	0		ns	
Data WRITE setup time	tDW	20		ns	
End WRITE to Low-Z output	tOW	5		ns	2
$\overline{ADV}$ pulse width	tVP	5		ns	
$\overline{ADV}$ setup to end of WRITE	tVS	70		ns	
WRITE pulse width	tWP	55		ns	3
WRITE recovery time	tWR	0		ns	
$\overline{ADV}$ HIGH to $\overline{WE}$ LOW	tADVWE	5		ns	

1. The High-Z timings measure a 100mV transition from either V_{OH} or V_{OL} toward V_{CCQ}/2.
2. The Low-Z timings measure a 100mV transition away from the High-Z (V_{CCQ}/2) level toward either V_{OH} or V_{OL}.
3. $\overline{WE}$ LOW time must be limited to 2.5μs.

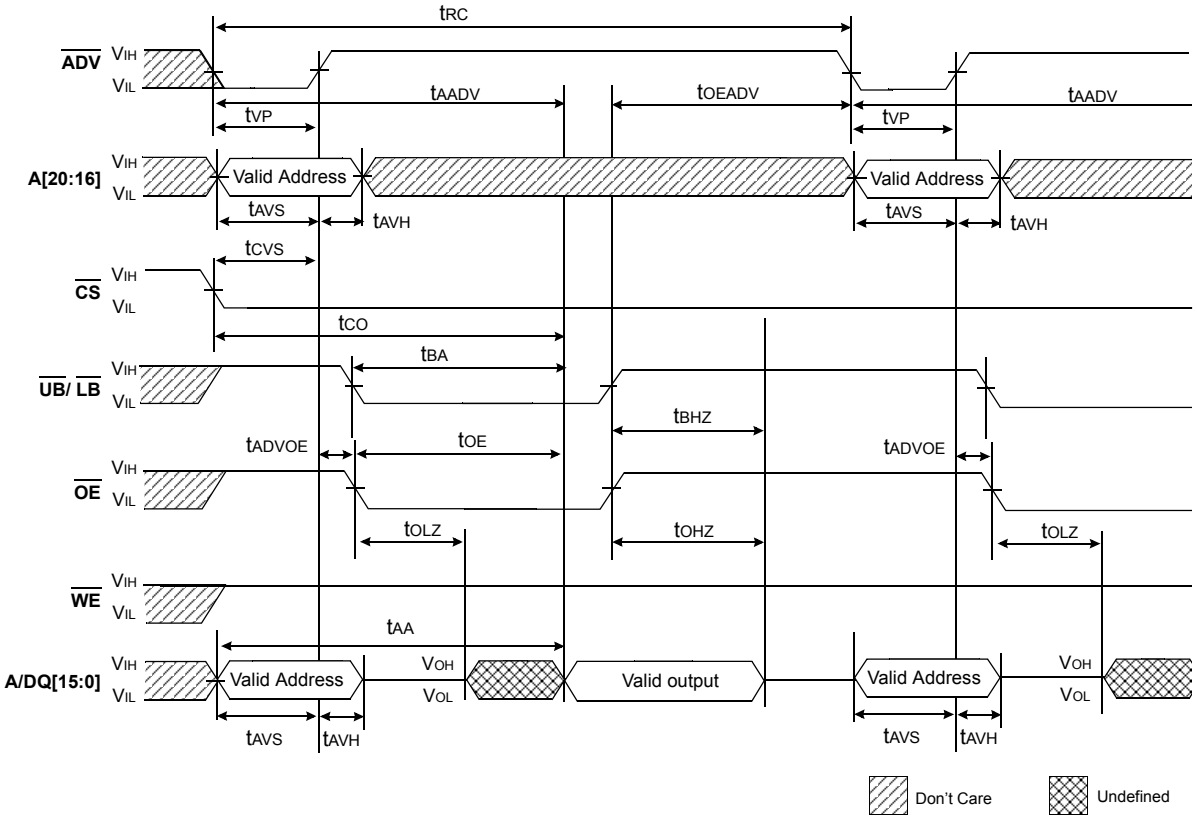
TIMING DIAGRAMS

READ ($\overline{CS}$ controlled)



1. Don't care must be in V_{IL} or V_{IH}.
2. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.
4. t_{OE}(max) is met only when $\overline{OE}$ becomes enabled after t_{AA}(max).
5. If invalid address signals shorter than min. t_{RC} are continuously repeated for over 2.5us, the device needs a normal read timing(t_{RC}) or needs to sustain standby state for min. t_{RC} at least once in every 2.5us.

READ ($\overline{OE}$ controlled)



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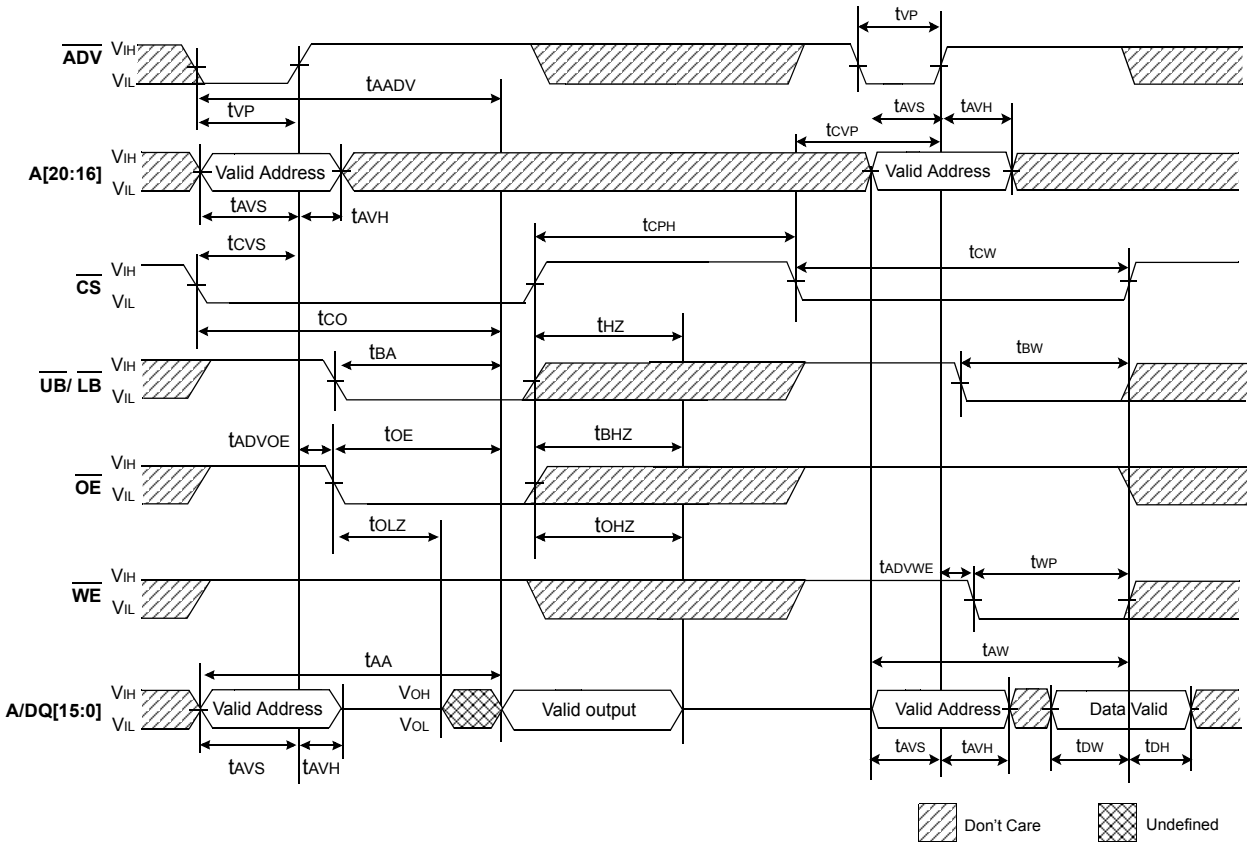
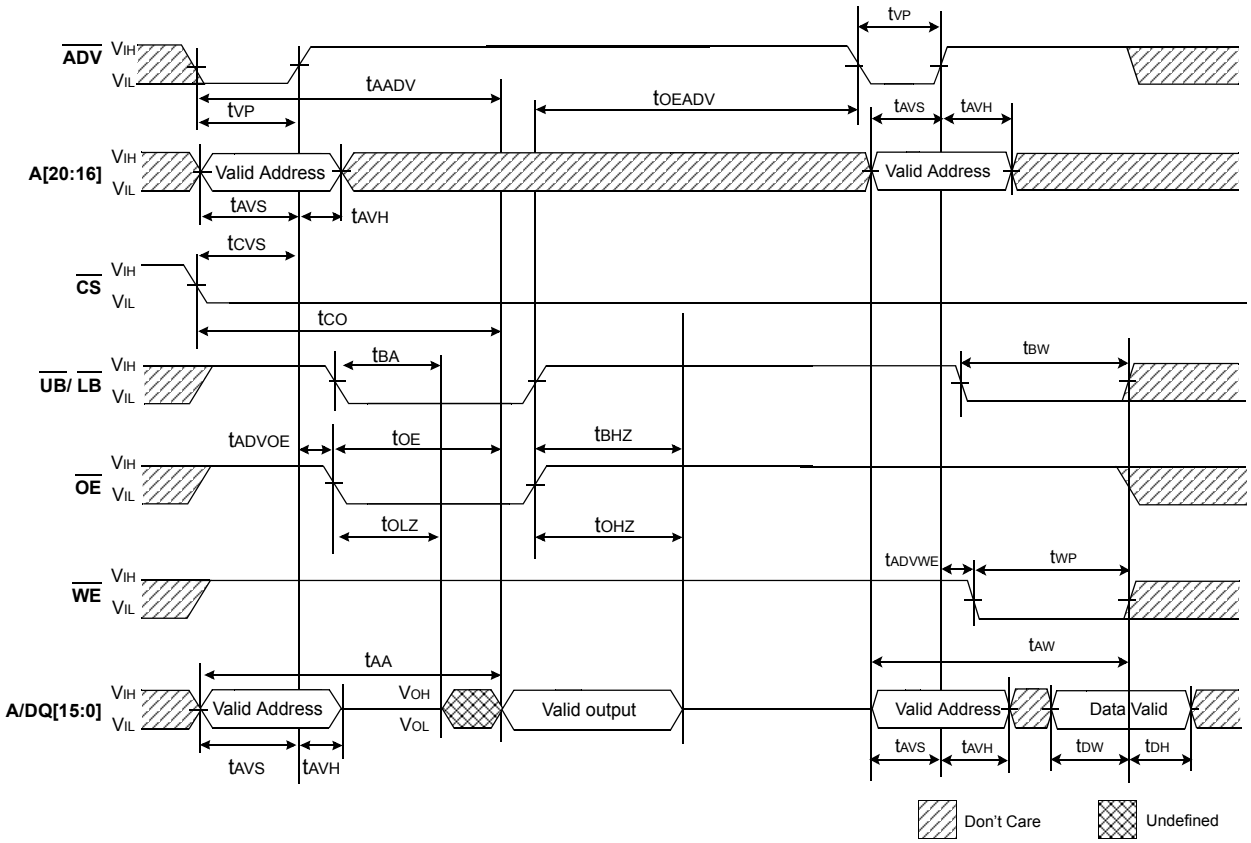
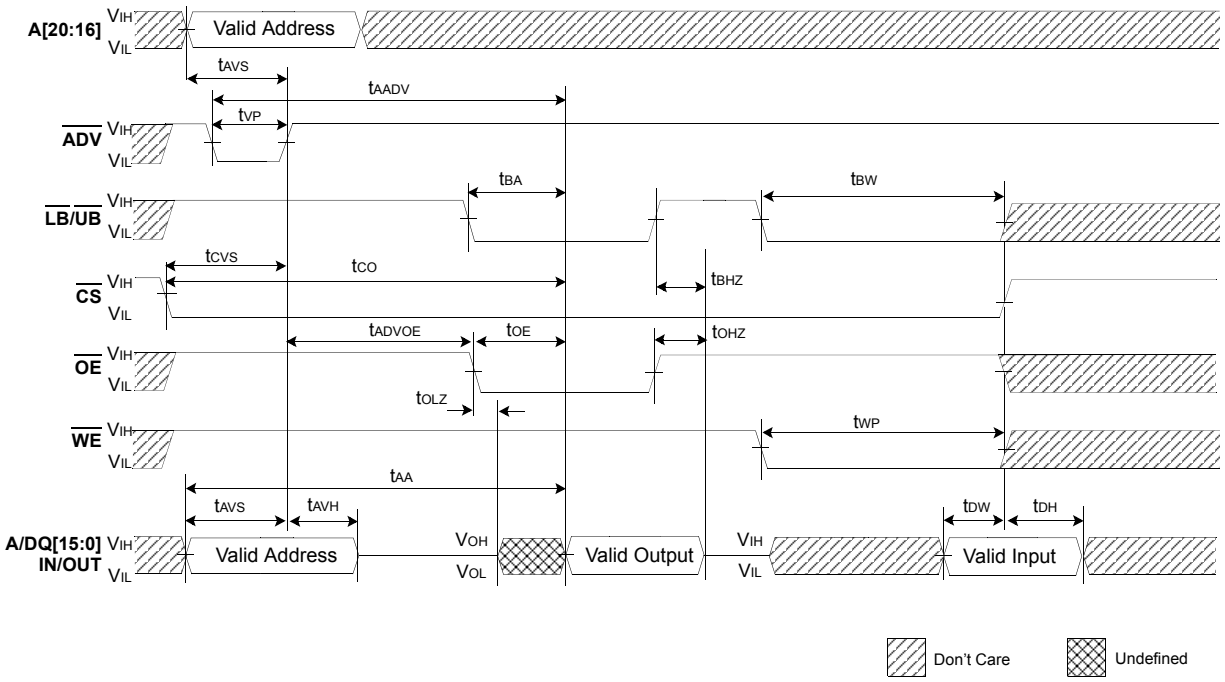
READ Followed by WRITE ($\overline{CS}$ Controlled)



READ Followed by WRITE ($\overline{OE}$, $\overline{WE}$ Controlled)

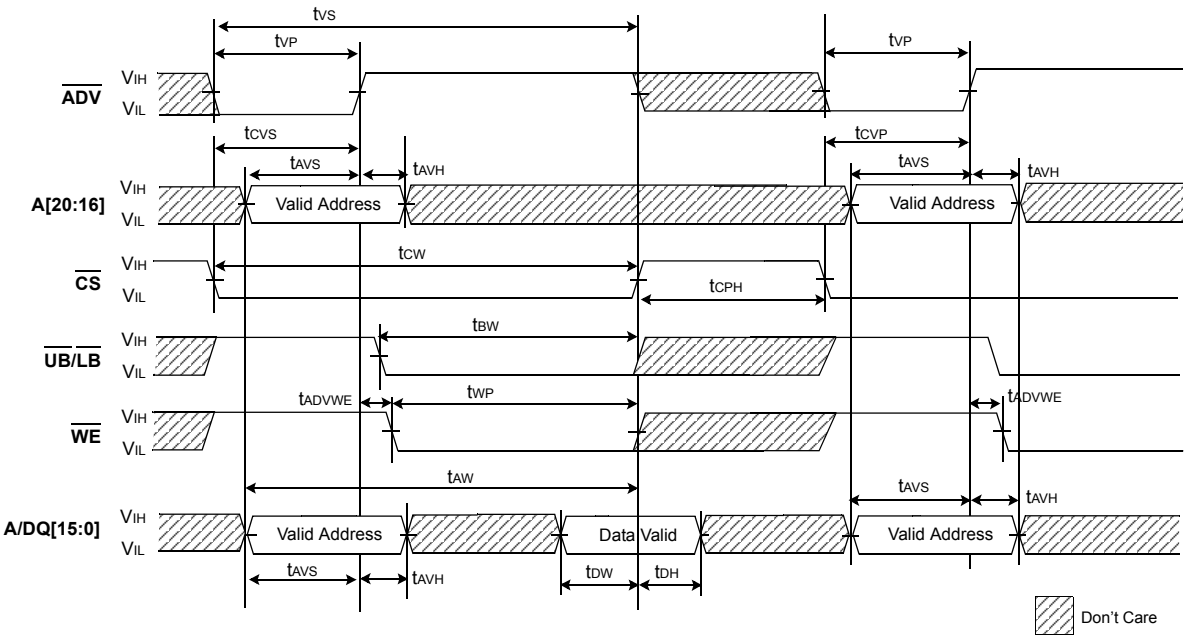


READ Followed by WRITE at the Same Address



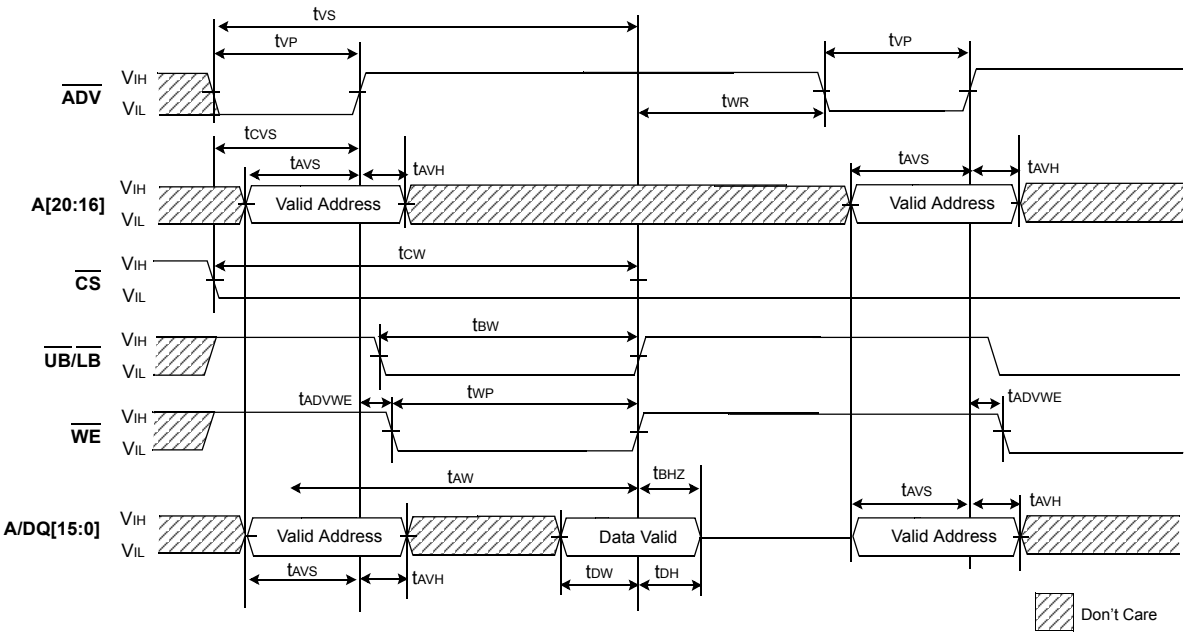
1. The end of the WRITE cycle is controlled by $\overline{CS}$, $\overline{LB}$/$\overline{UB}$, or $\overline{WE}$, whichever de-asserts first.
2. Don't care must be in V_{IL} or V_{IH}.

WRITE ($\overline{CS}$ Controlled)



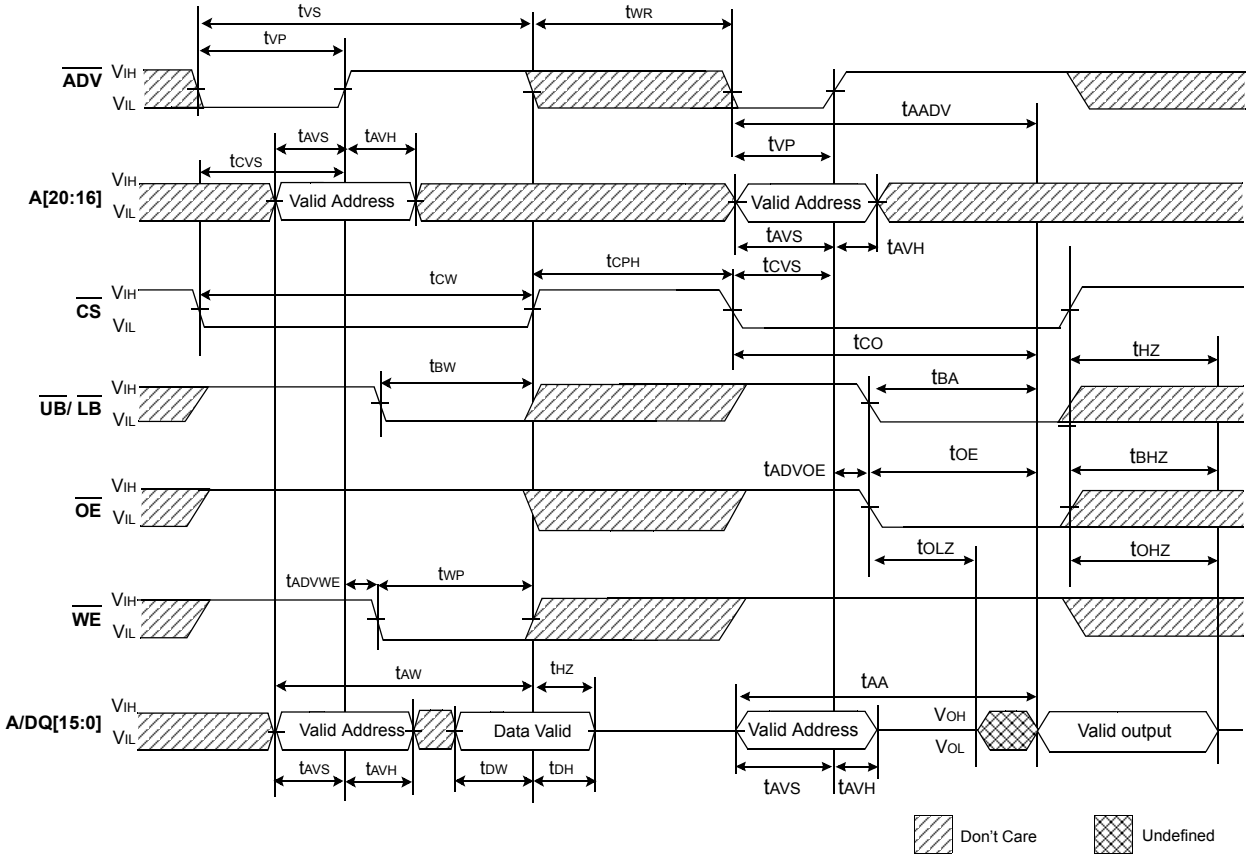
1. Don't care must be in V_{IL} or V_{IH}.
2. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high or $\overline{UB}$/$\overline{LB}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

WRITE (WE, UB/LB Controlled)

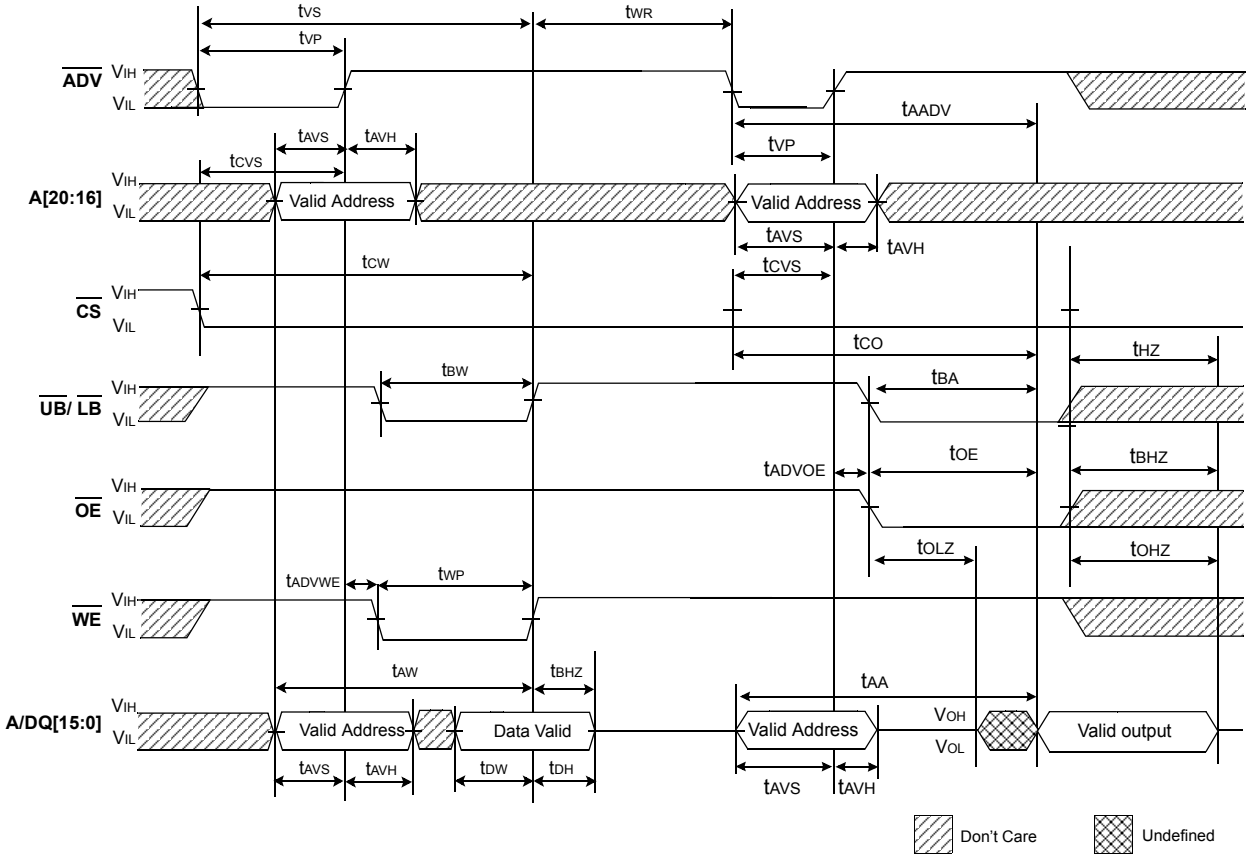


1. Don't care must be in V_{IL} or V_{IH}.
2. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high or $\overline{WE}$ goes high or $\overline{UB}$/$\overline{LB}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the $\overline{CS}$ going low to the end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} is applied in case a write ends with $\overline{CS}$ or $\overline{WE}$ going high.

WRITE Followed by READ ($\overline{CS}$ Controlled)



WRITE Followed by READ (OE, WE Controlled)

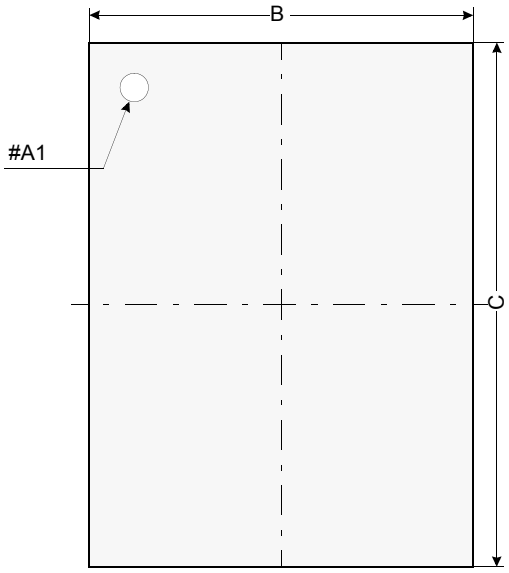


PACKAGE DIMENSION

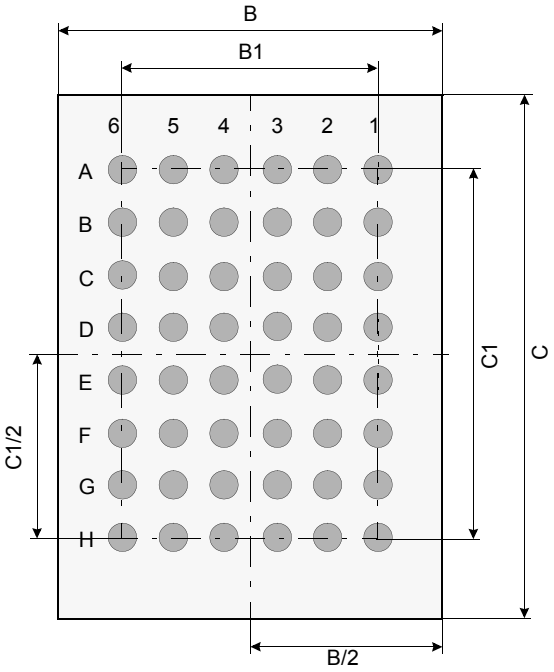
Unit: millimeters

48 BALL FINE PITCH BGA(0.75mm ball pitch)

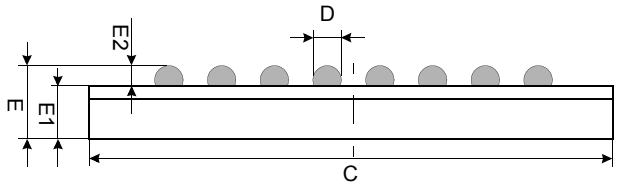
Top View



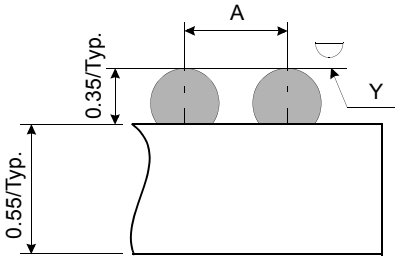
Bottom View



Side View



Detail A



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.40	0.45	0.50
E	-	0.90	1.00
E1	-	0.55	-
E2	0.30	0.35	0.40
Y	-	-	0.08

Notes.

1. Bump counts: 48(8 row x 6 column)
2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
3. All tolerence are ±0.050 unless specified beside figures.
4. Typ : Typical
5. Y is coplanarity: 0.08(Max)