AMERICAN MICROSYSTEMS, INC.

FS6070-01

1:4 HSTL to LVTTL Fanout Buffer IC

October 2000

Preliminary Information

1.0 Features

- Distributes one differential HSTL or HCSL reference clock to two banks of two single-ended LVTTL outputs
- DIVSEL pin selects output divide-by-three or divide-by-four of input frequency
- LVTTL output-enable control for each bank
- Input-to-output propagation delay: 5ns at 66.7MHz
- 16-pin (0.150″) SOIC and (4.4mm) TSSOP available

Figure 1: Pin Configuration

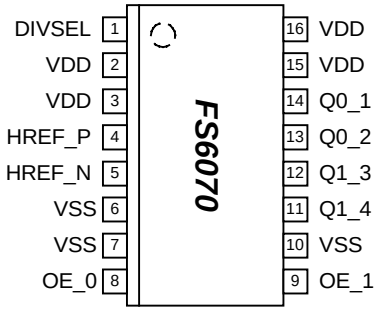


Figure 2: Block Diagram

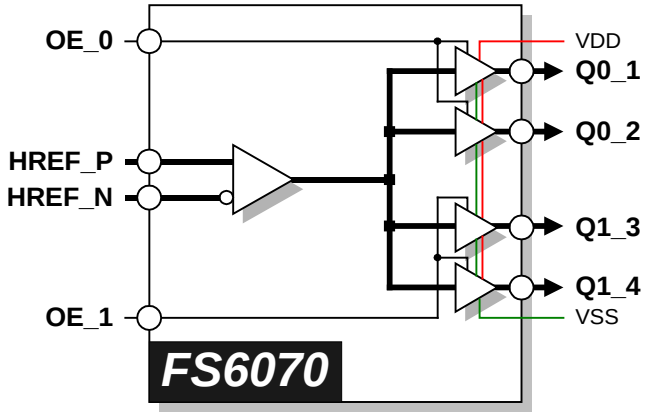


Table 1: Clock Enable Configuration

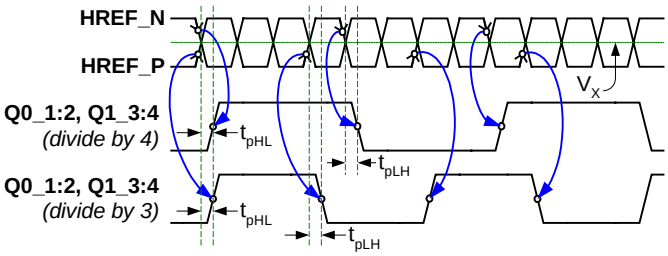
CONTROL			CLOCK OUTPUTS	
OE_0	OE_1	DIVSEL	Q0_1:2	Q1_3:4
0	0	X	Tristate	Tristate
0	1	0	Tristate	HREF ÷ 3
0	1	1	Tristate	HREF ÷ 4
1	0	0	HREF ÷ 3	Tristate
1	0	1	HREF ÷ 4	Tristate
1	1	0	HREF ÷ 3	HREF ÷ 3
1	1	1	HREF ÷ 4	HREF ÷ 4

Table 2: Pin Descriptions

Key: DI = Digital Input; DI^U = Input with Internal Pull-Up; DI_D = Input with Internal Pull-Down; DIO = Digital Input/Output; DO = Digital Output; P = Power/Ground; # = Active-low pin

PIN	TYPE	NAME	DESCRIPTION	
4	AI	HREF_P	HSTL input (true)	Differential Input
5	AI	HREF_N	HSTL input (complement)	
14	DO	Q0_1	LVTTL clock output	Output Bank 0
13	DO	Q0_2	LVTTL clock output	
12	DO	Q1_3	LVTTL clock output	Output Bank 1
11	DO	Q1_4	LVTTL clock output	
1	DI	DIVSEL	Divider selection control input	
8	DI	OE_0	Bank 0 output enable control; also used with DIVSEL, OE_1 to select dividers	
9	DI	OE_1	Bank 1 output enable control; also used with DIVSEL, OE_0 to select dividers	
2, 3, 15,16	P	VDD	3.3V power supply	
6, 7, 10	P	VSS	Ground	

Figure 3: Divide-by-3, Divide-by-4 Timing



ISO9001
QS9000

2.0 Electrical Specifications

Table 3: Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These conditions represent a stress rating only, and functional operation of the device at these or any other conditions above the operational limits noted in this specification is not implied. Exposure to maximum rating conditions for extended conditions may affect device performance, functionality, and reliability.

PARAMETER	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage (V_{SS} = ground)	V_{DD}	V_{SS}-0.5	7	V
Input Voltage, dc	V_I	V_{SS}-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	V_{SS}-0.5	V_{DD}+0.5	V
Input Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{IK}	-50	50	mA
Output Clamp Current, dc ($V_I < 0$ or $V_I > V_{DD}$)	I_{OK}	-50	50	mA
Storage Temperature Range (non-condensing)	T_S	-65	150	°C
Ambient Temperature Range, Under Bias	T_A	-55	125	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
Input Static Discharge Voltage Protection (MIL-STD 883E, Method 3015.7)			2	kV

CAUTION: ELECTROSTATIC SENSITIVE DEVICE

Permanent damage resulting in a loss of functionality or performance may occur if this device is subjected to a high-energy electrostatic discharge.

Table 4: Operating Conditions

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Supply Voltage	V_{DD}		3.135	3.3	3.465	V
Operating Temperature Range	T_A		0		70	°C
Load Capacitance	C_L	Q0_1:2, Q1_3:4	10		30	pF
Reference Frequency Range	f_{HREF}	C_L = 30pF			250	MHz
Input Signal Edge Rate				1.0		V/ns
Input Duty Cycle			40		60	%
Input High-Level Voltage	V_{IH}	Required HSTL signalling parameters	V_X + 0.1		1.2	V
Input Low-Level Voltage	V_{IL}		V_{SS} - 0.3		V_X - 0.1	V
Input Differential Cross Point Voltage	V_X		0.68		0.90	V

Table 5: DC Electrical Specifications

Unless otherwise stated, all power supplies = 3.465V, no load on any output, and ambient temperature range T_A = 0°C to 70°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical. Negative currents indicate current flows out of the device.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	MIN.	TYP.	MAX.	UNITS
Overall						
Supply Current, Dynamic, with Loaded Outputs	I_{DD}	f_{HREF} = 200.0MHz, f_{OUT} = 66.67MHz (divide-by-3) all supplies = 3.465V		45		mA
		f_{HREF} = 200.0MHz, f_{OUT} = 50.00MHz (divide-by-4); all supplies = 3.465V		35		
Supply Current, Static	I_{DDs}	HREF stopped either high or low		1		mA
HSTL Reference Input (HREF_P, HREF_N)						
High-Level Input Voltage	V_{IH}	See Table 4 for proper HSTL signal input levels	V_X + 0.1		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		V_X - 0.1	V
Differential Cross Point Voltage	V_X				2.2	V
Input Leakage Current	I_{IL}		-5		5	µA
LVTTL Digital Inputs (OE_0, OE_1, DIVSEL)						
High-Level Input Voltage	V_{IH}		2.0		V_{DD}+0.3	V
Low-Level Input Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input Leakage Current	I_{IL}		-5		5	µA
LVTTL Clock Outputs (Q0_1:2, Q1_3:4)						
High Level Output Source Current	$I_{OH\ min}$	V_{DD} = 3.135V, V_O = 1.0V	-33	-74		mA
	$I_{OH\ max}$	V_{DD} = 3.465V, V_O = 3.135V		-22	-33	
Low Level Output Sink Current	$I_{OL\ min}$	V_{DD} = 3.135V, V_O = 1.95V	30	90		mA
	$I_{OL\ max}$	V_{DD} = 3.465V, V_O = 0.4V		34	38	
Output Impedance	z_{OL}	Measured at 1.65V, output driving low	12	18	55	Ω
	z_{OH}	Measured at 1.65V, output driving high	12	22	55	
Tristate Output Current	I_{OZ}		-10		10	µA
Short Circuit Output Source Current	I_{OSH}	V_O = 0V; shorted for 30s, max.		-85		mA
Short Circuit Output Sink Current	I_{OSL}	V_O = 3.3V; shorted for 30s, max.		98		mA

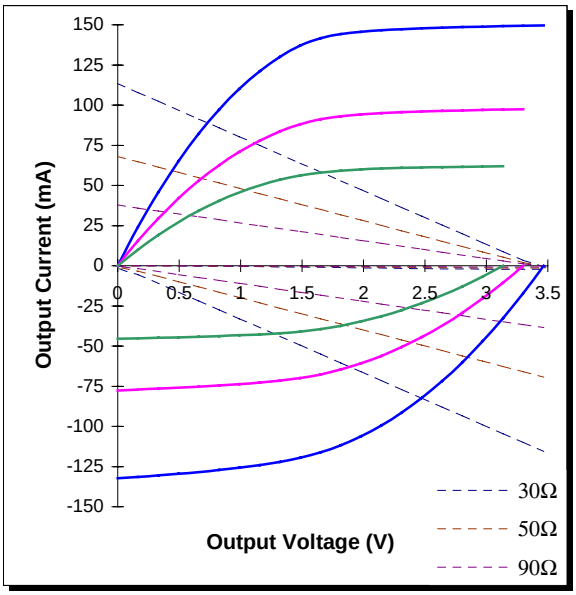
Table 6: AC Timing Specifications

Unless otherwise stated, all power supplies = 3.465V, no load on any output, and ambient temperature range T_A = 25°C. Parameters denoted with an asterisk (*) represent nominal characterization data and are not currently production tested to any specific limits. MIN and MAX characterization data are ±3σ from typical.

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION		MIN.	TYP.	MAX.	UNITS
Overall							
Propagation Delay	t_{pLH}, t_{pHL}			1.5	6.0	8.0	ns
Output Tristate Enable Delay *	t_{DZL}, t_{DZH}			1.0		10	ns
Output Tristate Disable Delay *	t_{DLZ}, t_{DHZ}			1.0		10	ns
LVTTL Clock Outputs (Q0_1:2, Q1_3:4)							
Duty Cycle *	d_t	Ratio of high pulse width to one clock period, measured at V_X	divide by 3	45	50.7	55	%
			divide by 4	45	49.5	55	
Output Skew *	$t_{sk(o)}$	One clock output relative to another at 1.5V, with both outputs at the same frequency, C_L = 30pF			90		ps
Rise Time *	$t_{r\ min}$	Measured at 0.4V – 2.4V; C_L = 10pF		1.0	1.2		ns
	$t_{r\ max}$	Measured at 0.4V – 2.4V; C_L = 30pF			1.7	2.0	
Fall Time *	$t_{f\ min}$	Measured at 2.4V – 0.4V; C_L = 10pF		1.0	1.0		ns
	$t_{f\ max}$	Measured at 2.4V – 0.4V; C_L = 30pF			1.8	2.0	

Table 7: Q0, Q1 Clock Outputs

Voltage (V)	Low Drive Current (mA)		Voltage (V)	High Drive Current (mA)	
	MIN.	MAX.		MIN.	MAX.
0.000	0.0	0.0	0.000	-45.5	-132.2
0.165	10.0	24.2	0.165	-45.2	-131.4
0.330	19.1	45.9	0.330	-44.9	-130.5
0.495	27.1	65.2	0.495	-44.5	-129.5
0.660	34.2	82.3	0.660	-44.2	-128.4
0.825	40.4	97.2	0.825	-43.8	-127.2
0.990	45.6	110.1	0.990	-43.3	-125.8
1.155	50.0	121.1	1.155	-42.8	-124.1
1.320	53.5	130.2	1.320	-42.1	-122.1
1.485	56.2	137.1	1.485	-41.0	-119.5
1.650	58.0	141.7	1.650	-39.5	-116.1
1.815	59.2	144.2	1.815	-37.4	-111.7
1.980	59.9	145.6	1.980	-34.7	-106.1
2.145	60.5	146.5	2.145	-31.5	-99.3
2.310	60.9	147.2	2.310	-27.7	-91.4
2.475	61.2	147.7	2.475	-23.4	-82.2
2.640	61.4	148.2	2.640	-18.4	-71.8
2.805	61.7	148.5	2.805	-12.9	-60.1
2.970	61.8	148.8	2.970	-6.7	-47.1
3.135	62.0	149.1	3.135	0.0	-32.8
3.300		149.4	3.300		-17.1
3.465		149.6	3.465		0.0



Data in this table represents nominal characterization data only

3.0 Package Information

Table 8: 16-pin SOIC (0.150") Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.061	0.068	1.55	1.73
A1	0.004	0.0098	0.102	0.249
A2	0.055	0.061	1.40	1.55
B	0.013	0.019	0.33	0.49
C	0.0075	0.0098	0.191	0.249
D	0.386	0.393	9.80	9.98
E	0.150	0.157	3.81	3.99
e	0.050 BSC		1.27 BSC	
H	0.230	0.244	5.84	6.20
h	0.010	0.016	0.25	0.41
L	0.016	0.035	0.41	0.89
Θ	0°	8°	0°	8°

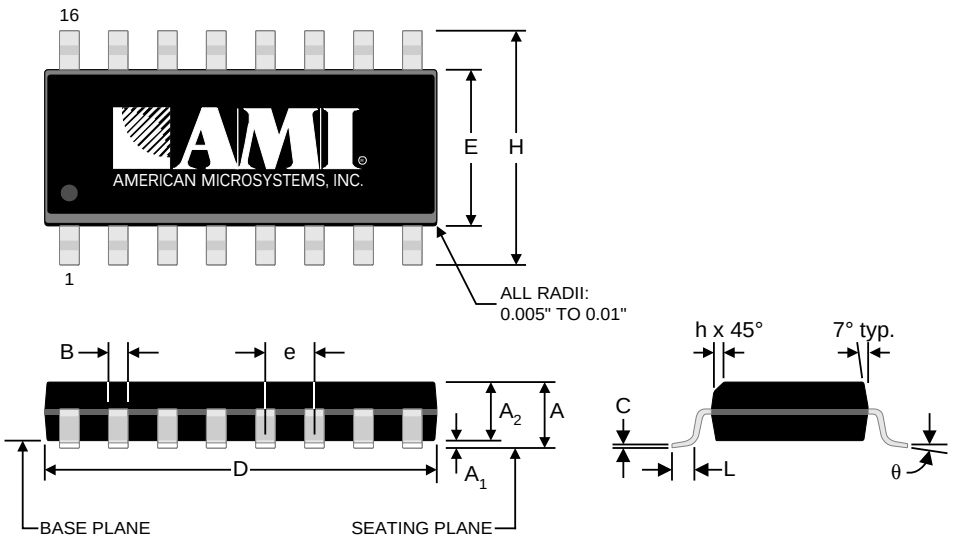


Table 9: 16-pin SOIC (0.150") Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	Θ_{JA}	Air flow = 0 m/s	109	°C/W
Lead Inductance, Self	L_{11}	Corner lead	4.0	nH
		Center lead	3.0	
Lead Inductance, Mutual	L_{12}	Any lead to any adjacent lead	0.4	nH
Lead Capacitance, Bulk	C_{11}	Any lead to V_{SS}	0.5	pF

4.0 Package Information

Table 10: 16-pin TSSOP (4.4mm) Package Dimensions

	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	-	0.0472	-	1.20
A_1	0.002	0.006	0.05	0.15
A_2	0.0315	0.041	0.80	1.05
b	0.0075	0.0118	0.19	0.30
c	0.0035	0.0079	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.252 BSC		6.40 BSC	
E_1	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
S	0.0079	-	0.20	-
L	0.0177	0.0295	0.45	0.75
θ_1	0°	8°	0°	8°
θ_2	12° REF		12° REF	
θ_3	12° REF		12° REF	

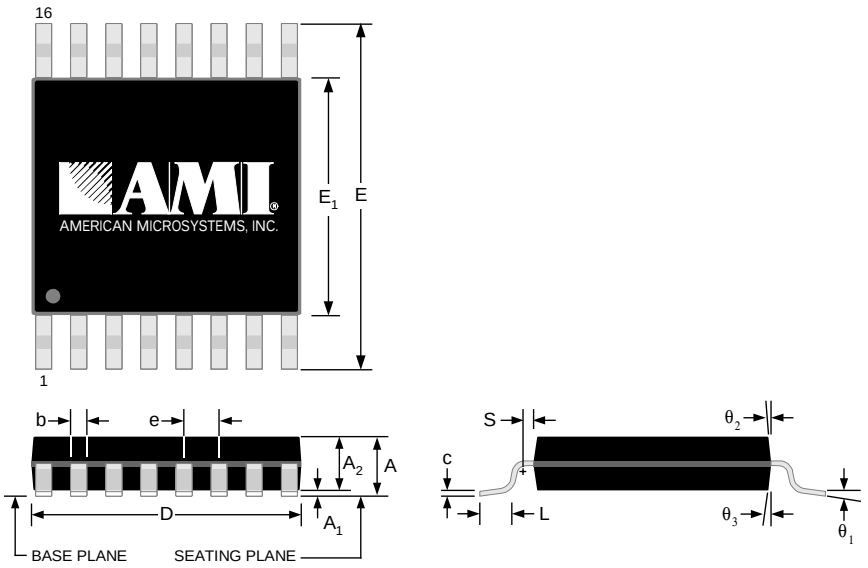


Table 11: 16-pin TSSOP (4.4mm) Package Characteristics

PARAMETER	SYMBOL	CONDITIONS/DESCRIPTION	TYP.	UNITS
Thermal Impedance, Junction to Free-Air	θ_{JA}	Air flow = 0 m/s	89	°C/W
Lead Inductance, Self	L_{11}	Corner lead plus wire	2.361	nH
		Center lead plus wire	1.443	
Lead Inductance, Mutual	L_{12}	Corner lead plus wire, to first adjacent lead	0.754	nH
		Center lead plus wire, to first adjacent lead	0.367	
	L_{13}	Corner lead plus wire, to next adjacent lead	0.293	
		Center lead plus wire, to next adjacent lead	0.249	
Lead Capacitance, Bulk	C_{11}	Any corner lead plus wire to V_{SS}	0.375	pF
		Any center lead plus wire to V_{SS}	0.254	
Lead Capacitance, Mutual	C_{12}	Any corner lead plus wire to first adjacent lead	0.137	pF
		Any center lead plus wire to first adjacent lead	0.053	
	C_{13}	Any corner lead plus wire to next adjacent lead	0.008	
		Any center lead plus wire to next adjacent lead	0.006	

5.0 Ordering Information

Table 12: Device Ordering Codes

DEVICE NUMBER	ORDERING CODE	PACKAGE TYPE	OPERATING TEMPERATURE RANGE	SHIPPING CONFIGURATION
FS6070-01	13710-801	16-pin (0.150") SOIC	0° C to 70° C (Commercial)	Tape and Reel
	13710-201	16-pin (4.4mm) TSSOP		

6.0 Revision Information

DATE	PAGE	DESCRIPTION
7/31/00	-	This document contains information on a new product. Specifications and information herein are subject to change without notice.
8/1/00	1	Flipped HREF_P, HREF_N signals in timing diagram, revised DC electrical specs.
10/18/00	6, 7	Added 16-pin TSSOP
	-	This document contains information on a preproduction product. Specifications and information herein are subject to change without notice.

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