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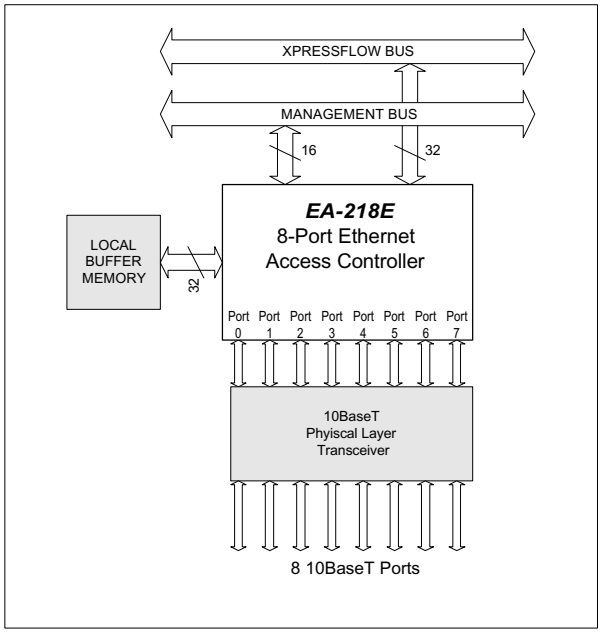
EA218E – 8-Port Ethernet Access Controller

XpressFlow 2020 Ethernet Routing Switch Chipset

Distinctive Characteristics

- 8 10Mbps Ethernet Access Ports
  - ◊ Direct interface with 10BaseT transceiver
- 0.5 micron 3.3 Volt CMOS process
- 352-BGA package
- Operating frequency
  - ◊ -33 33 MHz maximum
  - ◊ -40 40 MHz maximum
  - ◊ -50 50 MHz maximum
  - ◊ -66 66.66 MHz maximum
- 32-bit Local Buffer Memory Interface
  - ◊ Supports 128k to 1M bytes
  - ◊ Utilize high performance 32-bit Synchronous Burst SRAM
- Hardware assisted Buffer and Queue Management
- 16-bit Management Bus I/O Interface
  - ◊ Allows host to access Control Registers & Local Buffer Memory
  - ◊ Big and Little Endian CPUs
  - ◊ Direct interface to standard microprocessors, including 386, 486 families and Motorola MPC series embedded processors
- 32-bit *XpressFlow* Bus Interface
  - ◊ Uses Granule for frame transferring between Access Controllers
- Unicast, multicast, and broadcast frames
  - ◊ Also detects IEEE 802.3X MAC Control frames
- Works together with SC-220 XpressFlow Engine
  - ◊ Forwards frames at full line-rate
  - ◊ Distributed Flow Caching™ to reduce frame forwarding latency
- Half and Full Duplex operation
- Programmable Flow Control
  - ◊ Jam Collision for Half Duplex Mode
  - ◊ Transmit Flow Control Frame for IEEE 802.3x Full Duplex Mode

Supports Store-&-Forward frame forward-



Block Diagram-
EA218E 8-Port Ethernet Access Controller

General Description

The EA-218E provides eight 10Mbps Ethernet network access interface ports.

The EA-218E provides the Ethernet MAC protocols, handles the local buffer memory interface and management, arbitrates among multiple priority queues, and interfaces with the *XpressFlow* Engine and other Access Controllers through the *XpressFlow* message passing protocol.

Related Components:

- *SC220* – XpressFlow Engine
- *EA218* – 6-port 10 + 2-port 10/100 Ethernet Access Controller
- *EA234* – 4-port 10/100Mbps Ethernet Access Controller

ing mode

Characteristics Continue

- ◊ Automatically selects the optimized mode for forwarding
- ◊ Allows manual frame forwarding mode selection override

♦ Multi-Media ready with QoS supports
- ◊ Four frame transmission priority queues

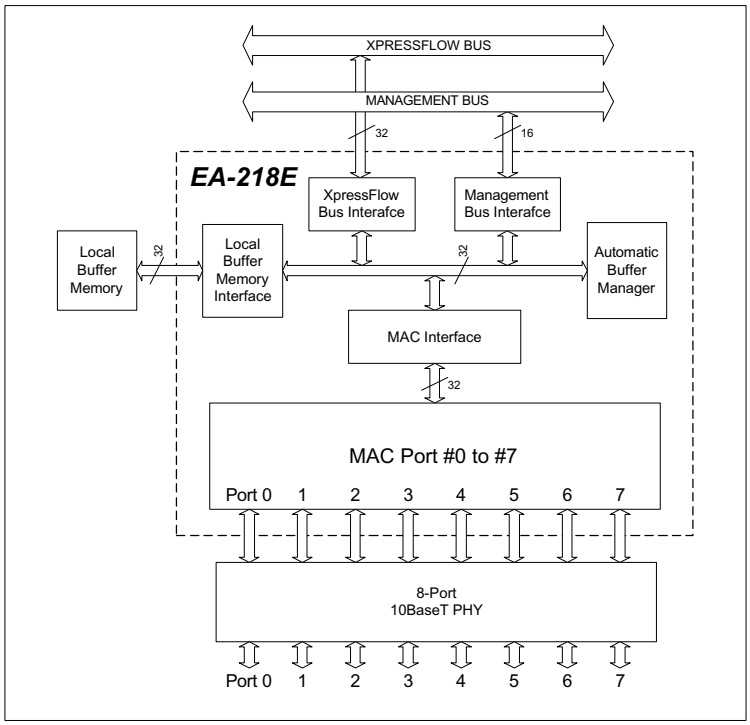
♦ Complies with IEEE 802.1 Bridge Standard
- ◊ Assigns one unique MAC Address for each port

♦ VLAN ID Tagging & Stripping
- ◊ Auto padding if necessary after stripping

♦ Automatic retry frame transmission
- ◊ Transmit collision
- ◊ Transmit buffer under-run

♦ Automatic receive filtering for bad frames for Store & Forward Mode
- ◊ Bad FCS
- ◊ Short events or frames under 64 bytes
- ◊ Long events or frames over 1518/1522 bytes

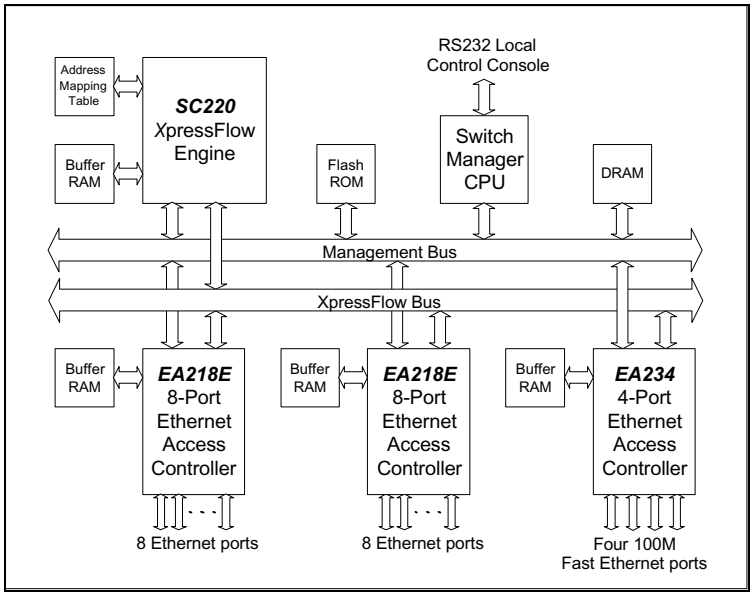
♦ Automatic statistic collection for RMON



Block Diagram –
EA218E 8-Port Ethernet Access Controller

Typical Application:

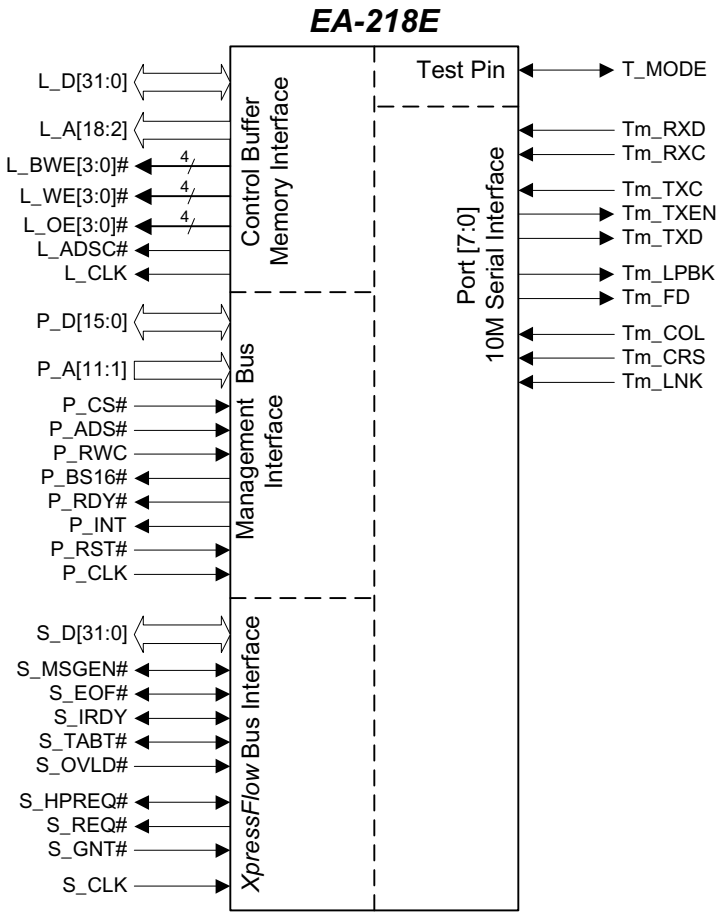
◊ A 16-port Ethernet Switch with 4-Fast Ethernet



System Block Diagram --
16-Port Ethernet Switch with 4 Fast Ethernet Up-Links

1. PIN ASSIGNMENT

1.1 Logic Symbol



1.2 Pin Assignment (Preliminary)

Note: # Active low signal
Input Input signal
In-ST Input signal with Schmitt-Trigger
Output Output signal (Tri-State driver)
Out-OD Output signal with Open-Drain driver
I/O-TS Input & Output signal with Tri-State driver
I/O-OD Input & Output signal with Open-Drain driver
5VT Input with 5V Tolerance
① Output signal with programmable polarity.
② Input or output pins with weak internal pull up resistors (50k to 100k Ohms each)
③ These pins are reserved for internal use only. They should be left unconnected.

Pin No(s).	Symbol	Type	Max I_{OL} / I_{OH}	Name and Functions
Management Bus Interface				
J25,K26,L24,K25,L26, M24,L25,M26,N24,M25, P24,N26,N25,R24,P26, P25	P_D[15:0]	TTL I/O-TS (5VT)	16mA	Management Bus – Data Bit [15:0]
C26,D24,C25,E24,D26, D25,F24,E26,E25,G24, F26	P_A[11:1]	TTL In (5VT)		Management Bus – Address Bit [11:1]
F25	P_ADS#	TTL In (5VT)		Management Bus – Address Strobe
H25	P_RWC	TTL In (5VT)		Management Bus – Read/Write Control
J24	P_RDY#	TTL Out-OD	16mA	Management Bus – Data Ready
G25	P_BS16#	TTL Out-OD	16mA	Management Bus – 16 bit Data Bus
G26	P_CS#	TTL In (5VT)		Management Bus – Chip Select
H26	P_INT ①	CMOS Output	4mA	Management Bus – Interrupt Request
J26	P_RST#	TTL In-ST (5VT)		Management Bus – Master Reset
K24	P_CLK	TTL In (5VT)		Management Bus – Bus Clock
XpressFlow Bus Interface				
C23,A23,B22,C22,A22	S_D[31:27] / P_C[0:4]	CMOS I/O-TS	12 mA	*XpressFlow* Bus – Data Bit [31:27] or Management Bus Interface Configuration bit [0:4]
B21,D20,C21,A21,B20, A20,C20,B19,A19,C19, B18,A18,B17,C18,A17, D17,B16,C17,A16,B15, A15,C16,B14,D15,A14, C15,B13	S_D[26:0]	CMOS I/O-TS	12mA	*XpressFlow* Bus – Data Bit [26:0]
B12	S_MSGEN#	CMOS I/O-TS	12 mA	*XpressFlow* Bus – Message Envelope
A12	S_EOF#	CMOS I/O-TS	12mA	*XpressFlow* Bus – End of Frame
C14	S_IRDY	CMOS I/O-TS	12 mA	*XpressFlow* Bus – Initiator Ready
C13	S_TABT#	CMOS I/O-OD	12 mA	*XpressFlow* Bus – Target Abort
B23	S_HPREQ#	CMOS I/O-OD	12mA	*XpressFlow* Bus – High Priority Request
A24	S_REQ#	CMOS Output	4mA	*XpressFlow* Bus – Bus Request to SC201
B24	S_GNT#	CMOS Input		*XpressFlow* Bus – Bus Grant from SC201
A13	S_OVLD#	CMOS Input		*XpressFlow* Bus – Bus Overload
D13	S_CLK	CMOS Input		*XpressFlow* Bus – Clock

Pin No(s).	Symbol	Type		Name and Functions
Control Buffer Memory Interface				
M4,N2,L3,M1,M2,L1,K3, L2,K4,K1,J3,K2,J1,J2, H3,H1,H2,G3,G1,G2,F1,F3,F 2,E1,E3,E2,D1,D3,D2,C1,C2, B1	L_D[31:0]	TTL I/O-TS ②	8mA	Local Memory Bus – Data Bit [31:0]
A6,B6,C8,A7,D8,D7,C9, A8,B8,A9,C10,B9,D10, A10,C11,B10,A11	L_A[18:2]	CMOS Output	8mA	Local Memory Bus – Address Bit [17:2]
C7	L_A[19] / L_OE[3]#	CMOS Output	8mA	Local Memory Bus – Address Bit [19] or Memory Read Chip Select [3]
D5,A5,A3	L_OE[2:0]#	CMOS Output	2mA	Local Memory Read Chip Select [2:0]
D7,E4,B5,C4	L_WE[3:0]#	CMOS Output	2mA	Local Memory Write Chip Select [3:0]
C6,B4,A4,C5	L_BWE[3:0]#	CMOS Output	8mA	Local Memory Byte Write Enable, Byte [3:0]
B3	L_ADSC#	CMOS Output	8mA	Local Memory Controller Address Status
G4	L_CLK	CMOS Output	8mA	Local Memory Clock input
Ethernet Access Port cont. [7:0]				
AF20,AE17,AD12,AD9, AC2,T25	T[7:2]_RXD	TTL In (5VT) ②		Receive Data – (one for each 10Mbps Serial Interface Port)
AC25,AF6	T[1:0]_RXD	TTL In (5VT)		
AD19,AD16,AE14,AF10,AC2 1U24	T[7:2]_RXC	TTL In (5VT) ②		Receive Clock – (one for each 10Mbps Serial Interface Port)
AC24,AE7	T[1:0]_RXC	TTL In (5VT)		
AF18,AD14,AE12,AF8, W2,AA25,AE22,AD1	T[7:0]_TXC	TTL In (5VT)		Transmit Clock – (one for each 10Mbps Serial Interface Port)
AE19,AF15,AF12,AD8, W1,AA24	T[7:2]_TXEN	CMOS Out ②	4mA	Transmit Enable – (one for each 10Mbps Serial Interface Port)
AF22,AF2	T[1:0]_TXEN	CMOS Output		
AE20,AF16,AF13,AE10, Y1,W25	T[7:2]_TXD	CMOS Out ②	4mA	Transmit Data – (one for each 10Mbps Serial Interface Port)
AF23,AE4	T[1:0]_TXD	CMOS Output		
AD18,AD15,AE13,AF9, Y2,Y26	T[7:2]_LPBK ①	CMOS Out ②	2mA	Loop Back Enable – (one for each 10Mbps Serial Interface Port)
AE23,AF3	T[1:0]_LPBK ①	CMOS Output		
AF19,AE16,AD11,AE9, V3,AA26	T[7:2]_FD ①	CMOS Out ②	2mA	Full Duplex Mode – (one for each 10Mbps Serial Interface Port)
AD21,AE3	T[1:0]_FD ①	CMOS Output		
AD17,AE15,AF11,AE8, V1,AB26	T[7:2]_COL	TTL In (5VT) ②		Collision Detected – (one for each 10Mbps Serial Interface Port)
AD20,AC23	T[1:0]_COL	TTL In (5VT)		
AE18,AD13,AD10,AD7, U3,AB24,	T[7:2]_CRS	TTL In (5VT) ②		Carrier Sense – (one for each 10Mbps Serial Interface Port)
AF21,AD2	T[1:0]_CRS	TTL In (5VT)		
AF17,AF14,AE11,AF7, V2,AB25,	T[7:2]_LNK ①	TTL In (5VT) ②		Link Status – (one for each 10Mbps Serial Interface Port)
AE21,AB3	T[1:0]_LNK ①	TTL In (5VT)		

Pin No(s).	Symbol	Type	Max I_{OL} / I_{OH}	Name & Functions
Test Facility				
A25	T_MODE	CMOS I/O-TS ②	2mA	Test Pin – Set Test Mode upon Reset, and provides test status output during test mode
N1,M3,P2,P1,N3,R2,P3,R1,T2R3,T1,R4,U2,T3,U1,U4	T_D[15:10] ③	CMOS Output	4mA	Test Pins – Reserved for internal use only

Pin No(s).	Symbol	Type	Name & Functions
Power Pins			
D6,D11,D16,D21,F4, F23,L4,L23,T4,T23,AA4,AA23 AC6,AC11,AC16,AC21	VDD	Power	+3.3 Volt DC Supply
A1,A2,A26,B2,B25,B26, C3,C24,D4,D9,D14,D19,D23, H4,J23,N4,P23,V4,W23,AC4, AC8,AC13, AC18,AC23,AD3,AD24, AE1,AE2,AE25,AF1, AF25	VSS	Power	Ground

1.3 ***Pin Reference Table:*** *(352 pin BGA)*

Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
F26	P_A[1]	C18	S_D[13]	E3	L_D[7] ②	V1	T3_COL ②	T2	T_D[7] ③
G24	P_A[2]	B17	S_D[14]	E1	L_D[8] ②	V3	T3_FD ①②	R1	T_D[8] ③
E25	P_A[3]	A18	S_D[15]	F2	L_D[9] ②	Y2	T3_LPBK ①②	P3	T_D[9] ③
E26	P_A[4]	B18	S_D[16]	F3	L_D[10] ②	Y1	T3_TXD ②	R2	T_D[10] ③
F24	P_A[5]	C19	S_D[17]	F1	L_D[11] ②	W1	T3_TXEN ②	N3	T_D[11] ③
D25	P_A[6]	A19	S_D[18]	G2	L_D[12] ②	W2	T3_TXC	P1	T_D[12] ③
D26	P_A[7]	B19	S_D[19]	G1	L_D[13] ②	AC1	T3_RXC ②	P2	T_D[13] ③
E24	P_A[8]	C20	S_D[20]	G3	L_D[14] ②	AC2	T3_RXD ②	M3	T_D[14] ③
C25	P_A[9]	A20	S_D[21]	H2	L_D[15] ②	AF7	T4_LNK ①②	N1	T_D[15] ③
D24	P_A[10]	B20	S_D[22]	H1	L_D[16] ②	AD7	T4_CRS ②		
C26	P_A[11]	A21	S_D[23]	H3	L_D[17] ②	AE8	T4_COL ②	D6	VDD
F25	P_ADS#	C21	S_D[24]	J2	L_D[18] ②	AE9	T4_FD ①②	D11	VDD
G26	P_CS#	D20	S_D[25]	J1	L_D[19] ②	AF9	T4_LPBK ①②	D16	VDD
H25	P_RWC	B21	S_D[26]	K2	L_D[20] ②	AE10	T4_TXD ②	D21	VDD
G25	P_BS16#	A22	S_D[27] / P_C[4]	J3	L_D[21] ②	AD8	T4_TXEN ②	F4	VDD
J24	P_RDY#	C22	S_D[28] / P_C[3]	K1	L_D[22] ②	AF8	T4_TXC	F23	VDD
J26	P_RST#	B22	S_D[29] / P_C[2]	K4	L_D[23] ②	AF10	T4_RXC ②	L4	VDD
H26	P_INT ①	A23	S_D[30] / P_C[1]	L2	L_D[24] ②	AD9	T4_RXD ②	L23	VDD
K24	P_CLK	C23	S_D[31] / P_C[0]	K3	L_D[25] ②	AE11	T5_LNK ①②	T4	VDD
P25	P_D[0]			L1	L_D[26] ②	AD10	T5_CRS ②	T23	VDD
P26	P_D[1]	A11	L_A[2]	M2	L_D[27] ②	AF11	T5_COL ②	AA4	VDD
R24	P_D[2]	B10	L_A[3]	M1	L_D[28] ②	AD11	T5_FD ①②	AA23	VDD
N25	P_D[3]	C11	L_A[4]	L3	L_D[29] ②	AE13	T5_LPBK ①②	AC6	VDD
N26	P_D[4]	A10	L_A[5]	N2	L_D[30] ②	AF13	T5_TXD ②	AC11	VDD
P24	P_D[5]	D10	L_A[6]	M4	L_D[31] ②	AF12	T5_TXEN ②	AC16	VDD
M25	P_D[6]	B9	L_A[7]			AE12	T5_TXC	AC21	VDD
N24	P_D[7]	C10	L_A[8]	AB3	T0_LNK ①	AE14	T5_RXC ②	A1	GND
M26	P_D[8]	A9	L_A[9]	AD2	T0_CRS	AD12	T5_RXD ②	A2	GND
L25	P_D[9]	B8	L_A[10]	AC3	T0_COL	AF14	T6_LNK ①②	A26	GND
M24	P_D[10]	A8	L_A[11]	AE3	T0_FD ①	AD13	T6_CRS ②	B2	GND
L26	P_D[11]	C9	L_A[12]	AF3	T0_LPBK ①	AE15	T6_COL ②	B25	GND
K25	P_D[12]	B7	L_A[13]	AE4	T0_TXD	AE16	T6_FD ①②	B26	GND
L24	P_D[13]	D8	L_A[14]	AF2	T0_TXEN	AD15	T6_LPBK ①②	C3	GND
K26	P_D[14]	A7	L_A[15]	AD1	T0_TXC	AF16	T6_TXD ②	C24	GND
J25	P_D[15]	C8	L_A[16]	AE7	T0_RXC	AF15	T6_TXEN ②	D4	GND
		B6	L_A[17]	AF6	T0_RXD	AD14	T6_TXC	D9	GND
D13	S_CLK	A6	L_A[18]	AE21	T1_LNK ①	AD16	T6_RXC ②	D14	GND
A13	S_OVLD#	C7	L_A[19] / OE[3]#	AF21	T1_CRS	AE17	T6_RXD ②	D19	GND
B23	S_HPREQ#	D5	L_OE[2]#	AD20	T1_COL	AF17	T6_LNK ①②	D23	GND
A24	S_REQ#	A5	L_OE[1]#	AD21	T1_FD ①	AE18	T7_CRS ②	H4	GND
B24	S_GNT#	A3	L_OE[0]	AE23	T1_LPBK ①	AD17	T7_COL ②	J23	GND
B12	S_MSGEN#	D7	L_WE[3]#	AF23	T1_TXD	AF19	T7_FD ①②	N4	GND
A12	S_EOF#	E4	L_WE[2]#	AF22	T1_TXEN	AD18	T7_LPBK ①②	P23	GND
C14	S_IRDY	B5	L_WE[1]#	AE22	T1_TXC	AE20	T7_TXD ②	V4	GND
C13	S_TABT#	C4	L_WE[0]#	AC24	T1_RXC	AE19	T7_TXEN ②	W23	GND
B13	S_D[0]	C6	L_BWE[3]#	AC25	T1_RXD	AF18	T7_TXC	AC4	GND
C15	S_D[1]	B4	L_BWE[2]#	AB25	T2_LNK ①②	AD19	T7_RXC ②	AC8	GND
A14	S_D[2]	A4	L_BWE[1]#	AB24	T2_CRS ②	AF20	T7_RXD ②	AC13	GND
D15	S_D[3]	C5	L_BWE[0]#	AB26	T2_COL ②			AC18	GND
B14	S_D[4]	B3	L_ADSC#	AA26	T2_FD ①②	A25	T_MODE ②	AC23	GND
C16	S_D[5]	G4	L_CLK	Y26	T2_LPBK ①②			AD3	GND
A15	S_D[6]	B1	L_D[0] ②	W25	T2_TXD ②	U4	T_D[0] ③	AD24	GND
B15	S_D[7]	C2	L_D[1] ②	AA24	T2_TXEN ②	U1	T_D[1] ③	AE1	GND
A16	S_D[8]	C1	L_D[2] ②	AA25	T2_TXC	T3	T_D[2] ③	AE2	GND
C17	S_D[9]	D2	L_D[3] ②	U24	T2_RXC ②	U2	T_D[3] ③	AE25	GND
B16	S_D[10]	D3	L_D[4] ②	T25	T2_RXD ②	R4	T_D[4] ③	AF1	GND
D17	S_D[11]	D1	L_D[5] ②	V2	T3_LNK ①②	T1	T_D[5] ③	AF25	GND
A17	S_D[12]	E2	L_D[6] ②	U3	T3_CRS ②	R3	T_D[6] ③		

Note: ① Output signals with programmable polarity.

② Input or output pins with weak internal pull up resistors (50k to 100k Ohms each)

③ These pins are reserved for internal use only. They should be left unconnected.

2. FUNCTIONAL DESCRIPTION

2.1 Local Memory (Local Buffer Memory) Interface

- Uses industry standard Synchronous Burst Mode SRAM up to 1M bytes
  - 32k x 32, 64k x 32, 128k x 32, or 256k x 32
- Provides separate Read and Write Chip Selects (L_OE[3:0]# and L_WE[3:0]#) for each memory chip
- Supports back to back Read or Write operations across memory chips

2.1.1 Pin Description

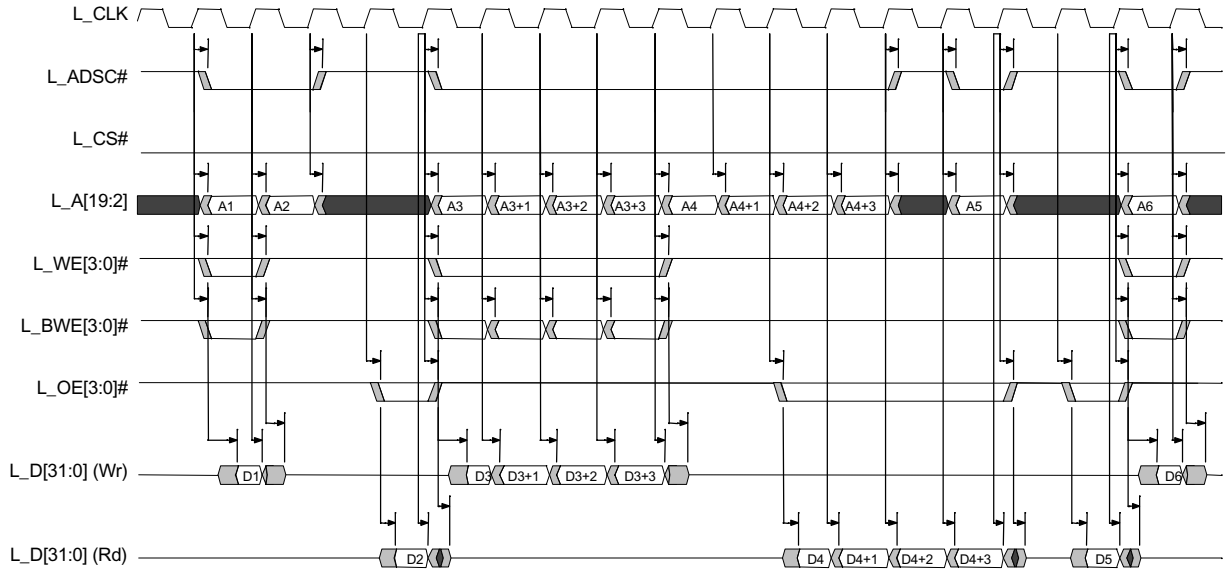
Symbol	Type	Name and Functions
L_D[31:0] ②	TTL I/O-TS	***Local Memory Data Bus Bit [31:0]*** – a 32-bit synchronous data bus.
L_A[18:2]	CMOS Output	***Local Memory Address Bus Bit [18:2]*** – Bit [18:2] of a synchronous address bus. The memory address is sampled when L_CS# is enabled and L_ADSC# is asserted.
L_A[19] / L_OE[3]#	CMOS Output	***Local Memory Address Bus Bit [19] or Local Memory Read Chip Select [3]*** – Depends on memory configuration, this pin can be used as the Local Memory Address Bit [19] or as the Local Memory Read Chip Select [3].
L_OE[2:0]#	CMOS Output	***Local Memory Read Chip Select [2:0]*** – allows up to read one of the 4 banks of memory.
L_WE[3:0]#	CMOS Output	***Local Memory Write Chip Select [3:0]*** – allows up to write one of the 4 banks of memory.
L_BWE[3:0]#	CMOS Output	***Local Memory Byte Write Enable [3:0]*** – use to write individual bytes.
L_ADSC#	CMOS Output	***Local Memory Controller Address Status*** – to load a new address.
L_CLK	CMOS Output	***Local Memory Clock*** – a synchronous clock to memory devices.
L_D[31:0]	TTL I/O-TS	***Local Memory Data Bus Bit [31:0]*** – a 32-bit synchronous data bus.
L_A[18:2]	CMOS Output	***Local Memory Address Bus Bit [18:2]*** – Bit [17:2] of a synchronous address bus. The memory address is sampled when L_CS# is enabled and L_ADSC# is asserted.
L_A[19] / L_WE[3]#	CMOS Output	***Local Memory Address Bus Bit [19] or Local Memory Write Chip Select [3]*** – Depends on memory configuration, this pin can be used as the Local Memory Address Bit [19] or as the Local Memory Write Chip Select [3].
L_WE[2:0]#	CMOS Output	***Local Memory Write Chip Select [2:0]*** – allows up to write one of the 4 banks of memory.
L_OE[3:0]#	CMOS Output	***Local Memory Read Chip Select [3:0]*** – allows up to read one of the 4 banks of memory.
L_BWE[3:0]#	CMOS Output	***Local Memory Byte Write Enable [3:0]*** – use to write individual bytes.
L_ADSC#	CMOS Output	***Local Memory Controller Address Status*** – to load a new address.
L_CLK	CMOS Output	***Local Memory Clock*** – a synchronous clock to memory devices.

Note: ② These pins have weak internal pull up resistors (50k to 100k Ohms each).

2.1.2 Supported Memory Configurations

RAM Chip Size	# of RAM Chips	Total Buffer Memory Size	Read/Write Chip Select and High Address Bits							
			Chip #3		Chip #2		Chip #1		Chip #0	
			L_WE[3]#	L_A[19] / L_OE[3]#	L_WE[2]#	L_OE[2]#	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
32k x 32	1	128k bytes	----	----	----	----	----	----	L_WE[0]#	L_OE[0]#
	2	256k bytes	----	----	----	----	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
	4	512k bytes	L_WE[3]#	L_OE[3]#	L_WE[2]#	L_OE[2]#	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
64k x 32	1	256k bytes	----	----	----	----	----	----	L_WE[0]#	L_OE[0]#
	2	512k bytes	----	----	----	----	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
	4	1M bytes	L_WE[3]#	L_OE[3]#	L_WE[2]#	L_OE[2]#	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
128k x32	1	512k bytes	----	----	----	----	----	----	L_WE[0]#	L_OE[0]#
	2	1M bytes	----	----	----	----	L_WE[1]#	L_OE[1]#	L_WE[0]#	L_OE[0]#
256k x32	1	1M bytes	----	L_A[19]	----	----	----	----	L_WE[0]#	L_OE[0]#

2.1.3 Bus Cycle Waveforms



Typical Local Memory Access Operations

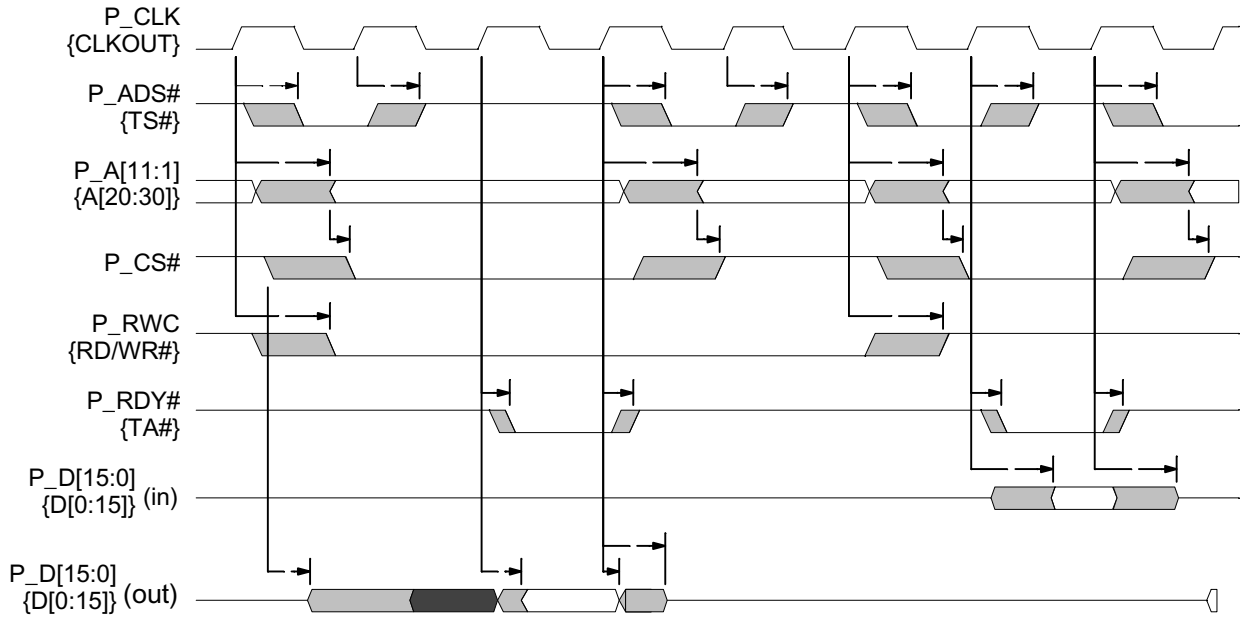
2.2 Processor Bus Interface

- Supports various industry standard micro-processors including:
  - ◊ Intel 186, 386, and 486 family or equivalent
  - ◊ Motorola MPC series embedded processors
- Easily adapts to other industry standard CPUs
- Provides separate Address and Data bus
- Supports Big & Little Endian byte ordering
- Supports 16-bit Data Bus
- Supports early RDY cycle
  - ◊ Meets timing requirement for Intel/AMD 186 family processors
- Supports 1X or 2X CPU Clock
  - ◊ 2X CPU Clock for 386 family processors
- Provides a single interrupt signal to Switch Manager CPU

2.2.1 Pin Description

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and Functions</th></tr>
<tr><td>P_C[4:0]</td><td>CMOS Input</td><td>Processor Configuration bit [4:0]: – During the Reset Cycle, the P_C[4:0] pins provides the processor configuration. By using external weak pull-up or -down resistors, they define the External Management Bus Interface Configuration. These inputs are sampled at the trailing edge of the Reset cycle.
C[0] – Defines the CPU Clock input is 1X or 2X clock
C[1] – Selects either Big or Little Endian byte ordering
C[2] – Defines the polarity of the P_RWC (Rd/Wr Control) input
C[3] – Defines the CPU Bus width – For EA-208, it is default to 16-bit CPU Bus interface, and the setting of this bit is ignored.
C[4] – Defines the timing relationship between P_RDY and P_D[15:0] valid. If C[4] is High, the P_D[15:0] are valid along in the same clock period as P_RDY is asserted. If C[4] is Low, the P_RDY is asserted one clock period <u>early</u> ahead of the P_D[15:0] are valid.
<table>
<tr><th></th><th>C[0]
CPU Clock</th><th>C[1]
Byte Order</th><th>C[2]
RWC</th><th>C[3]
Bus Size</th><th>C[4]
RDY Timing</th></tr>
<tr><td>Lo</td><td>1X Clock</td><td>Little Endian</td><td>P_R/W#</td><td>n/a</td><td>Normal</td></tr>
<tr><td>Hi</td><td>2x Clock</td><td>Big Endian</td><td>P_W/R#</td><td>n/a</td><td>Early</td></tr>
</table>
After RESET, these pins are used as XpressFlow Bus Data bit [31:27].</td></tr>
<tr><td>P_A[11:1]</td><td>TTL In (5VT)</td><td>Address Bus Bit [11:1] – I/O port address</td></tr>
<tr><td>P_D[15:0]</td><td>TTL I/O-TS (5VT)</td><td>Data Bus Bit [15:0] – a 16-bit synchronous data bus.</td></tr>
<tr><td>P_ADS#</td><td>TTL In (5VT)</td><td>Address Strobe – indicates valid address is on the bus</td></tr>
<tr><td>P_RWC</td><td>TTL Input (5VT)</td><td>Read/Write Control – indicates the current bus cycle is a read or write cycle. C[1] defines the polarity of this signal during the Reset cycle.
C[1]=Low P_R/W# is used for PowerPC or other similar processors.
C[1]=High P_W/R# is used for 386, 486 or other similar processors</td></tr>
<tr><td>P_RDY#</td><td>TTL Out-OD</td><td>Data Ready – timing indicates for bus data valid</td></tr>
<tr><td>P_BS16#</td><td>TTL Out-OD</td><td>Bus Size 16 – response to bus master that the EA208 only supports 16-bit data bus width.</td></tr>
<tr><td>P_CS#</td><td>TTL Input (5VT)</td><td>Chip Select – indicates the XpressFlow Engine is the target for the current bus operation.</td></tr>
<tr><td>P_INT ①</td><td>CMOS Output</td><td>Interrupt Request to Switch Manager CPU The polarity of this signal output is programmable via chip configuration register.</td></tr>
<tr><td>P_RST#</td><td>TTL In-ST (5VT)</td><td>CPU Reset – Synchronous reset Input from Switch Manager CPU</td></tr>
<tr><td>P_CLK</td><td>TTL In (5VT)</td><td>CPU Clock – 2X Clock for 386 family, and 1X Clock for the others</td></tr>
</table>

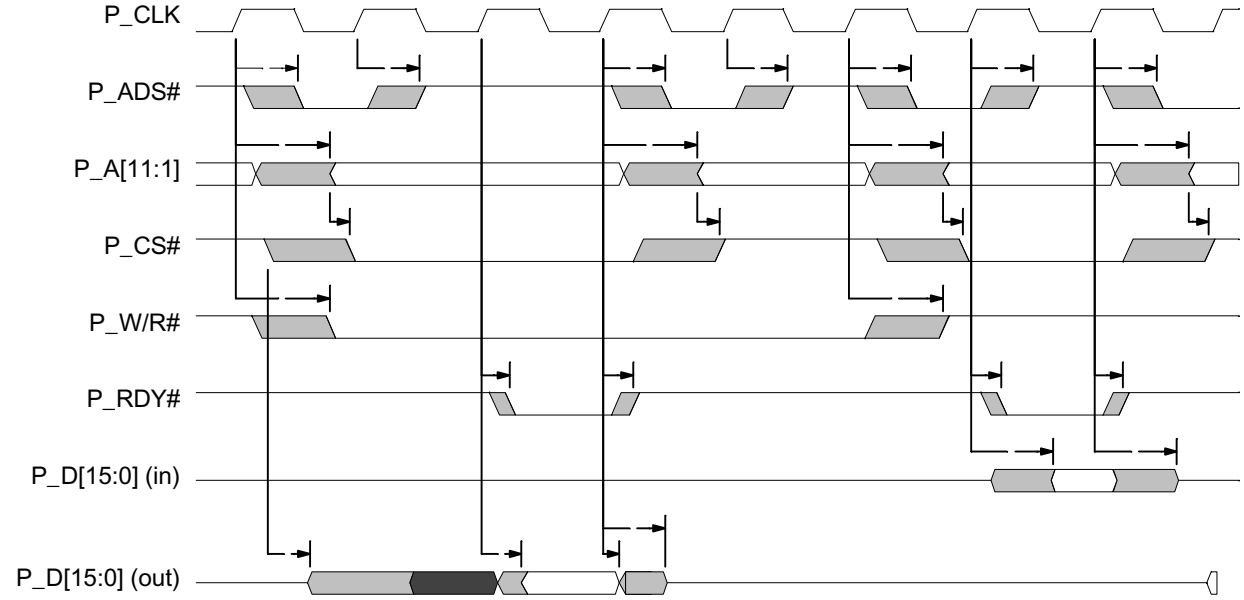
2.2.2 Motorola MPC801 Processor Interface



Note: Mnemonics with in {} are the equivalent signals defined by MPC801

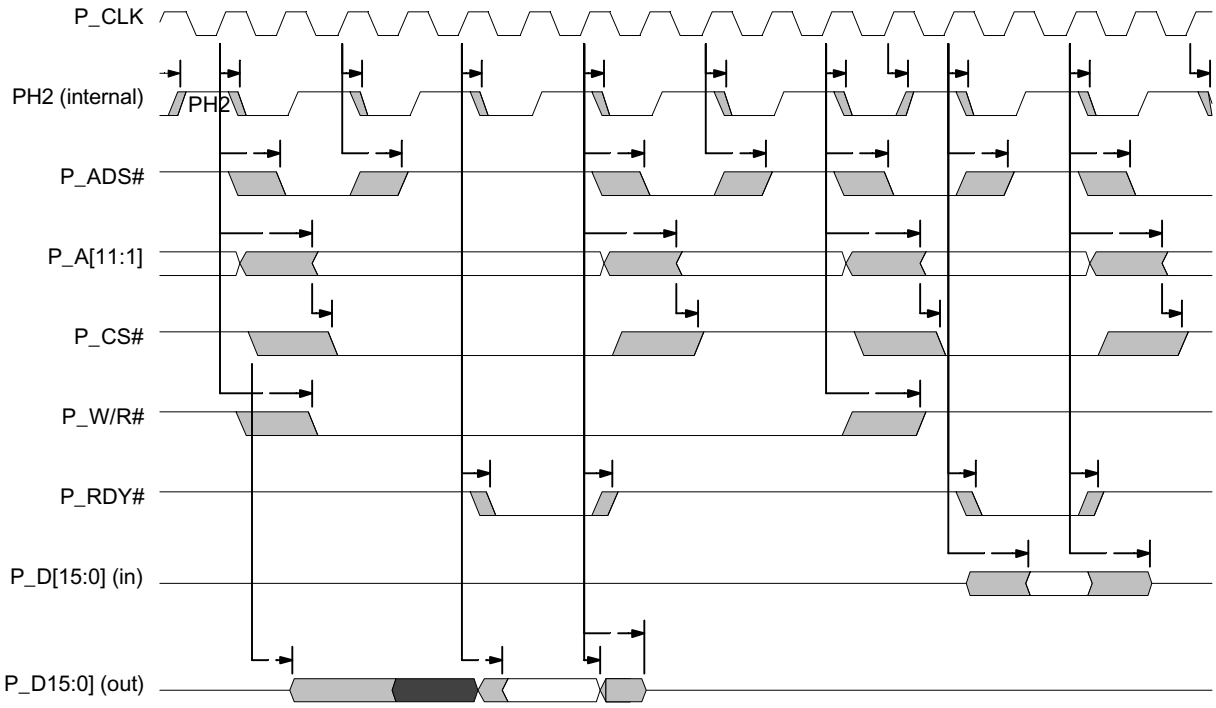
Typical Motorola MPC801 CPU I/O Access Operations

2.2.3 Intel 486 Processor Interface

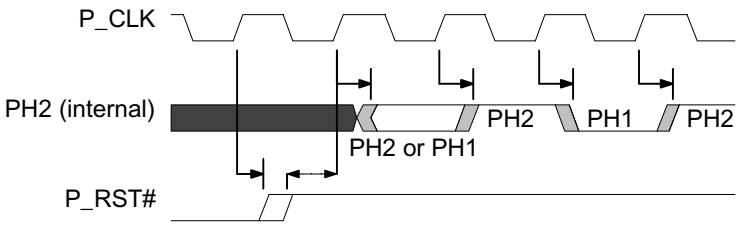


Typical 486 CPU I/O Access Operations

2.2.4 Intel 386 Processor Interface



Typical 386 CPU I/O Access Operations



Internal PH2 Clock Synchronization **

Note: ** See Intel 386 Processor Data Book for more details

2.2.5 Register Map

Note: All 32-bit registers are D-word aligned.

All 16-bit registers are also D-word aligned and right justified.

For the Little Endian CPUs, register offset bit [1,0] are always set to be 00.

For the Big Endian CPUs, register offset bit [1,0] are always set to be 10.

① This is a Global Register. CPU is allowed to write the Global Register of all devices by a single operation.

② These registers are reserved for system diagnostic usage only.

Register	Description	I/O Offset		Reg. Size	W/R	Note:
		Little Endian	Big Endian			
Device Configuration Registers (DCR)						
GCR	Global Control Register	hF00	hF02	16-bit	W/--	①
DCR0	Device Status Register	hF00	hF02	16-bit	--/R	
DCR1	Signature & Revision Register	hF10	hF12	16-bit	--/R	
DCR2	ID Register	hF20	hF22	16-bit	W/R	
DCR3	Device Configuration Register	hF30	hF32	16-bit	W/R	
DCR4	Interfaces Status Register	hF40	hF42	16-bit	--/R	
DTSR	Test Register	hF70	hF72	16-bit	W/R	
Interrupt Controls						
ISR	Interrupt Status Register – Unmasked	hF80	hF82	16-bit	--/R	
ISRM	Interrupt Status Register – Masked	hF90	hF92	16-bit	--/R	
IMSK	Interrupt Mask Register	hFA0	hFA2	16-bit	W/R	
IAR	Interrupt Acknowledgment Register	hFB0	hFB2	16-bit	W/--	
Buffer Memory Interface						
MWAR	Memory Write Address Reg. – Single Cycle	hE08	hE08	32-bit	W/R	
MRAR	Memory Read Address Reg. – Single Cycle	hE18	hE18	32-bit	W/R	
MBAR	Memory Address Register – Burst Mode	hE28	hE28	32-bit	W/R	
MWBS	Memory Write Burst Size (in D-words)	hE40	hE42	16-bit	W/R	
MRBS	Memory Read Burst Size (in D-words)	hE50	hE52	16-bit	W/R	
MWDR	Memory Write Data Register	hE68	hE68	32-bit	W/--	
MWDX	Memory Write Data Reg. – Byte Swapping	hE6C	hE6C	32-bit	W/--	
MRDR	Memory Read Data Register	hE68	hE68	32-bit	--/R	
MRDX	Memory Read Data Reg. – Byte Swapping	hE6C	hE6C	32-bit	--/R	
FCB Buffer & Stack Management						
FCBBA	Frame Control Buffer – Base Address	hD00	hD02	16-bit	W/R	
FCBAG	Frame Control Buffer – Buffer Aging Status	hD30	hD32	16-bit	--/R	②
FCBSL	Frame Ctrl Buffer Stack – Size Limit	hD90	hD92	16-bit	W/R	
FCBST	Frame Ctrl Buffer Stack – Buffer Low Threshold	hDA0	hDA2	16-bit	W/R	
FCBSS	Frame Ctrl Buffer Stack – Allocation Status	hDB0	hDB2	16-bit	--/R	②

Register	Description	I/O Offset		Reg. Size	W/R	Note:
		Little Endian	Big Endian			
Access Control Function (Chip Level controls)						
AVXR	VLAN Control Table (VCT) Index Register	hC00	hC02	16-bit	W/--	
AVDR	VCT Data Register	hC10	hC12	16-bit	W/R	
AVTC	VLAN Type Code	hC20	hC22	16-bit	W/R	
AXSC	Transmission Scheduling Control Register	hC30	hC32	16-bit	W/R	
AMIIC	MII Command Register	hC40	hC40	32-bit	W/--	
AMIIS	MII Status Register	hC40	hC40	32-bit	--/R	
AFCR	Flow Control Register	hC70	hC72	16-bit	W/R	
AMAR0	Multicast Address. for MAC Control Frames Byte [1,0]	hC80	hC82	16-bit	W/R	
AMAR1	Byte [3,2]	hC90	hC92	16-bit	W/R	
AMAR2	Byte [5,4]	hCA0	hCA2	16-bit	W/R	
AMCT	MAC Control FrameType Code Register	hCB0	hCB2	16-bit	W/R	
ADAR0	Base MAC Address Register – Byte [1,0]	hCC0	hCC2	16-bit	W/R	
ADAR1	Base MAC Address Register – Byte [3,2]	hCD0	hCD2	16-bit	W/R	
ADAR2	Base MAC Address Register – Byte [5,4]	hCE0	hCE2	16-bit	W/R	
Ethernet MAC Port Control Registers – (substitute [n] with Port Number, n = {0..3])						
ECR0	MAC Port Control Register	h*n*00	h*n*02	16-bit	W/R	
ECR1	MAC Port Configuration Register	h*n*10	h*n*12	16-bit	W/R	
ECR2	MAC Port Interrupt Mask Register	hn20	hn22	16-bit	W/R	
ECR3	MAC Port Interrupt Status Register	hn30	hn32	16-bit	--/R	
EXSR	MAC Tx Status Register	hn40	hn42	16-bit	--/R	②
EXEC	MAC Tx Error Counters	hn50	hn52	16-bit	--/R	②
ERSR	MAC Rx Status Register	hn68	hn68	32-bit	--/R	②
EREC	MAC Rx Error Counters	hn78	hn78	32-bit	--/R	②

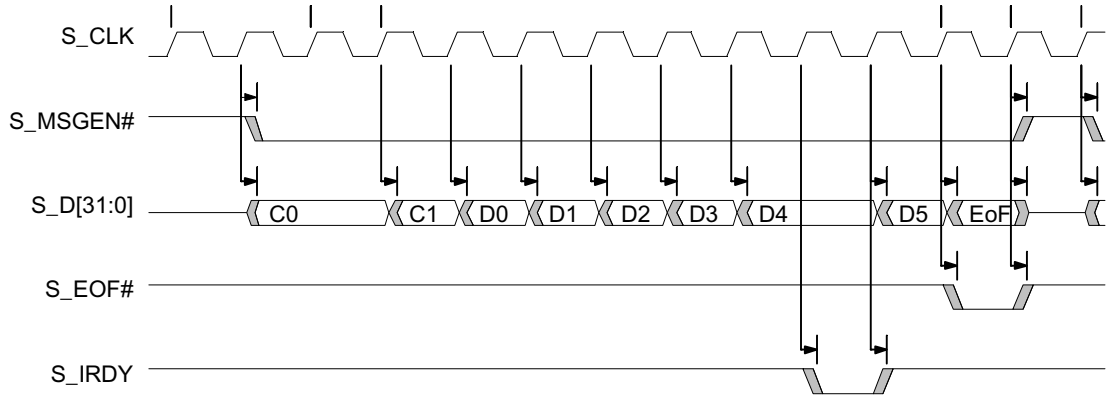
2.3 XpressFlow Bus Operation

- Zarlink's optimized XpressFlow Bus architecture
- Provides 1.6G bps switching bandwidth
  - ◊ -33 1.07G bps
  - ◊ -40 1.28G bps
  - ◊ -50 1.6G bps
- Full multi bus master structure
- Allows *XpressFlow* Engine to communicate with Access Controllers via a message passing protocol
  - ◊ Command Messages for passing control information between devices
  - ◊ Data Messages for forwarding an Ethernet frame from receiving port to transmission port
- Built-in intelligent bus load regulator for data traffic balancing
- Provides centralized bus arbitration with two level request priorities
  - ◊ High priority for Data Messages
  - ◊ Low priority for Command Messages

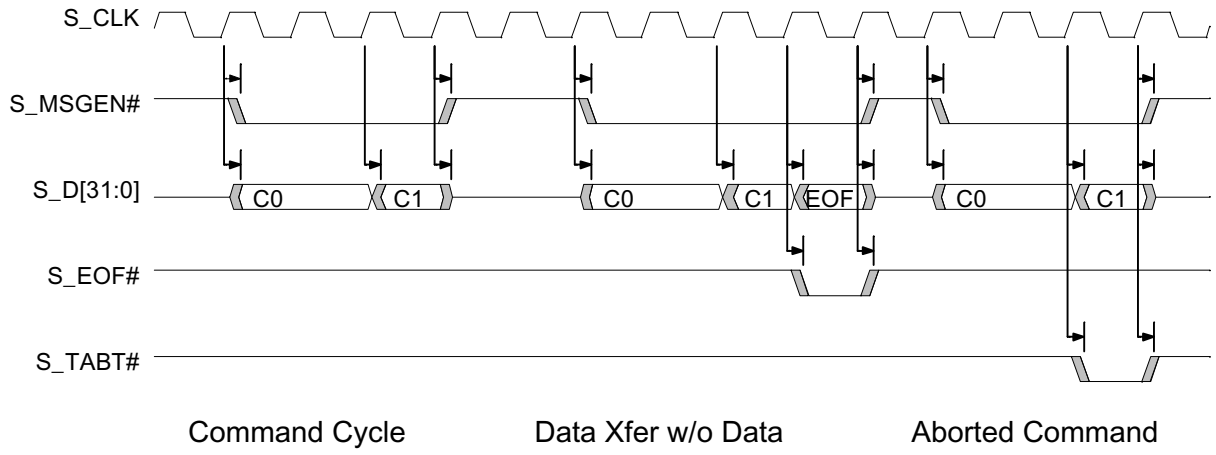
2.3.1 Pin Description

Symbol	Type	Name and Functions
S_D[31:0]	CMOS I/O-TS	***Data Bus Bit [31:0]*** – a 32-bit synchronous data bus. **Note:** *During the system RESET period, Data Bit [31:28] are used as Processor Interface Configuration bit [0:3]*
S_MSGEN#	CMOS I/O-TS	***Message Envelope*** – encompasses the entire period of a message transfer. Targets use the leading edge of this signal to detect the beginning of a message transfer, and to decode the message header for the intended target(s).
S_EOF#	CMOS I/O-TS	***End of Frame*** – only used by frame data transfer messages to identify the end of frame condition. This signal is synchronous with the Rx Frame Status word appended to the end of the message.
S_IRDY	CMOS I/O-TS	***Initiator Ready*** – a normal true signal. When negated, it indicates the initiator had asserted wait state(s) in between command words. Target should use this signal as enable signal for latching the data from the bus.
S_TABT#	CMOS I/O-OD	***Target Abort*** – when asserted, the target had aborted the reception of current message on the bus.
S_HPREQ#	CMOS I/O-OD	***High Priority Request*** – indicates one or more Bus Requester is requesting for high priority message transfer.
S_REQ#	CMOS Output	***Bus Request*** –Bus Request signals from Access Controller to Bus Access Arbitrator in *XpressFlow* Engine
S_GNT#	CMOS Input	***Bus Grant*** –Bus Grant signals from Bus Arbitrator to Bus Requester
S_OVLD#	CMOS Output	***Bus Overload*** – when asserted, all data forwarding bus bandwidth has been allocated. Cannot support additional load for data forwarding traffic.
S_CLK	CMOS Input	***XpressFlow Bus Clock*** – 33MHz system clock

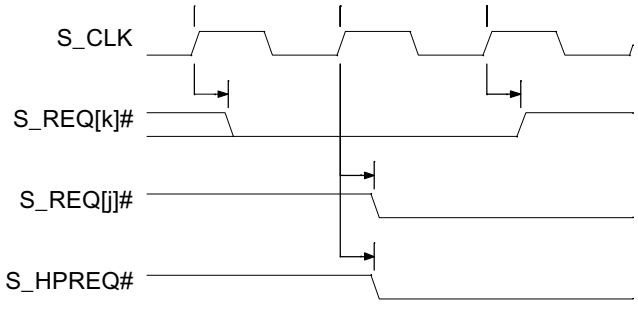
2.3.2 Bus Cycle Waveforms



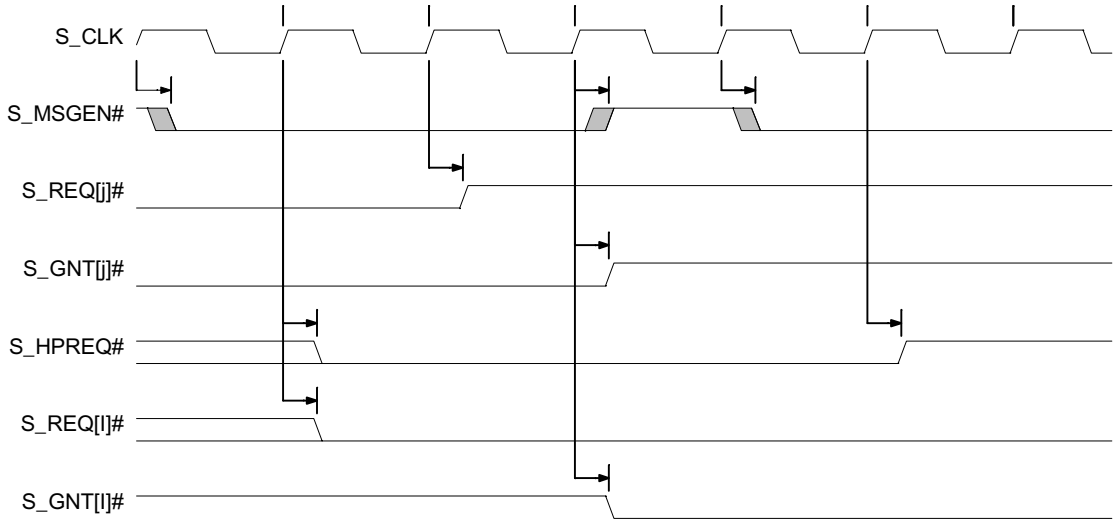
XpressFlow Bus Data Transfer Cycle



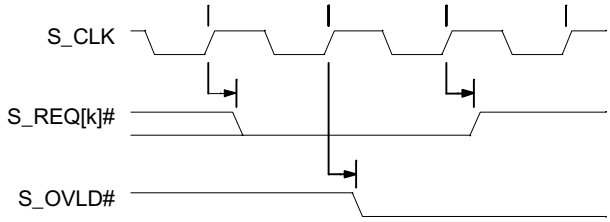
Other XpressFlow Bus Cycles



High Priority Request pre-empts the low priority request.



XpressFlow Bus arbitration



Bus Overload pre-empts the data transfer request

2.4 10Mb Serial Interface for Port 0 through 7

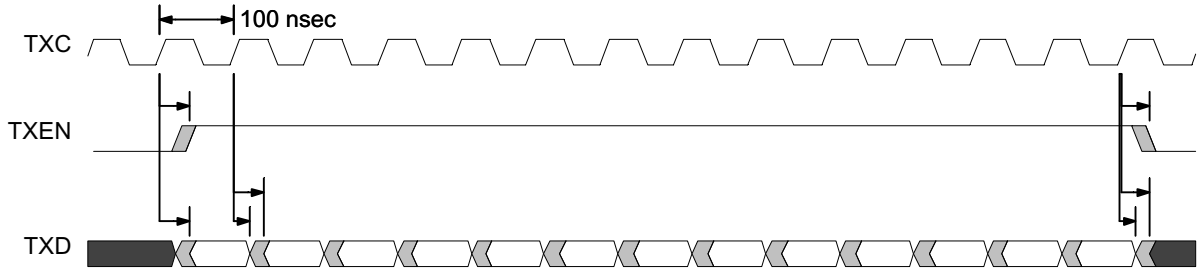
- Fully compliant with IEEE 802.3 10M bit Serial Interface Standard for connecting with external 10Mbps Ethernet Physical Layer Transceiver
- Supports 10Mbps 10BaseT serial interface
- Supports both half and full duplex operation

2.4.1 Pin Description

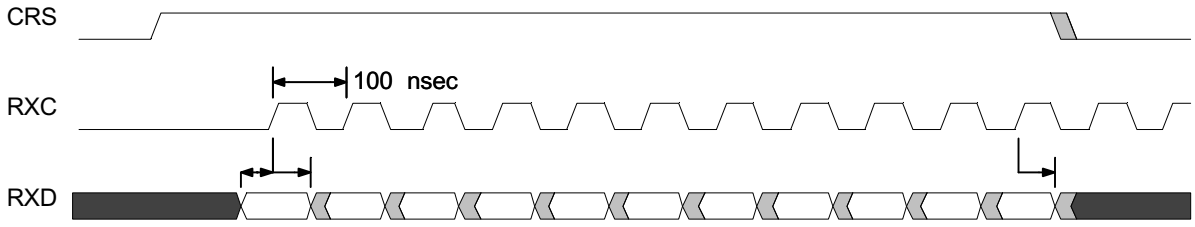
Symbol	Type	Name and Functions
Tn_RXD	TTL In (5VT)	***Receive Data*** – (one for each 10M bit Serial Interface Port) a receive data stream.
Tn_RXC	TTL In (5VT)	***Receive Clock*** – (one for each 10M bit Serial Interface Port) from external phy for sampling the receive data from Tn_RXD input
Tn_TXC	TTL In (5VT)	***Transmit Clock*** – (one for each 10M bit Serial Interface Port) a continuous clock input with 35% to 65% duty cycles.
Tn_TXEN	CMOS Output	***Transmit Enable*** – (one for each 10M bit Serial Interface Port)
Tn_TXD	CMOS Output	***Transmit Data*** – (one for each 10M bit Serial Interface Port) a transmit data stream.
Tn_LPBK ①	CMOS Output	***Loop Back Enable*** – (one for each 10M bit Serial Interface Port) The polarity of this signal is programmable via Port Configuration Register
Tn_FD ①	CMOS Output	***Full Duplex Mode*** – (one for each 10M bit Serial Interface Port) The polarity of this signal is programmable via Port Configuration Register
Tn_COL	TTL In (5VT)	***Collision Detected*** – (one for each 10M bit Serial Interface Port)
Tn_CRS	TTL In (5VT)	***Carrier Sense*** – (one for each 10M bit Serial Interface Port)
Tn_LNK ①	TTL In (5VT)	***Link Status*** – (one for each 10M bit Serial Interface Port) The polarity of this signal is programmable via Port Configuration Register

Note: "n" is the port number [7:0]

① These signals have programmable output polarity.



10M bit Serial Interface – Transmit Timing



10M bit Serial Interface – Receive Timing

2.5 Test Pins

Symbol	Type	Name and Functions
T_MODE	CMOS I/O-TS	***Test Mode Selection & Test Output*** – Set Test Mode upon Reset, and provides test status output during test mode

3. DC SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-50°C to +125°C
Operating Temperature	0°C to +70°C
Supply Voltage V_{DD} with Respect to V_{SS}	+3.0 V to +3.6 V
Voltage on 5V Tolerant Input Pins	-0.5 V to (V_{DD} + 1.8 V)
Voltage on Other Input Pins	-0.5 V to (V_{DD} + 10%)

Stresses above those listed may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

3.2 DC CHARACTERISTICS

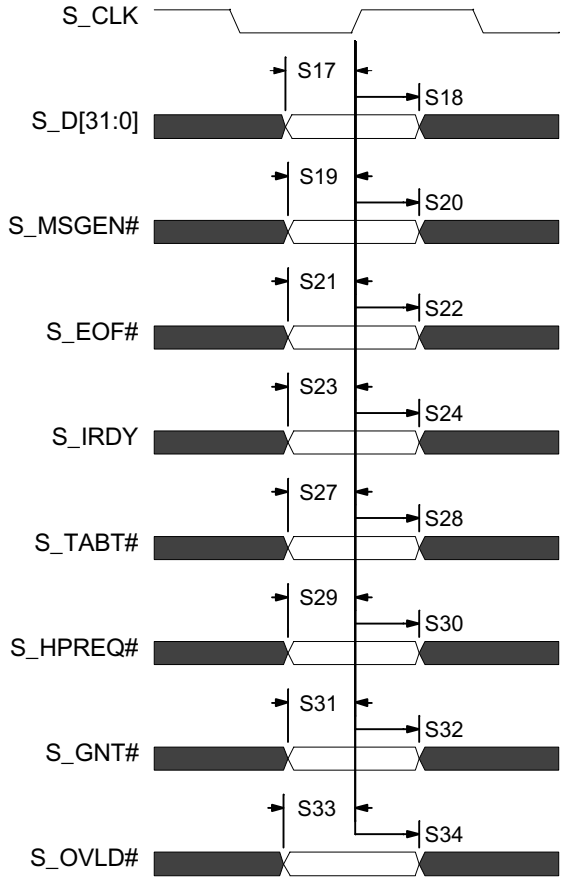
V_{DD} = +3.0 V to +3.6 V $T_{AMBIENT}$ = 0°C to +70°C

Symbol	Parameter Description	Preliminary			Unit
		Min	Type	Max	
f_{osc}	Frequency of Operation (-40)	20		40.0000	MHz
	Frequency of Operation (-50)	20		50.0000	MHz
	Frequency of Operation (-66)	20		66.6667	MHz
I_{DD}	Supply Power – @ 40 MHz (V_{DD} =3.3 V)		300	500	mA
	Supply Power – @ 50 MHz (V_{DD} =3.3 V)		300	500	mA
	Supply Power – @ 66.67 MHz (V_{DD} =3.3 V)		360	600	mA
$V_{OH-CMOS}$	Output High Voltage (CMOS) I_{OH} = maximum	V_{DD} - 0.5			V
$V_{OL-CMOS}$	Output Low Voltage (CMOS) I_{OL} = maximum			0.45	V
V_{OH-TTL}	Output High Voltage (TTL) I_{OH} = maximum	2.4			V
V_{OL-TTL}	Output Low Voltage (TTL) I_{OL} = maximum			0.45	V
$V_{IH-CMOS}$	Input High Voltage (CMOS)	VDD x 70%		V_{DD} + 10%	V
$V_{IL-CMOS}$	Input Low Voltage (CMOS)	-0.5		VDD x 30%	V
V_{IH-TTL}	Input High Voltage (TTL)	2.0		V_{DD} + 10%	V
V_{IL-TTL}	Input Low Voltage (TTL)	-0.3		+0.8	V
V_{IH-5VT}	Input High Voltage (TTL 5V tolerant)	2.0		V_{DD} + 1.8	V
V_{IL-5VT}	Input Low Voltage (TTL 5V tolerant)	-0.3		+0.8	V
I_{LI}	Input Leakage Current (0.1 V ≤ V_{IN} ≤ V_{DD}) (all pins except those with internal pull-up/pull-down resistors)			±10	µA
I_{LO}	Output Leakage Current (0.1 V ≤ V_{OUT} ≤ V_{DD})			±15	µA
I_{IH}	Input Leakage Current V_{IH} = V_{DD} - 0.1 V (pins with internal pull-down resistors)			60	µA
I_{IL}	Input Leakage Current V_{IL} = 0.1 V (pins with internal pull-up resistors)			-60	µA
C_{IN}	Input Capacitance		8		pF
C_{OUT}	Output Capacitance		8		pF
$C_{I/O}$	I/O Capacitance		10		pF

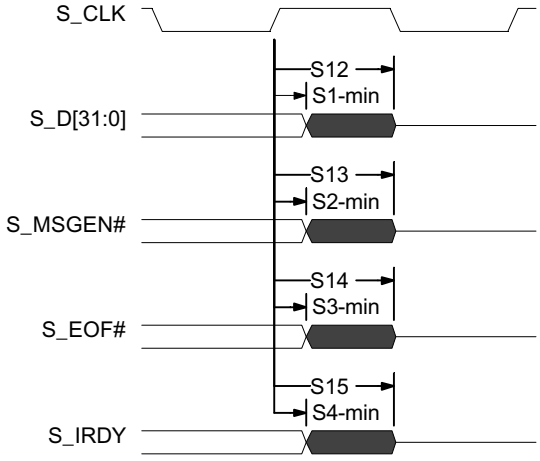
Notes:

4. AC SPECIFICATION

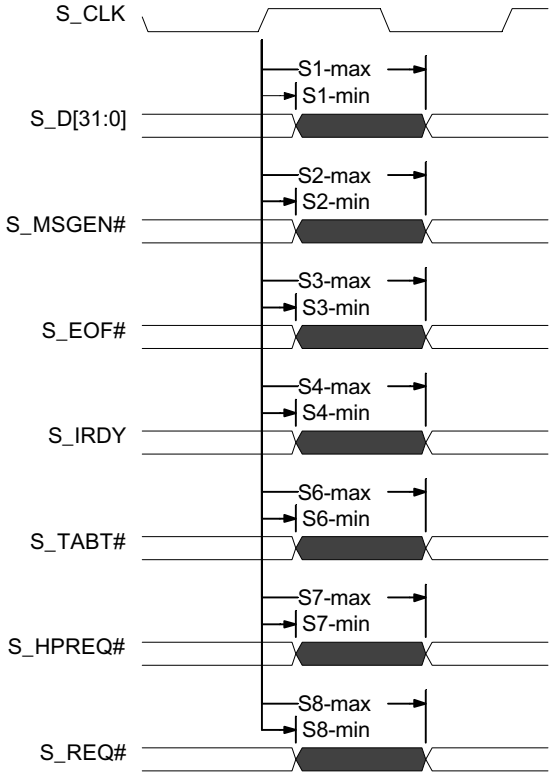
4.1 XpressFlow Bus Interface:



XpressFlow Bus Interface –
Input setup and hold timing



XpressFlow Bus Interface –
Output float delay timing

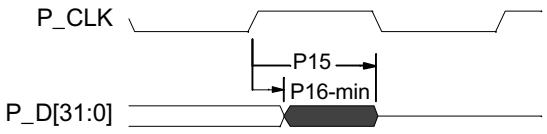


XpressFlow Bus Interface –
Output valid delay timing

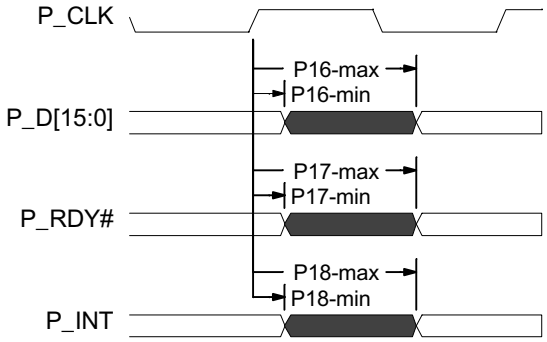
Symbol	Parameter	-40		-50		-66		Note:
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
S1	S_D[31:0] output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S2	S_MSGEN# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S3	S_EOF# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S4	S_IRDY output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S6	S_TABT# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S7	S_HPREQ# output valid delay	6	14	5	11	4	8.5	C_L = 50pf
S8	S_REQ# output valid delay	6	14	5	11	4	8.5	C_L = 20pf
S12	S_D[31:0] output float delay		18		15		12	
S13	S_MSGEN# output float delay		18		15		12	
S14	S_EOF# output float delay		18		15		12	
S15	S_IRDY output float delay		18		15		12	
S17	S_D[31:0] input set-up time	2		1.5		1		
S18	S_D[31:0] input hold time	5.5		4.5		3.5		
S19	S_MSGEN# input set-up time	2		1.5		1		
S20	S_MSGEN# input hold time	5.5		4.5		3.5		
S21	S_EOF# input set-up time	2		1.5		1		
S22	S_EOF# input hold time	5.5		4.5		3.5		
S23	S_IRDY input set-up time	2		1.5		1		
S24	S_IRDY input hold time	5.5		4.5		3.5		
S27	S_TABT# input set-up time	13		10		8		
S28	S_TABT# input hold time	5.5		4.5		3.5		
S29	S_HPREQ# input set-up time	2		1.5		1		
S30	S_HPREQ# input hold time	5.5		4.5		3.5		
S31	S_GNT# input set-up time	13		10		8		
S32	S_GNT# input hold time	5.5		4.5		3.5		
S33	S_OVLD# input set-up time	15		12		9		
S34	S_OVLD# input hold time	5.5		4.5		3.5		

AC Characteristics – XpressFlow Bus Interface

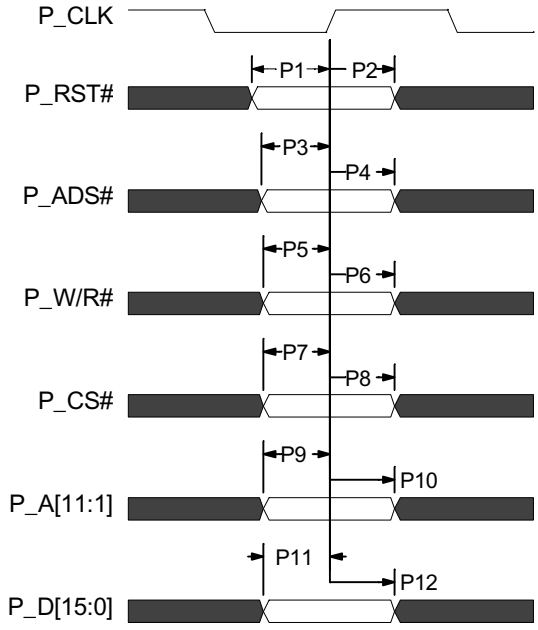
4.2 CPU Bus Interface:



**CPU Bus Interface –
Output float delay timing**



CPU Bus Interface –
Output valid delay timing

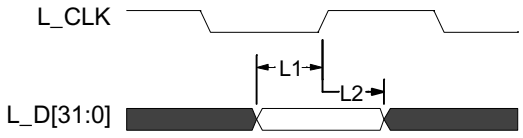


**CPU Bus Interface –
Input setup and hold timing**

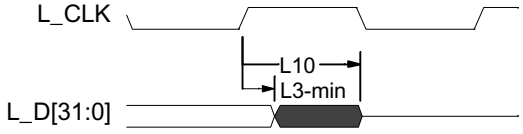
Symbol	Parameter	-40		-50		-66		Note:
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
P1	P_RST# input setup time	13		10		8		
P2	P_RST# input hold time	3.5		2.5		2		
P3	P_ADS# input set-up time	13		10		8		
P4	P_ADS# input hold time	3.5		2.5		2		
P5	P_W/R# input set-up time	13		10		8		
P6	P_W/R# input hold time	3.5		2.5		2		
P7	P_CS# input set-up time	13		10		8		
P8	P_CS# input hold time	3.5		2.5		2		
P9	P_A[11:1] input set-up time	13		10		8		
P10	P_A[11:1] input hold time	3.5		2.5		2		
P11	P_D[31:0]# input set-up time	13		10		8		
P12	P_D[31:0]# input hold time	3.5		2.5		2		
P15	P_D[31:0]# output float delay		17		13		10	
P16	P_D[31:0]# # output valid delay		8.5		6.5		5	C_L = 60pf
P17	P_RDY# output valid delay		8.5		6.5		5	C_L = 60pf
P18	P_INT# output valid delay		17		13		10	C_L = 20pf

AC Characteristics -- CPU Bus Interface

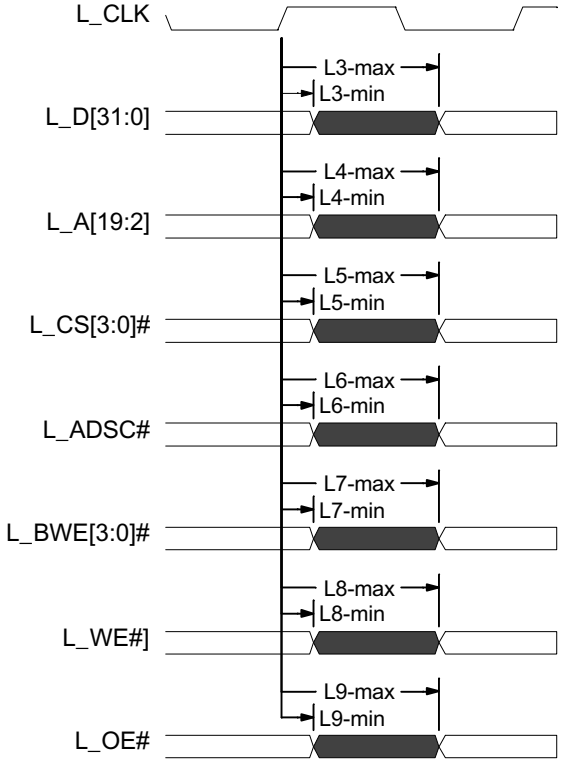
4.3 Local Memory Interface:



Local Memory Interface – Input setup and hold timing



Local Memory Interface – Output float delay timing



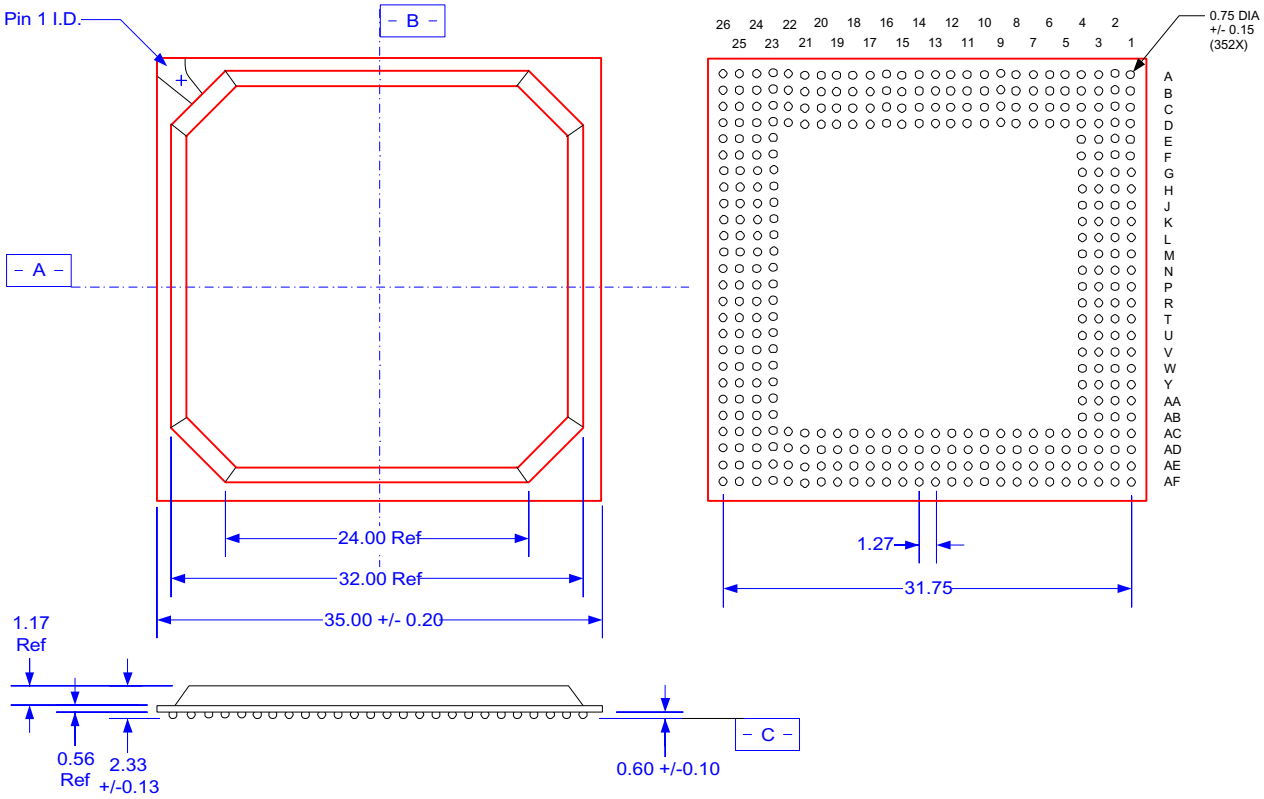
Local Memory Interface – Output valid delay timing

Symbol	Parameter	-40		-50		-66		Note:
		Min (ns)	Max (ns)	Min (ns)	Max (ns)	Min (ns)	Max (ns)	
L1	L_D[31:0]# input set-up time	6.5		5.5		4		
L2	L_D[31:0]# input hold time	3		2.5		2		
L3	L_D[31:0]# output valid delay		17		13		10	C_L = 30pf
L4	L_A[19:2] output valid delay		17		13		10	C_L = 30pf
L6	L_ADSC# output valid delay		17		13		10	C_L = 30pf
L7	L_BWE[3:0]# output valid delay		17		13		10	C_L = 30pf
L8	L_WE# output valid delay		17		13		10	C_L = 10pf
L9	L_OE# output valid delay		17		13		10	C_L = 10pf
L10	L_D[31:0]# output float delay		22		18		14	

AC Characteristics – Local Memory Interface

5. PACKAGING INFORMATION

352-PIN BGA
(35x35x2.33mm)



Ordering Information				
Part Number	**Description**	**Identification**	**Zarlink Use**	**Revision**
EA218E	8-port 10Mbps Ethernet network access	**C 0 B**	**TAV**	**rrr**

Environmental – *C = Commercial*
I = Industrial

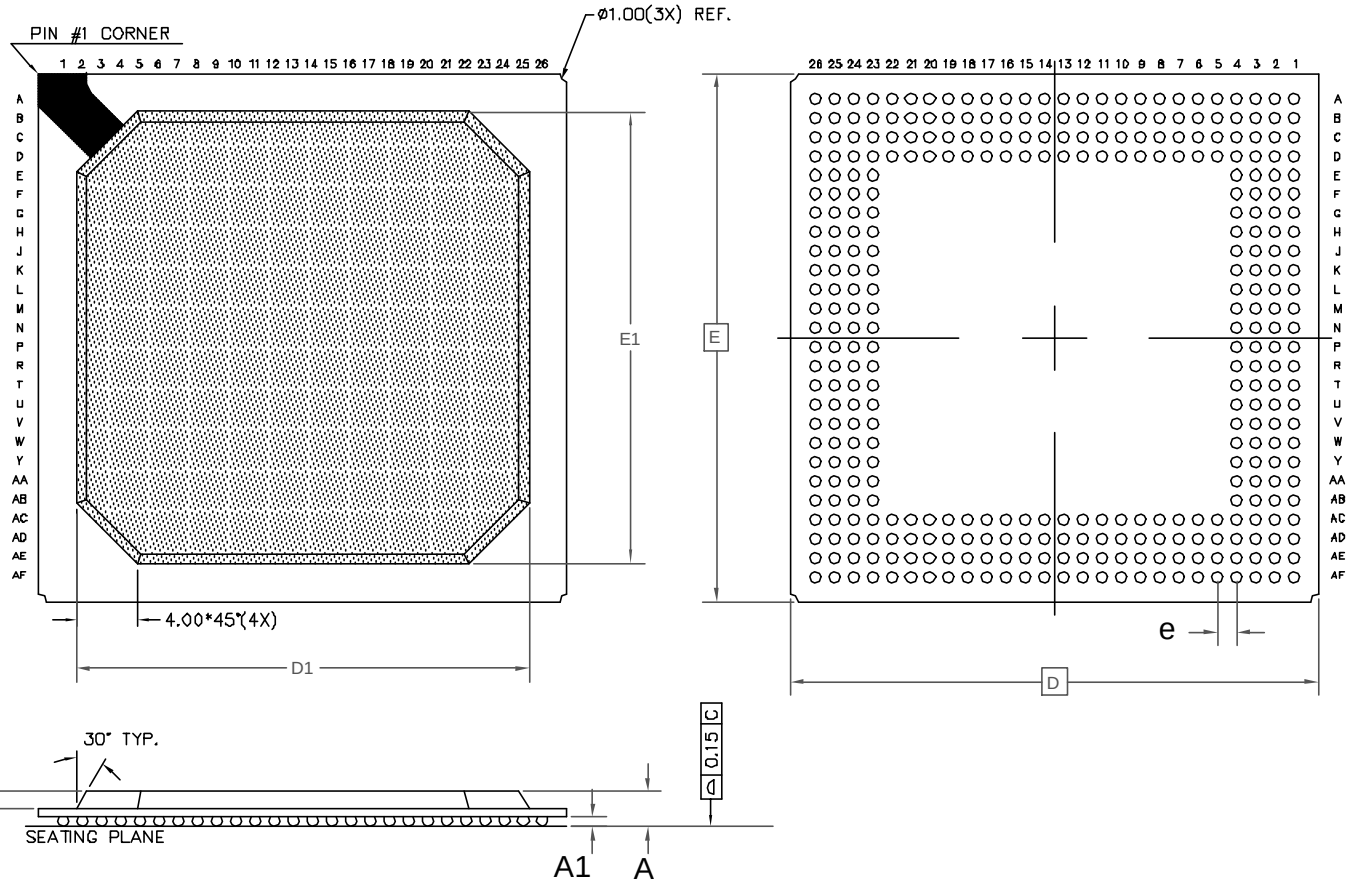
Speed grade - *0 = 40 MHz*
5 = 50 MHz
6 = 66 MHz

Package - *B = BGA*

Revision - *001 = Rev.1*
For latest revision, leave blank

ZARLINK SEMICONDUCTOR

400 March Road
Ottawa, Ontario, Canada K2K 3H4
Tel. 613 592 0200, FAX: 613 592 1010
Web Site: www.zarlink.com



DIMENSION	MIN	MAX
A	2.20	2.46
A1	0.50	0.70
A2	1.17 REF	
D	34.80	35.20
D1	30.00 REF	
E	34.80	35.20
E1	30.00 REF	
b	0.60	0.90
e	1.27	
N	352	
Conforms to JEDEC MS - 034		

1. CONTROLLING DIMENSIONS ARE IN MM
2. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER
3. SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
4. N IS THE NUMBER OF SOLDER BALLS
5. NOT TO SCALE.
6. SUBSTRATE THICKNESS IS 0.56 MM

ISSUE	1			
ACN	213933			
DATE	20Jan03			
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes: BP / G

Package Code GA

Package Outline for 352 Ball PBGA (35x35x2.33mm)

GPD00819

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE