



AP01

T-43-25

8 Channel Power MOSFET Array Monolithic P-channel Enhancement Mode

Ordering Information

BV _{DSS} / BV _{DGS} (min)	R _{DS(ON)} (max)	I _{D(ON)} (min)	I _{DSS} ** @ V _{DS} = -100V Max	I _{DSS} ** @ V _{DS} = -250V Max	Order Number / Package			
					18-Lead Ceramic DIP	18-Lead Plastic DIP	Plastic SOW-20*	Die
-160V	700Ω	-15mA	-1.5nA	—	AP0116NB	AP0116NA	AP0116WG	AP0116ND
-200V	600Ω	-15mA	—	—	AP0120NB	AP0120NA	—	AP0120ND
-300V	600Ω	-15mA	—	—	AP0130NB	AP0130NA	—	AP0130ND
-320V	700Ω	-15mA	—	-1.5nA	AP0132NB	AP0132NA	AP0132WG	AP0132ND
-400V	700Ω	-15mA	—	—	AP0140NB	AP0140NA	AP0140WG	AP0140ND

* Same as SO-20 with 300 mil wide body.

** Average current per channel, measured with all eight channels connected in parallel.

Features

- Low drain to source leakage for AP0116 and AP0132
- 200-volt to 400-volt capability
- Interfaces directly to CMOS logic
- 8 independent channels
- Low crosstalk between channels
- Low power dissipation
- Pin compatible with industry standard driver array
- Freedom from secondary breakdown

General Description

The Supertex AP01 series of high voltage arrays is designed to provide the interface between MOS logic and loads requiring high voltages and intermediate currents. Each circuit consists of eight channels in a common-source configuration with open drains. This design minimizes the number of package leads needed.

The AP0116 and AP0132 are ideally suited for low leakage/high impedance measurement, providing excellent accuracy and resolution for Automatic Test Equipment.

Applications

- High voltage electroluminescent panel drivers
- High voltage electrostatic array drivers
- General multi-channel driver array

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C
Channel-to-Channel Crosstalk	10mV/V

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

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Package	I _D (continuous)*	I _D (pulsed)*	Power Dissipation @ T _C = 25°C	θ _{JA} °C/W	θ _{JC} °C/W	I _{DR}	I _{DRM} *
18 lead plastic	-15mA	-40mA	1.5W	135	83	-15mA	-40mA
18 lead Ceramic	-15mA	-40mA	2.0W	85	62	-15mA	-40mA

* I_D (continuous) is limited by max rated T_J.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1, 2 and 3)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	AP0116 -160 AP0120 -200 AP0130 -300 AP0132 -320 AP0140 -400			V	I _D = -100µA, V _{GS} = 0V
VGS(th)	Gate Threshold Voltage	-2		-5	V	V _{GS} = V _{DS} , I _D = -1mA
ΔVGS(th)	Change in VGS(th) with Temperature		-3.5		mV/°C	V _{GS} = V _{DS} , I _D = -1mA
IGSS	Gate Body Leakage	AP0120 AP0130 AP0140		-10	nA	V _{GS} = ±20V, V _{DS} = 0
		AP0116 AP0132		-1	nA	V _{GS} = ±20V, V _{DS} = 0 (Note 3)
IDSS	Zero Gate Voltage Drain Current	AP0120		-1	µA	V _{GS} = 0, V _{DS} = Max Rating
		AP0130		-1	mA	V _{GS} = 0, V _{DS} = 0.8 Max Rating T _A = 125°C
		AP0116		-1.5	nA	V _{GS} = 0, V _{DS} = -100V (Note 3)
				-1	mA	V _{GS} = 0, V _{DS} = 0.8 Max Rating T _A = 125°C
		AP0132		-1.5	nA	V _{GS} = 0, V _{DS} = -250V (Note 3)
				-1	mA	V _{GS} = 0, V _{DS} = 0.8 Max Rating T _A = 125°C
ID(ON)	ON-State Drain Current	-15			mA	V _{GS} = -10V, V _{DS} = -25V
RDS(ON)	Static Drain-to-Source	AP0120 AP0130		600	Ω	V _{GS} = -10V, I _D = -10mA
	ON-State Resistance	AP0116 AP0132 AP0140		700	Ω	V _{GS} = -10V, I _D = -10mA
ΔRDS(ON)	Change in RDS(ON) with Temperature		0.8		%/°C	V _{GS} = -10V, I _D = -10mA
GFS	Forward Transconductance	3.0	5.0		mS	V _{DS} = -25V, I _D = -5mA
Ciss	Input Capacitance		5.0	7.5	pF	V _{DS} = -25V, V _{GS} = 0 f = 1 MHz
COSS	Common Source Output Capacitance		3.0	5.0		
CRSS	Reverse Transfer Capacitance		1.0	2.0		
t _d (ON)	Turn-ON Delay Time		3		ns	V _{DS} = -25V I _D = -10mA R _S = 50Ω, V _{GS} (ON) = -10V
t _r	Rise Time		3			
t _d (OFF)	Turn-OFF Delay Time		5			
t _f	Fall Time		3			
VSD	Diode Forward Voltage Drop			1.5	V	V _{GS} = 0, I _{SD} = -25mA

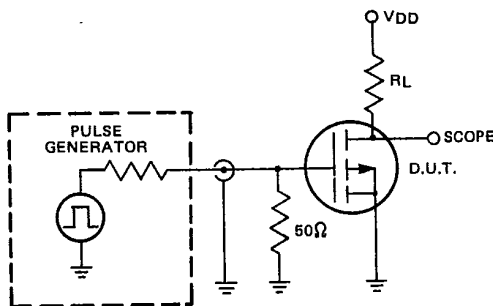
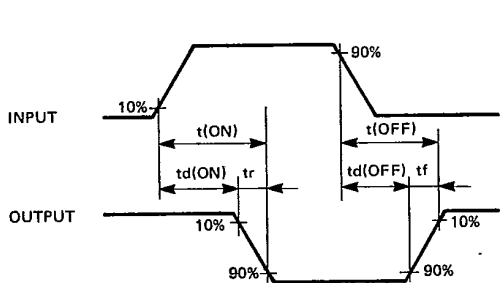
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300ms pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

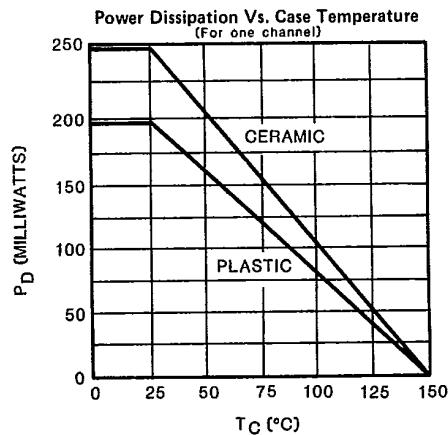
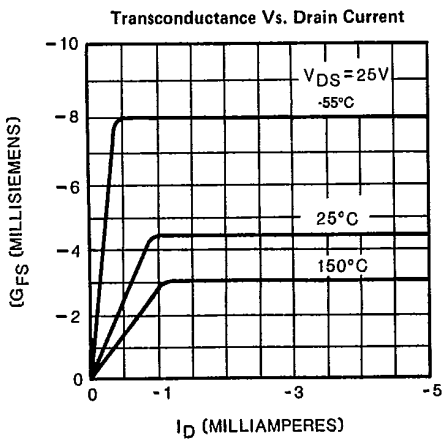
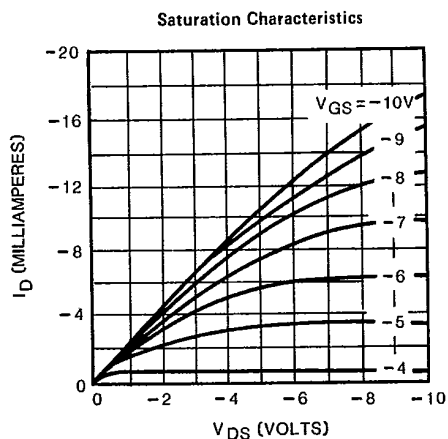
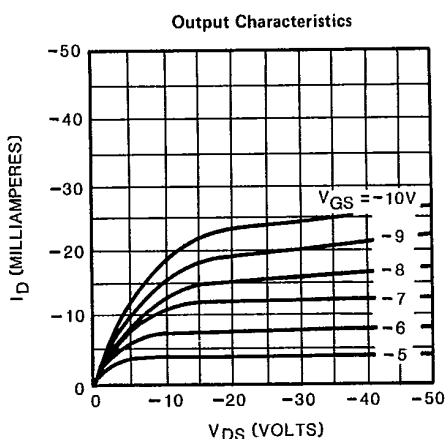
Note 3: Average current per channel, measured with all 8 channels connected in parallel.

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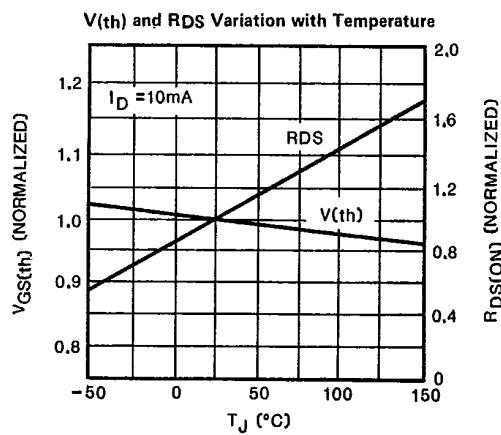
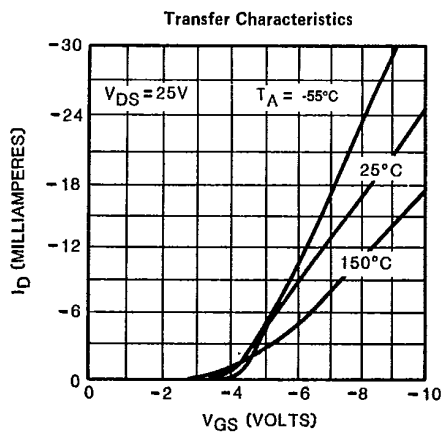
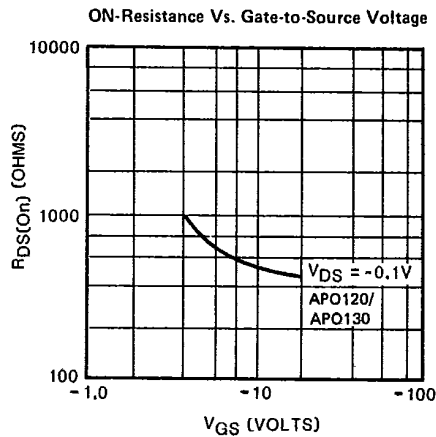
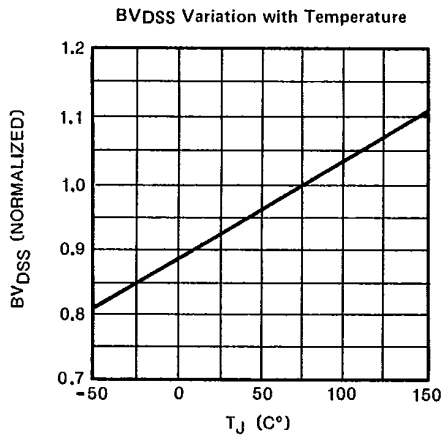
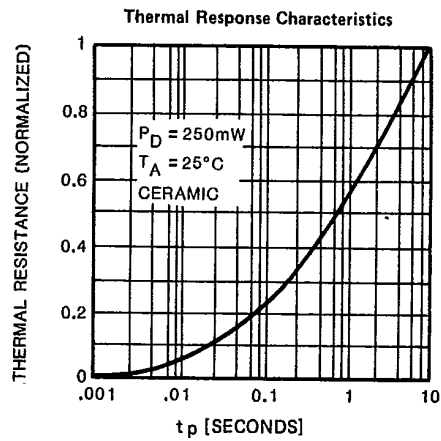
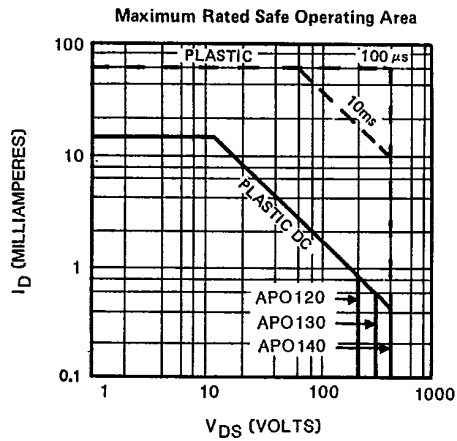
Switching Waveforms and Test Circuit



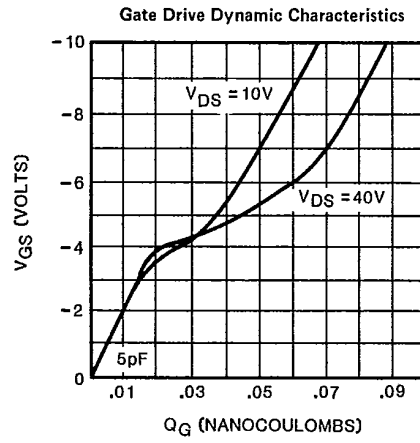
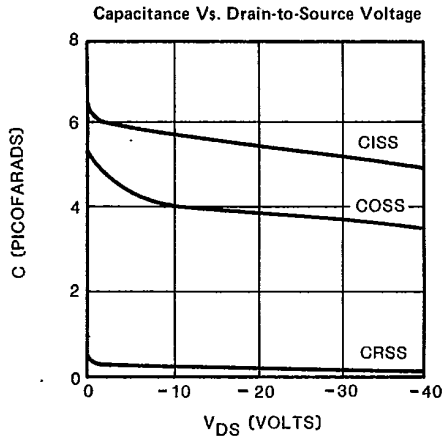
Typical Performance Curves



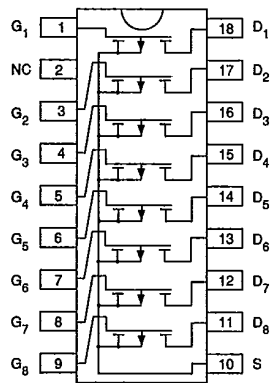
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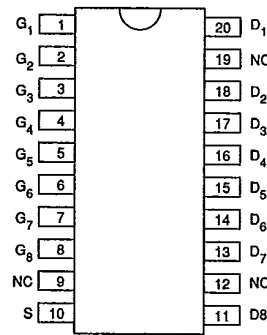
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Pin Configuration and Schematic



top view
18-pin DIP



top view
SOW-20