Process C1004
CMOS 1.0µm
5 Volt Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.55	0.75	0.95	V	100x1.0µm
Body Factor	γ_N		0.60		$V^{1/2}$	100x1.0µm
Conduction Factor	β_N	74	87	100	µA/V²	100x100µm
Effective Channel Length	$Leff_N$	0.60	0.75	0.90	µm	100x1.0µm
Width Encroachment	ΔW_N		0.8		µm	Per side
Punch Through Voltage	$BVDSS_N$	7			V	
Poly Field Threshold	$VTF_{P(N)}$	10			V	

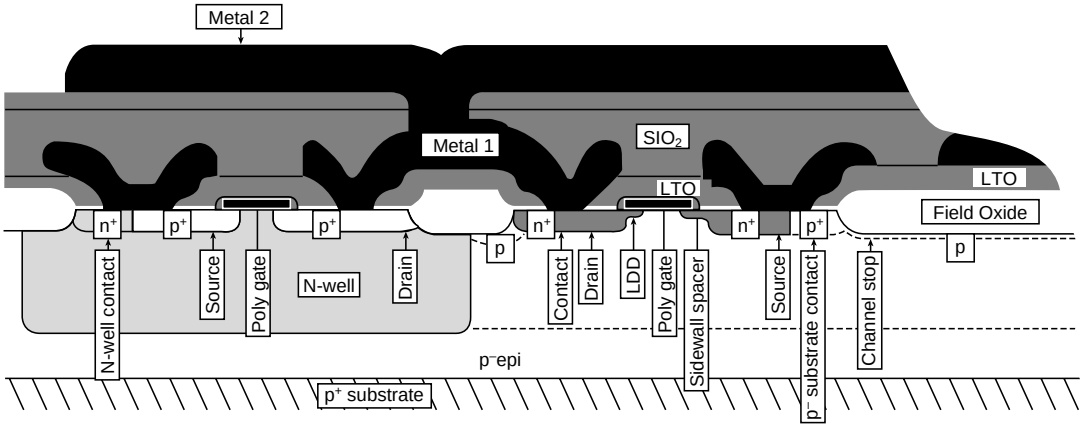
P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.85	–1.0	–1.15	V	100x1.0µm
Body Factor	γ_P		0.4		$V^{1/2}$	100x1.0µm
Conduction Factor	β_P	24	28	32	µA/V²	100x100µm
Effective Channel Length	$Leff_P$	0.83	0.98	1.13	µm	100x1.0µm
Width Encroachment	ΔW_P		0.85		µm	Per side
Punch Through Voltage	$BVDSS_P$	–7			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–10			V	

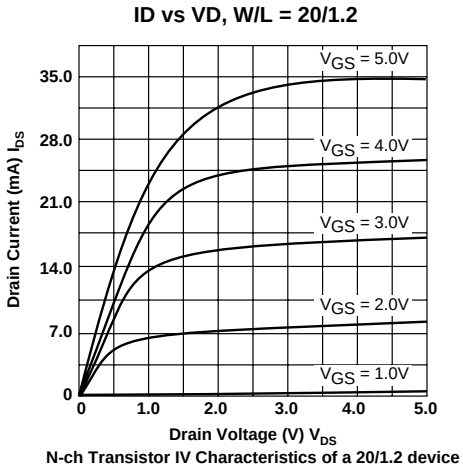
Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{N\text{-well(f)}}$	0.8	1.0	1.22	KΩ/□	n-well
N+ Sheet Resistance	ρ_{N+}	20	35	50	Ω/□	
N+ Junction Depth	x_{jN+}		0.45		µm	
P+ Sheet Resistance	ρ_{P+}	60	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.5		µm	
Gate Oxide Thickness	T_{GOX}		20		nm	
Field Oxide Thickness	T_{FIELD}		700		nm	
Poly Sheet Resistance	ρ_{POLY}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		50		mΩ/□	
Metal-2 Sheet Resistance	ρ_{M2}		30		mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{ox}	1.52	1.64	1.82	fF/µm²	
Metal-1 to Poly1	C_{M1P}		0.046		fF/µm²	
Metal-1 to SIlicon	C_{MIS}		0.028		fF/µm²	
Metal-2 to Metal-1	C_{MM}		0.038		fF/µm²	

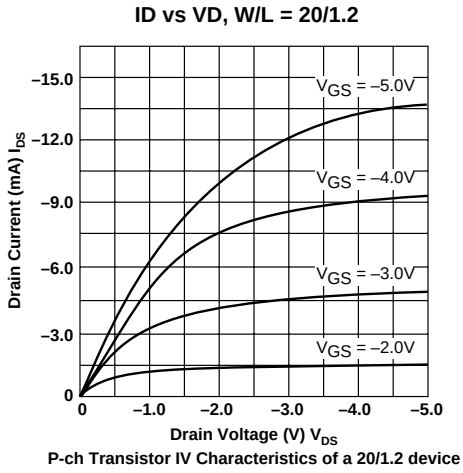
Physical Characteristics

Starting Material	P <100>	N+/P+ Width/Space	2.0 / 1.2µm
Starting Mat. Resistivity	7-8.5 Ω-cm	N+ To P+ Space	7.0µm
Typ. Operating Voltage	5V	Contact To Poly Space	0.8µm
Well Type	N-well	Contact Overlap Of Diffusion	0.7µm
Metal Layers	2	Contact Overlap Of Poly	0.7µm
Poly Layers	1	Metal-1 Overlap Of Contact	0.7µm
Contact Size	1.2x1.2µm	Metal-1 Overlap Of Via	0.7µm
Via Size	1.2x1.2µm	Metal-2 Overlap Of Via	0.7µm
Metal-1 Width/Space	1.4 / 1.2µm	Minimum Pad Opening	65x65µm
Metal-2 Width/Space	2.0 / 1.4µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	1.0 / 1.4µm	Minimum Pad Pitch	80.0µm





N-ch Transistor IV Characteristics of a 20/1.2 device



P-ch Transistor IV Characteristics of a 20/1.2 device