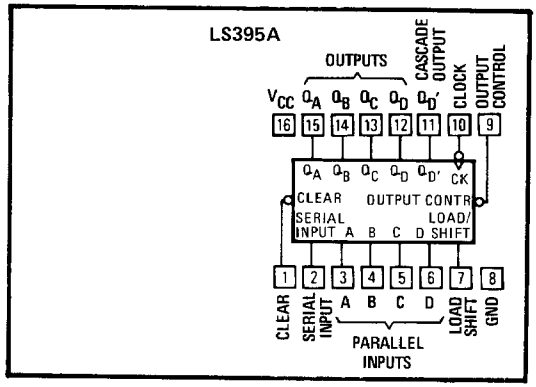
4-Bit Cascadable Shift Registers with 3-State Outputs

LS395A

FEATURES

- Three-State, 4-Bit, Cascadable, Parallel-In, Parallel-Out Registers
- Schottky-Diode-Clamped Transistors
- Low Power Dissipation . . . 75mW Typical (Enabled)
- Applications: N-Bit Serial-To-Parallel Converter
  N-Bit Parallel-To-Serial Converter
  N-Bit Storage Register
- Pin for pin compatible with LS395

PIN-OUT DIAGRAM



DESCRIPTION

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, load/shift, output control and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the reigsters is not affected. During the high-impedance mode, the output at $Q_{D'}$ is still available for cascading.

The 9LS/54LS395A is characterized for operation over the full military temperature range of −55°C to 125°C; the 9LS/74LS395A is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					3-STATE OUTPUTS				CASCADE
CLEAR	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL A B C D	Q_A	Q_B	Q_C	Q_D	OUTPUT Q_D
L	X	X	X	X X X X	L	L	L	L	L
H	H	H	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a b c d	a	b	c	d	d
H	L	H	X	X X X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X X X X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X X X X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D are not affected.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	25			25			ns
Setup time, high-level or low-level data, t_{setup}	20			20			ns
Hold time, high-level or low-level data, t_{hold}	10			10			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

Electrical Characteristics Over Recommended Free-Air Temperature Range (Unless Otherwise Noted)

Parameter	Test Conditions*			9LS/54LS			9LS/74LS			Unit
				Min	Typ**	Max	Min	Typ**	Max	
V_{IH}				2			2			V
V_{IL}						0.7			0.8	V
V_I	V_{CC}=MIN,	I_I=−18mA				−1.5			−1.5	V
V_{OH}	V_{CC}=MIN, V_{IL}=V_{IL}max,	V_{IH}=2V, I_{OH}=MAX		2.4	3.4		2.4	3.1		V
V_{OL}	V_{CC}=MIN, V_{IL}=V_{IL} max, V_{IH}=2V	Q_A, Q_B	I_{OL}=12mA		0.25	0.4		0.25	0.40	V
		Q_C, Q_D	I_{OC}=24mA					0.35	0.50	
		Q_D	I_{OL}=4mA		0.25	0.4		0.25	0.40	V
			I_{OL}=8mA					0.35	0.50	
I_{OZH}	V_{CC}=MAX, V_O=2.7V	V_{IH}=2V,	Q_A, Q_B Q_C, Q_D			20			20	μA
I_{OZL}	V_{CC}=MAX, V_O=0.4V	V_{IH}=2V,	Q_A, Q_B Q_C, Q_D			−20			−20	μA
I_I	V_{CC}=MAX,	V_I=7V				0.1			0.1	mA
I_{IH}	V_{CC}=MAX,	V_I=2.7V				20			20	μA
I_{IL}	V_{CC}=MAX,	V_I=0.4V				−0.4			−0.4	mA
I_{OS}†	V_{CC}=MAX			−15		−100	−15		−100	mA
I_{CC}††	V_{CC}=MAX,		Condition A		18	29		18	29	mA
			Condition B		15	25		15	25	

*For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

**All typical values are at V_{CC} = 5V, T_A = 25°C.

†Not more than one output should be shorted at a time.

††I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:

A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.

B. Output control and clock input grounded.

Switching Characteristics, V_{CC} = 5V Over Recommended Free-Air Temperature Range

Parameters	-55°C			+25°C			+125°C			Unit
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Test Conditions: C_L = 15pF, R_L = 2kΩ (See Fig. C, page 2-174)										
f_{max}				25	35					MHz
t_{PHL} Clear to output		27	40		23	35		27	40	ns
t_{PLH}		27	40		23	35		27	40	ns
t_{PHL}		24	35		20	30		24	35	ns
t_{PZH}		17	25		13	20		17	25	ns
t_{PZL}		28	41		24	36		28	41	ns
t_{PHZ}		15	22		11	17		15	22	ns
t_{PLZ}		19	27		15	23		19	27	ns
Test Conditions: C_L = 5.0pF, R_L = 2kΩ (See Fig. C, page 2-174)										
t_{HZ}		13	22		11	17		13	22	ns
t_{LZ}		18	27		15	23		18	27	ns
Test Conditions: C_L = 50pF, R_L = 2kΩ (See Fig. C, page 2-174)										
t_{PHL}		30	44		26	39		30	44	ns
t_{PLH}		30	44		26	39		30	44	ns
t_{PHL}		27	38		23	34		27	38	ns
t_{PZH}		20	29		18	24		22	27	ns
t_{PZL}		31	45		27	40		30	45	ns
t_{PHZ}		18	26		14	20		19	26	ns
t_{PLZ}		22	32		18	27		22	32	ns

Note: AC specification shown under -55°C and +125°C are for 9LS devices only. All 50pF specifications are for 9LS devices only.

LOGIC DIAGRAM