



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Aug.3.2005
Rev. 1.1	Revised STSOP Package Outline Dimension	Mar.26.2008
Rev. 1.2	Revised Test Condition of I_{SB1}/I_{DR} Revised V_{TERM} to V_{T1} and V_{T2} Revised FEATURES & ORDERING INFORMATION Lead free and green package available to Green package available	Apr.17.2009
	Deleted T_{SOLDER} in ABSOLUTE MAXIMUM RATINGS Added packing type in ORDERING INFORMATION	
Rev. 1.3	Revised PACKAGE OUTLINE DIMENSION in page 10	May.7.2010
Rev. 1.4	Revised ORDERING INFORMATION in page 11 Revised PACKAGE OUTLINE DIMENSION in page 9	Aug.25.2010

FEATURES

- Fast access time : 8/10/12/15ns
- Low power consumption:
Operating current : 110/100/90/80mA (TYP.)
Standby current : 1mA (TYP.)
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 28-pin 300 mil SOJ
28-pin 300 mil Skinny P-DIP
28-pin 8mm x 13.4mm STSOP

GENERAL DESCRIPTION

The LY6164 is a 65,536-bit high speed CMOS static random access memory organized as 8,192 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

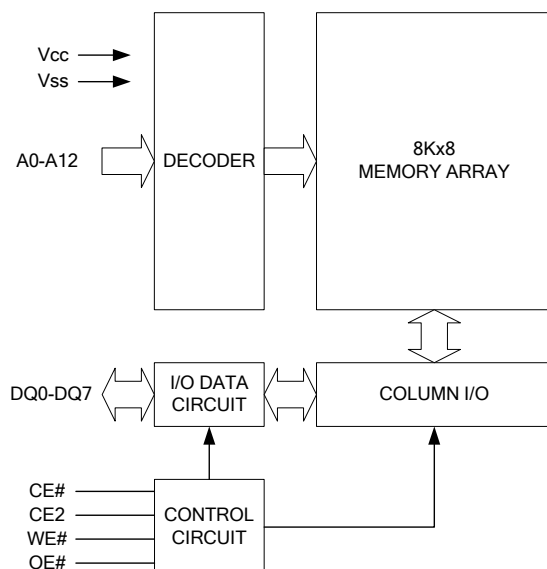
The LY6164 is well designed for high speed system applications, and particularly well suited for battery back-up nonvolatile memory application.

The LY6164 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

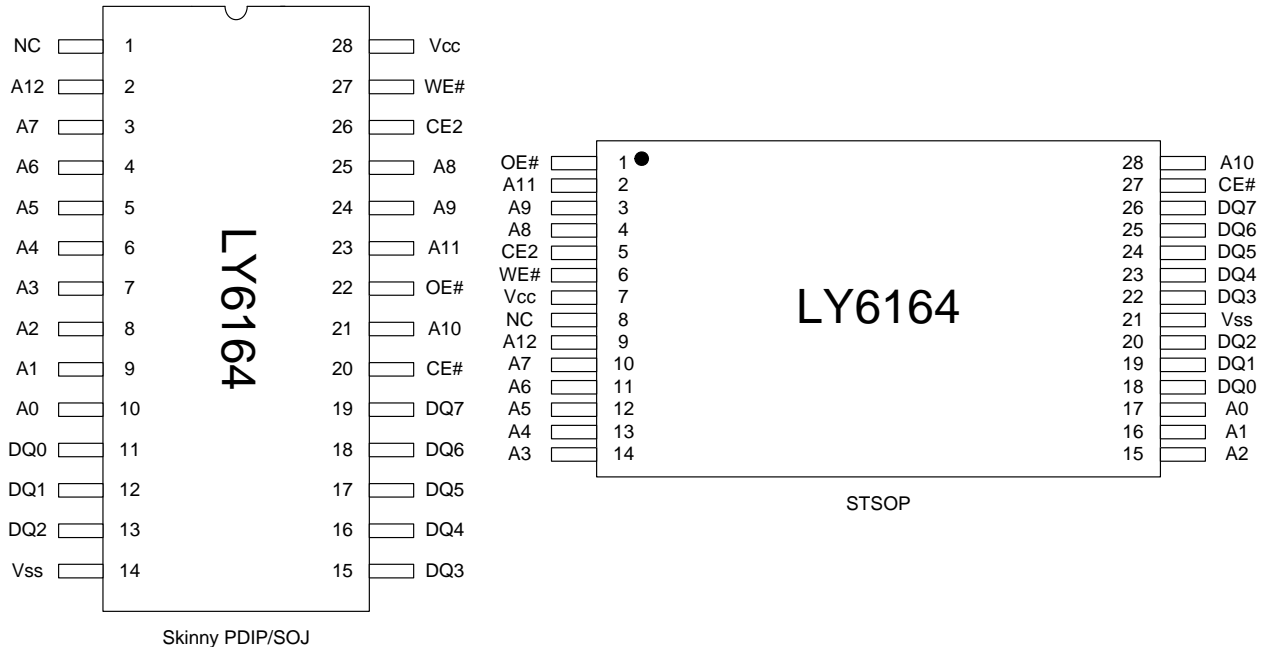
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{CC} ,TYP.)
LY6164	0 ~ 70°C	4.5 ~ 5.5V	8/10/12/15ns	1mA	110/100/90/80mA
LY6164(E)	-20 ~ 80°C	4.5 ~ 5.5V	8/10/12/15ns	1mA	110/100/90/80mA
LY6164(I)	-40 ~ 85°C	4.5 ~ 5.5V	8/10/12/15ns	1mA	110/100/90/80mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A12	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#, CE2	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to V _{cc} +0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	CE2	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	X	High-Z	I _{SB1}
	X	L	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	H	High-Z	I _{CC}
Read	L	H	L	H	D _{OUT}	I _{CC}
Write	L	H	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ⁴	MAX.	UNIT	
Supply Voltage	V _{CC}		4.5	5.0	5.5	V	
Input High Voltage	V _{IH} ¹		2.4	-	V _{CC} +0.5	V	
Input Low Voltage	V _{IL} ²		-0.5	-	0.8	V	
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	-1	-	1	μA	
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	-1	-	1	μA	
Output High Voltage	V _{OH}	I _{OH} = -1mA	2.4	-	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 2mA	-	-	0.4	V	
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} and CE2 = V _{IH} , I _{I/O} = 0mA Other pins at V _{IH} or V _{IL}	-8	-	110	190	mA
			-10	-	100	180	mA
			-12	-	90	160	mA
			-15	-	80	140	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} -0.2V or CE2 ≤ 0.2V Other pins at 0.2V or V _{CC} -0.2V	-	1	5	mA	

Notes:

- V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
- V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.
- Typical values are included for reference only and are not guaranteed or tested.
Typical values are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA



AC ELECTRICAL CHARACTERISTICS

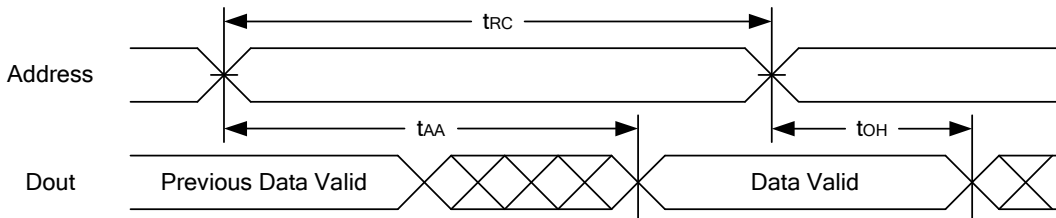
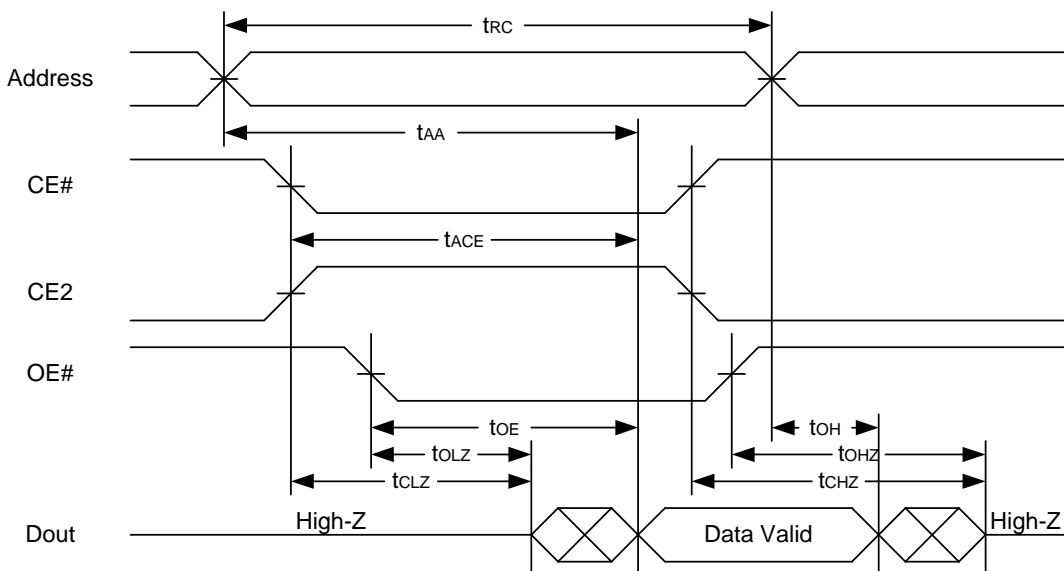
(1) READ CYCLE

PARAMETER	SYM.	LY6164-8		LY6164-10		LY6164-12		LY6164-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns

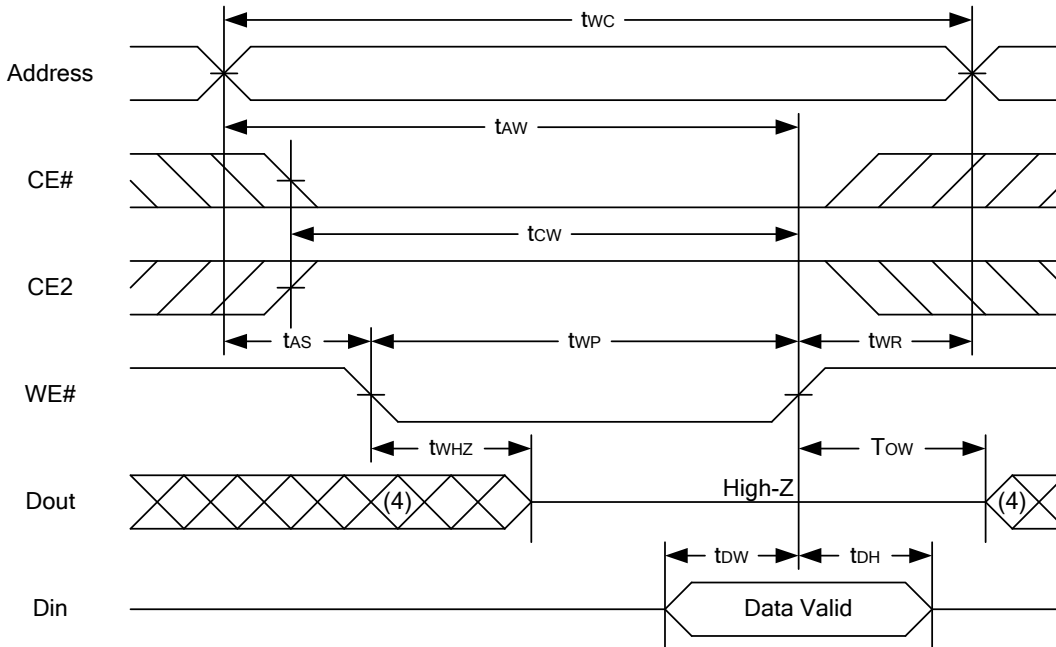
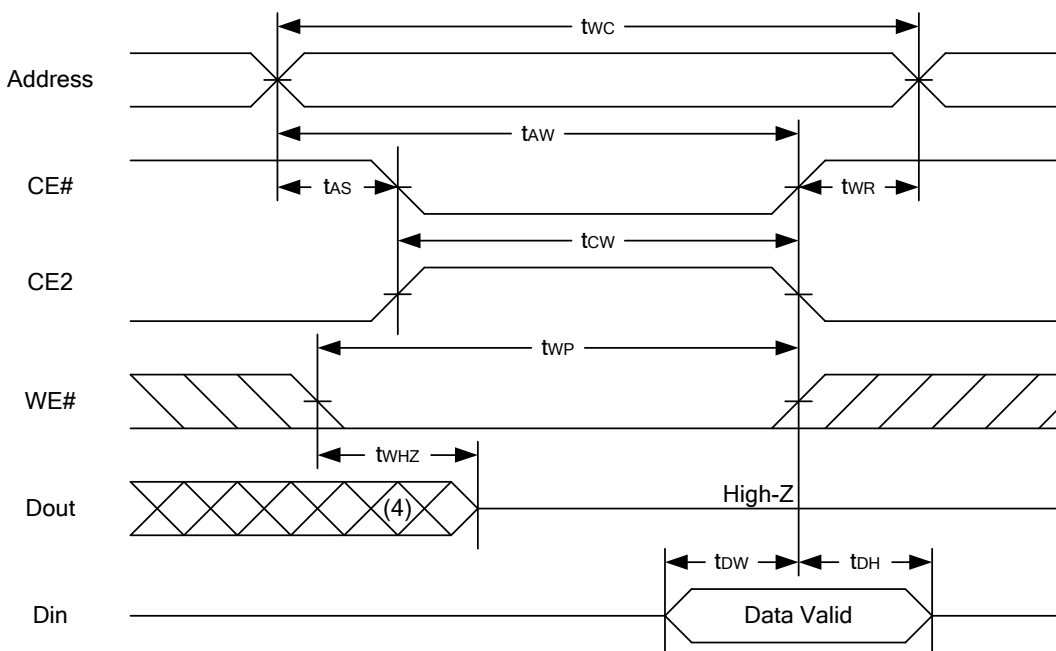
(2) WRITE CYCLE

PARAMETER	SYM.	LY6164-8		LY6164-10		LY6164-12		LY6164-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	6.5	-	8	-	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	6.5	-	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	1.5	-	2	-	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	5	-	6	-	7	-	8	ns

*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS
READ CYCLE 1 (Address Controlled) (1,2)

READ CYCLE 2 (CE# and CE2 and OE# Controlled) (1,3,4,5)

Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low., CE2 = high.
3. Address must be valid prior to or coincident with CE# = low, CE2 = high; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured ±500mV from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

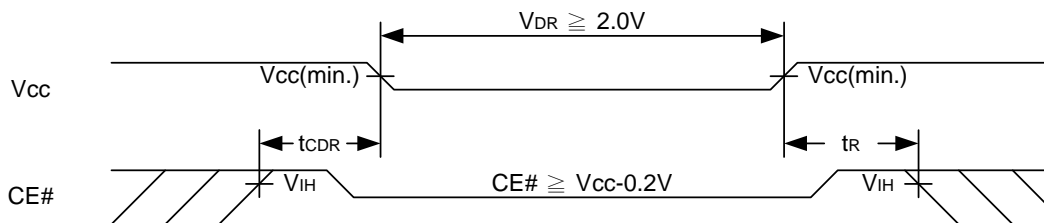
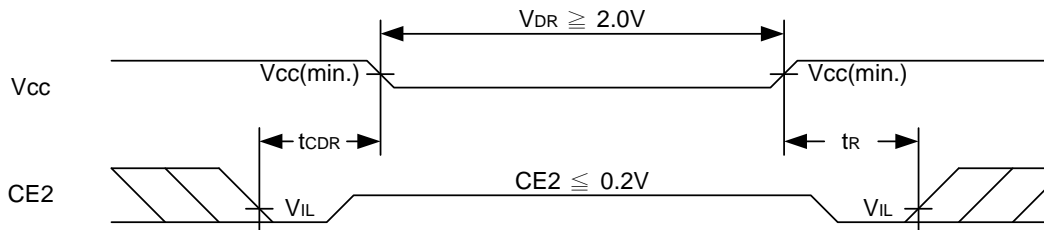
WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)

WRITE CYCLE 2 (CE# and CE2 Controlled) (1,2,5,6)

Notes :

1. WE#, CE# must be high or CE2 must be low during all address transitions.
2. A write occurs during the overlap of a low CE#, high CE2, low WE#.
3. During a WE#-controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition and CE2 high transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Vcc for Data Retention	V_{DR}	$CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$	2.0	-	5.5	V
Data Retention Current	I_{DR}	$V_{CC} = 2.0V$ $CE\# \geq V_{CC} - 0.2V$ or $CE2 \leq 0.2V$ Others at 0.2V or $V_{CC}-0.2V$	-	0.6	3	mA
Chip Disable to Data Retention Time	t_{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t_R		t_{RC*}	-	-	ns

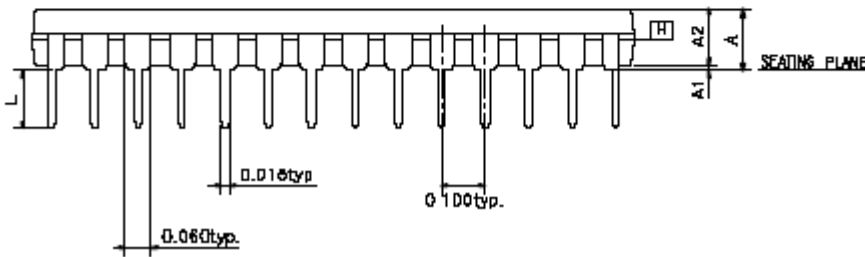
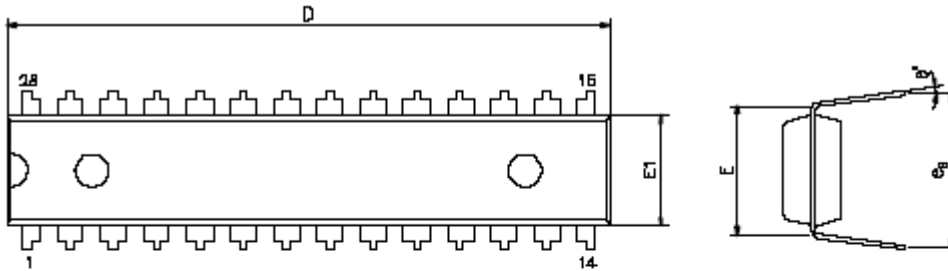
 t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM
Low Vcc Data Retention Waveform (1) (CE# controlled)

Low Vcc Data Retention Waveform (2) (CE2 controlled)




PACKAGE OUTLINE DIMENSION

28 pin 300 mil PDIP Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
θ_B	0.330	0.350	0.370
θ°	0	7	15

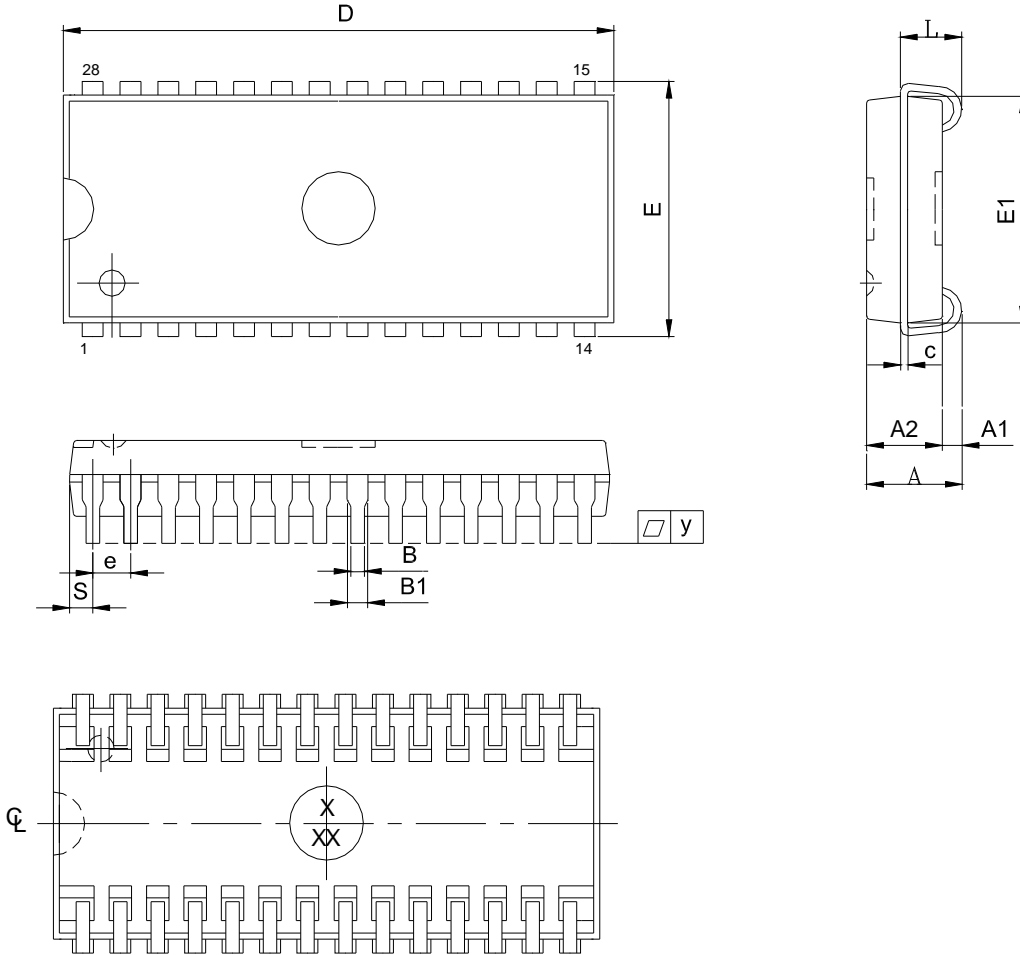
UNIT : INCH

NOTE:

1. JEDEC OUTLINE : MS-D15 AH

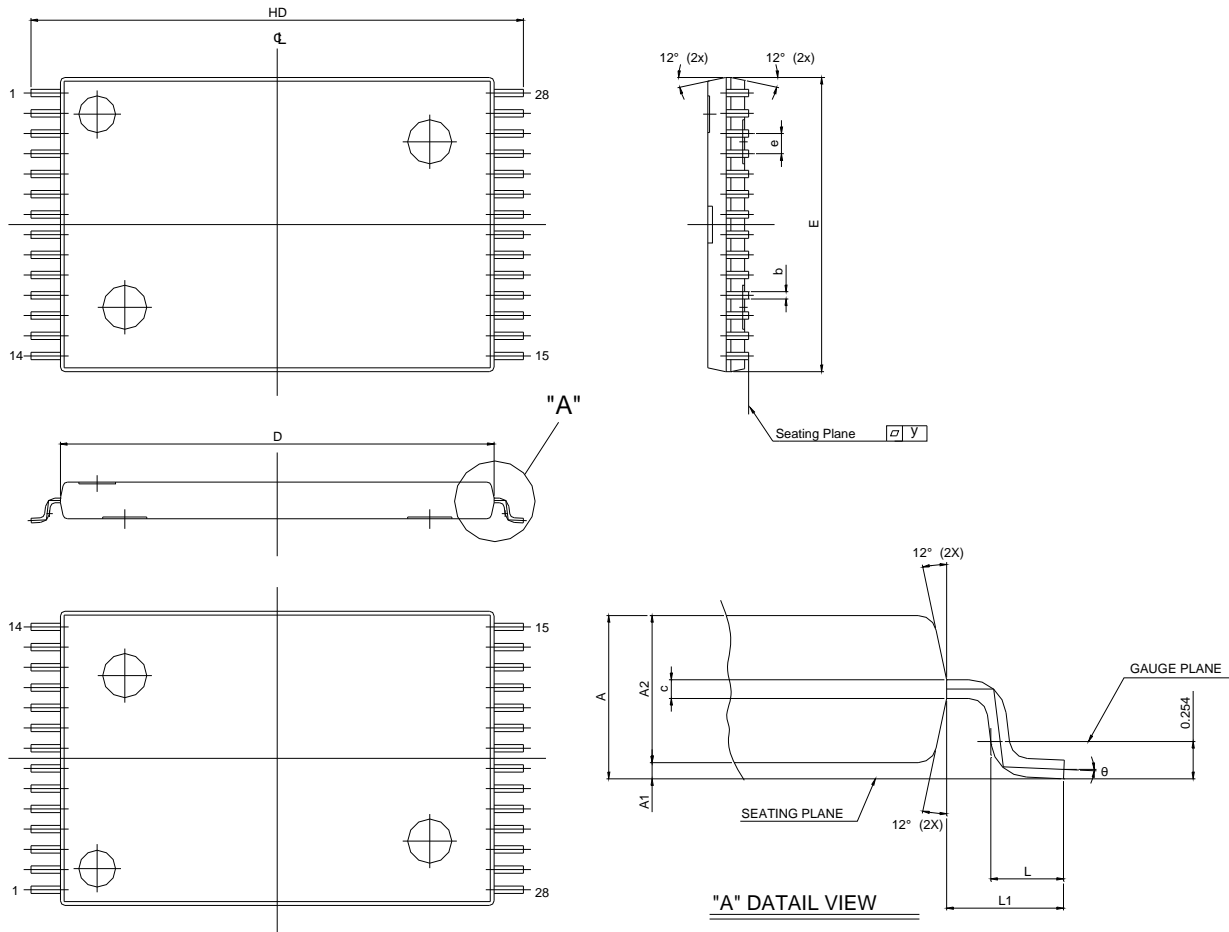


28-pin 300 mil SOJ Package Outline Dimension



SYM.	UNIT	INCH(REF)	MM(BASE)
A		0.140(MAX)	3.556(MAX)
A1		0.025(MIN)	0.635(MIN)
A2		0.100±0.015	2.540±0.381
B		0.018±0.004	0.457±0.102
B1		0.028±0.004	0.711±0.102
c		0.010±0.004	0.254±0.102
D		0.710±0.020	18.03±0.508
E		0.337±0.010	8.560±0.254
E1		0.300±0.005	7.620±0.127
e		0.050±0.006	1.270±0.152
L		0.087±0.010	2.210±0.254
S		0.045(MAX)	1.143(MAX)
Y		0.004(MAX)	0.102(MAX)

- Note : 1.S/E/D dimension is not including mold flash.
 2.The end flash in package lengthwise is not more than 10 mils each side.

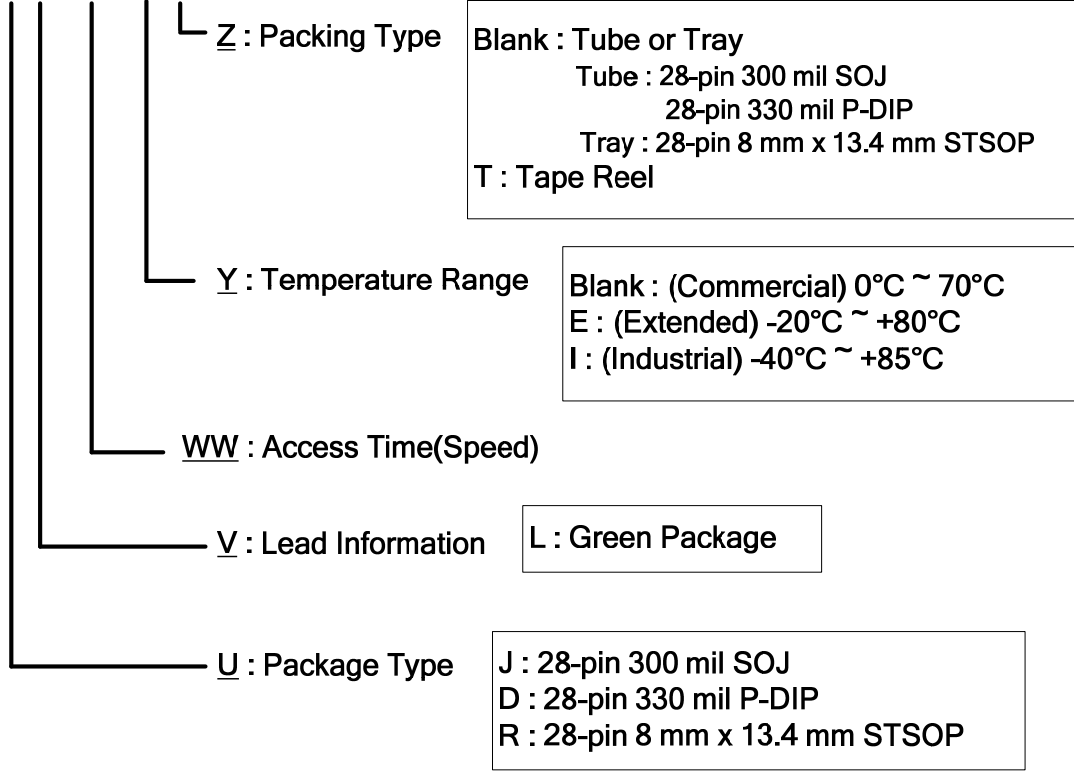
28 pin 8x13.4mm STSOP Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.07	0.15	0.23	0.003	0.006	0.009
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.60	11.80	12.00	0.457	0.465	0.472
E	7.80	8.00	8.20	0.307	0.315	0.323
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°



ORDERING INFORMATION

LY6164 U V - WW Y Z





Lyontek Inc.

LY6164

Rev. 1.4

8K X 8 BIT HIGH SPEED CMOS SRAM

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