

## 1000 MHz Quadrature Demodulator

### Description

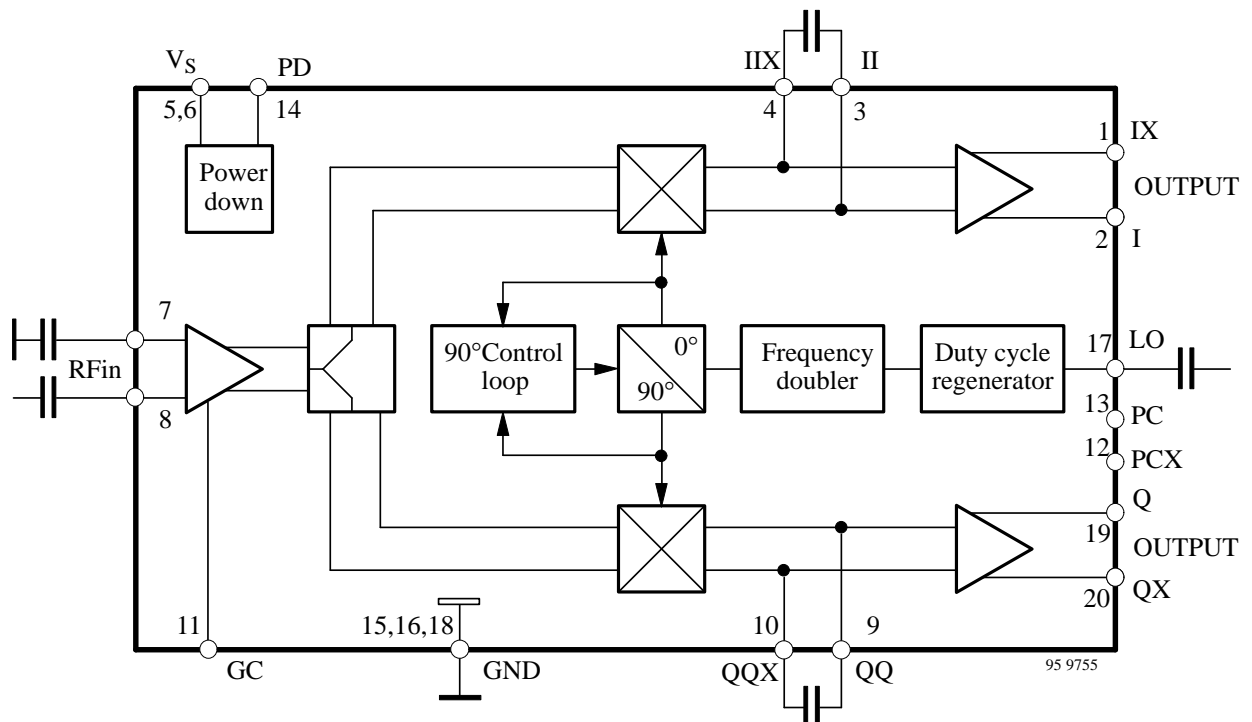
U2791B silicon monolithic integrated circuit is a quadrature demodulator that is manufactured using TELEFUNKEN's advanced UHF technology. This demodulator features a frequency range from 100 – 1000 MHz, low current consumption, selectable

gain, power down mode and is adjustment free. The IC is suitable for direct conversion and image rejection applications in digital radio systems up to 1 GHz such as cellular radio, cordless telephone, cable TV and satellite TV systems.

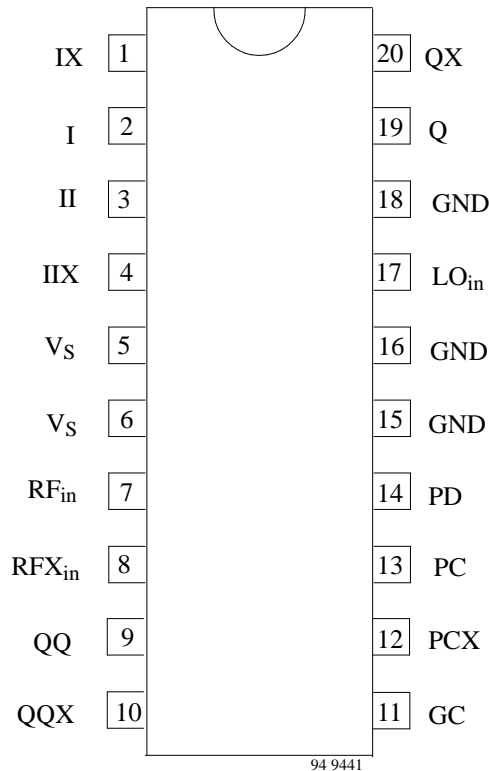
### Features

- Supply voltage 5 V (typ.)
- Very low power consumption 125 mW (typ.)
- Very good image rejection by means of phase control loop for precise 90° phase shifting
- Duty cycle regeneration for single ended LO input signal
- Low LO input level -10 dBm (typ.)
- LO – frequency from 100 MHz to 1 GHz
- Power down mode
- 25 dB gain control

### Block Diagram



## Pin Description



Pin	Symbol	Function
1	IX	IX output
2	I	I output
3	II	II low pass filter I
4	IIX	IIX low pass filter I
5	V <sub>S</sub>	Supply voltage
6	V <sub>S</sub>	Supply voltage
7	RF <sub>in</sub>	RF input
8	RFX <sub>in</sub>	RFX input
9	QQ	QQ low pass filter Q
10	QQX	QQX low pass filter Q
11	GC	GC gain control
12	PCX	PCX phase control
13	PC	PC phase control
14	PD	PD power down
15	GND	Ground
16	GND	Ground
17	LO <sub>in</sub>	LO input
18	GND	Ground
19	Q	Q output
20	QX	QX output

**Electrostatic sensitive device observe precautions for handling.**

## Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage Pins 5 and 6	V <sub>S</sub>	6	V
Input voltage Pins 7, 8 and 17	V <sub>i</sub>	0 to V <sub>S</sub>	V
Junction temperature	T <sub>j</sub>	125	°C
Storage temperature range	T <sub>stg</sub>	-40 to 125	°C

## Operating Range

Parameters	Symbol	Value	Unit
Supply voltage range Pins 5 and 6	V <sub>S</sub>	4.75 to 5.25	V
Ambient temperature range	T <sub>amb</sub>	-40 to 85	°C

## Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient SSO 20	R <sub>thJA</sub>	140	K/W

## Electrical Characteristics

Test conditions (unless otherwise specified);  $V_S = 5\text{ V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ , referred to test circuit  
 System impedance  $Z_O = 50\ \Omega$ ,  $\text{fiLO} = 950\text{ MHz}$ ,  $\text{PiLO} = -10\text{ dBm}$

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage range	Pins 5 and 6	$V_S$	4.75		5.25	V
Supply current	Pins 5 and 6	$I_S$		30		mA
<b>Power down mode, PD</b>						
“OFF”mode supply current	$V_{\text{PD}} \leq 0.5\text{ V}$ Pins 5, 6 $= 1.0\text{ V}$ Pin 14 Note 1	$I_{\text{SPD}}$		$\leq 1$ 20		$\mu\text{A}$
<b>Switch voltage</b> Pin 14						
“Power ON”		VPON	4			V
“Power DOWN”		VPOFF			1	V
<b>LO input, LO<sub>in</sub></b> Pin 17						
Frequency range		fiLO	100		1000	MHz
Input level	Note 2	PiLO	-12	-10	-5	dBm
Input impedance	See figure 6	ZiLO		50		$\Omega$
Voltage standing wave ratio	See figure 2	VSWRLO		1.2	2	
Duty cycle range		LODCR	0.4		0.6	
<b>RF input, RF<sub>in</sub></b>						
Noise figure (DSB) symmetrical output	@ 950 MHz Note 3 @ 100 MHz Pins 7 and 8	NF		12 10		dB
Frequency range	Pins 7 and 8	fiRF			>fiLO	
-1 dB input compression point	Pins 7 and 8 High gain Low gain	ICPHG ICPLG		-8 +3.5		dBm
Second order IIP	Note 4 Pins 7 and 8	IIP2HG		35		dBm
Third order IIP	Pins 7 and 8 High gain Low gain	IIP3HG IIP3LG		+3 +13		dBm
LO leakage	Pins 7 and 8 Symmetric input Asymmetric input	LOL		$\leq -60$ $\leq -55$		dBm
Input impedance	Pins 7 and 8 see figure 6	ZiRF		$500\ \Omega \parallel$ 0.8pF		

Note 1: During power down status a load circuitry with dc-isolation to GND is assumed otherwise a current of  $I \approx (V_S - 0.8\text{ V}) / R_I$  has to be added to the above power down current for each output I, IX, Q, QX.

Note 2: The required LO-Level is a function of the LO-frequency (see figure 3).

Note 3: Measured with input matching. For 950 MHz the optional transmission line T3 at the RF input may be used for this purpose. Noise figure measurements without using the differential output signal result in a worse noise figure.

Note 4: Using Pins 7 and 8 as a symmetric RF input, the second order IIP can be improved.

## Electrical Characteristics

Test conditions (unless otherwise specified);  $V_S = 5\text{ V}$ ,  $T_{\text{amb}} = 25^\circ\text{C}$ , referred to test circuit  
 System impedance  $Z_O = 50\ \Omega$ , fiLO = 950 MHz, PiLO = -10 dBm

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
<b>I/O outputs</b>	Emitter follower $I = 0.6\text{ mA}$	I, IX / Q, QX				
3-dB bandwidth w/o external C	Note 5 Pins 1, 2, 19 and 20	BW/Q	$\geq 30$			MHz
I/Q amplitude imbalance	Pins 1, 2, 19 and 20	AII/Q		$\leq \pm 0.2$		dB
I/Q quadrature error	Pins 1, 2, 19 and 20	QEI/Q		$\leq \pm 1.5$		Deg
I/Q maximum output swing	Pins 1, 2, 19 and 20 Symm. output $R_L > 5\text{ k}\Omega$	Max I/Q			2	V <sub>PP</sub>
DC output voltage	Pins 1, 2, 19 and 20	VOOUT		2.8		V
DC output offset voltage	Note 6 Pins 1, 2, 19 and 20	VOFSI/Q I/IX Q/QX		$\leq 30$		mV
Output impedance	Pins 1, 2, 19 and 20 see figure 6	Zout		50		$\Omega$
<b>Gain control, GC</b>						
Control range power gain, gain high/gain low	Note 7 Pin 11	GCR PGH/GGL		25 23/-2		dB
Switch voltage						
“Gain high”	Pin 11	GCVHigh			1	V
“Gain low”	Note 8 Pin 11	GCVLow				V
<b>Settling time, ST</b>						
Power “OFF” – “ON”		STON		< 4		$\mu\text{s}$
Power “ON” – “OFF”		STOFF		< 4		$\mu\text{s}$

Note 5: Due to test board parasitics this bandwidth is reduced and not equal for I, IX, Q, QX.

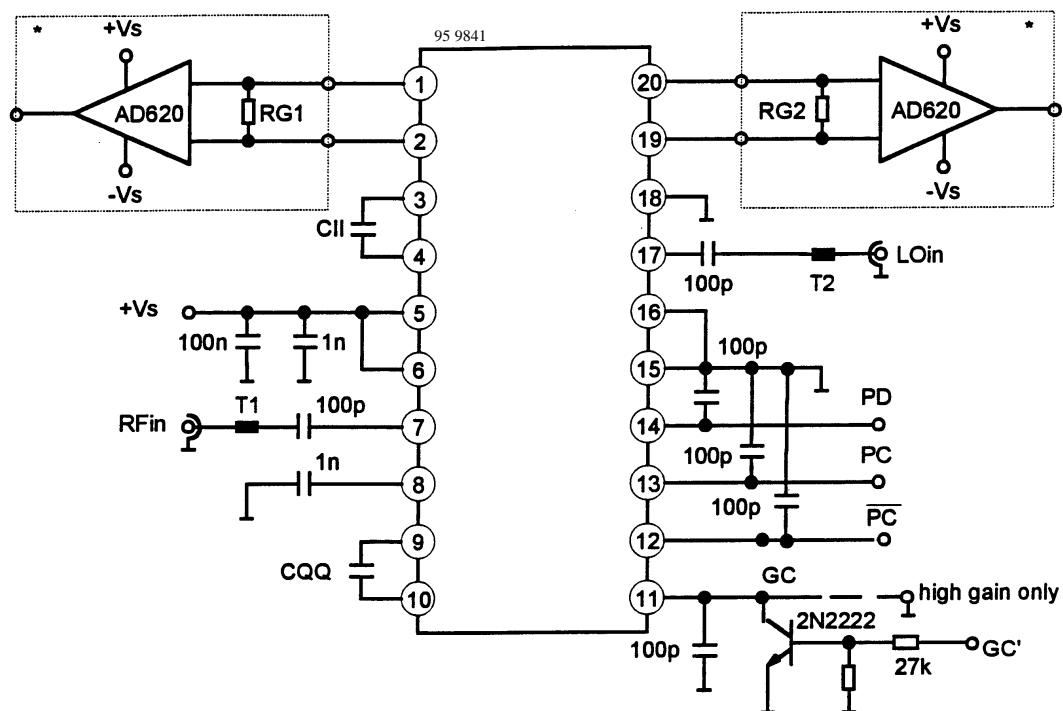
If symmetry and full bandwidth is required the low-pass Pins 3, 4, 9 and 10 should be isolated from the board.  
 The bandwidth of the I/Q outputs can be increased further by using a resistor between the Pins 3, 4, 9 and 10.  
 This resistors shunt the internal loads of  $R_I \sim 5.4\text{ k}\Omega$  The decrease in gain here has to be considered.

Note 6: Output emitter follower internal acurrent  $I = 0.6\text{ mA}$  allows only small voltage swing with a  $50\ \Omega$  load.  
 For low signal distortion the load impedance should be  $R_I \geq 5\text{ k}\Omega$ .

Note 7: Referred to the level of the output vector  $\sqrt{I^2 + Q^2}$ .

Note 8: The low gain status is achieved with an open or high ohmic Pin 11. A recommended application circuit for switching between high and low gain status is shown in figure 1.

## Test Circuit



\* optional for single ended tests (notice 3 dB bandwidth of AD620)

T1, T2 = transmission line  $Z_0 = 50 \Omega$

If no GC function is required, connect Pin 11 to GND.

For high and low gain status GC' is to be switched to GND respectively to  $V_S$ .

Figure 1.

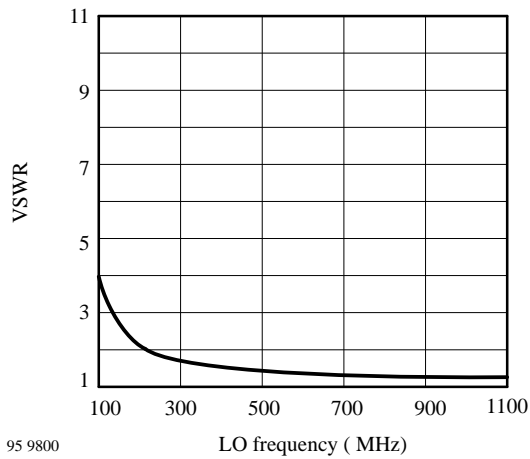


Figure 2. Typical VSWR frequency response of the LO input

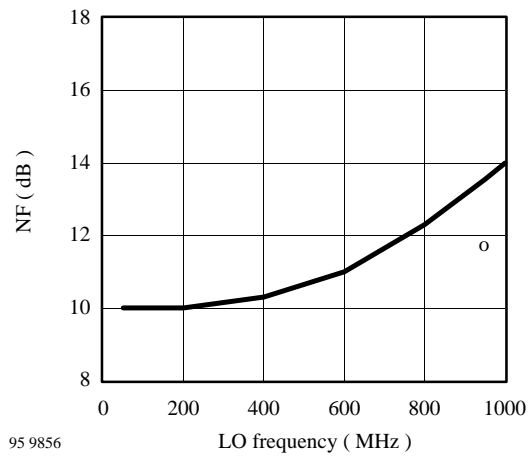


Figure 4. Noise figure vs. LO frequency; o: value at 950 MHz with RF input matching with T3

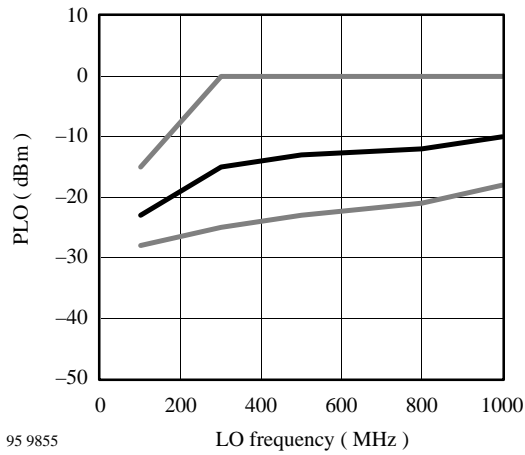


Figure 3. Typical suitable LO power range vs. frequency

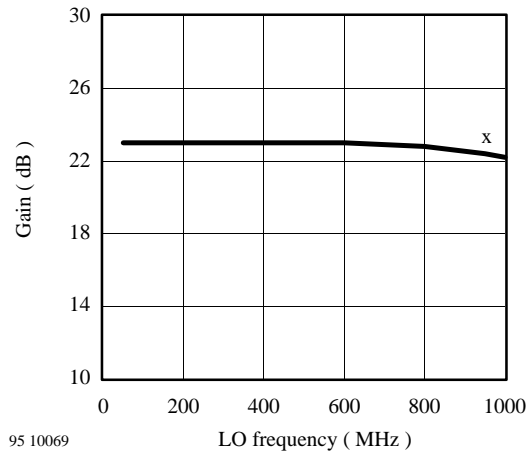


Figure 5. Gain vs. LO frequency, x: value at 950 MHz with RF input matching with T3

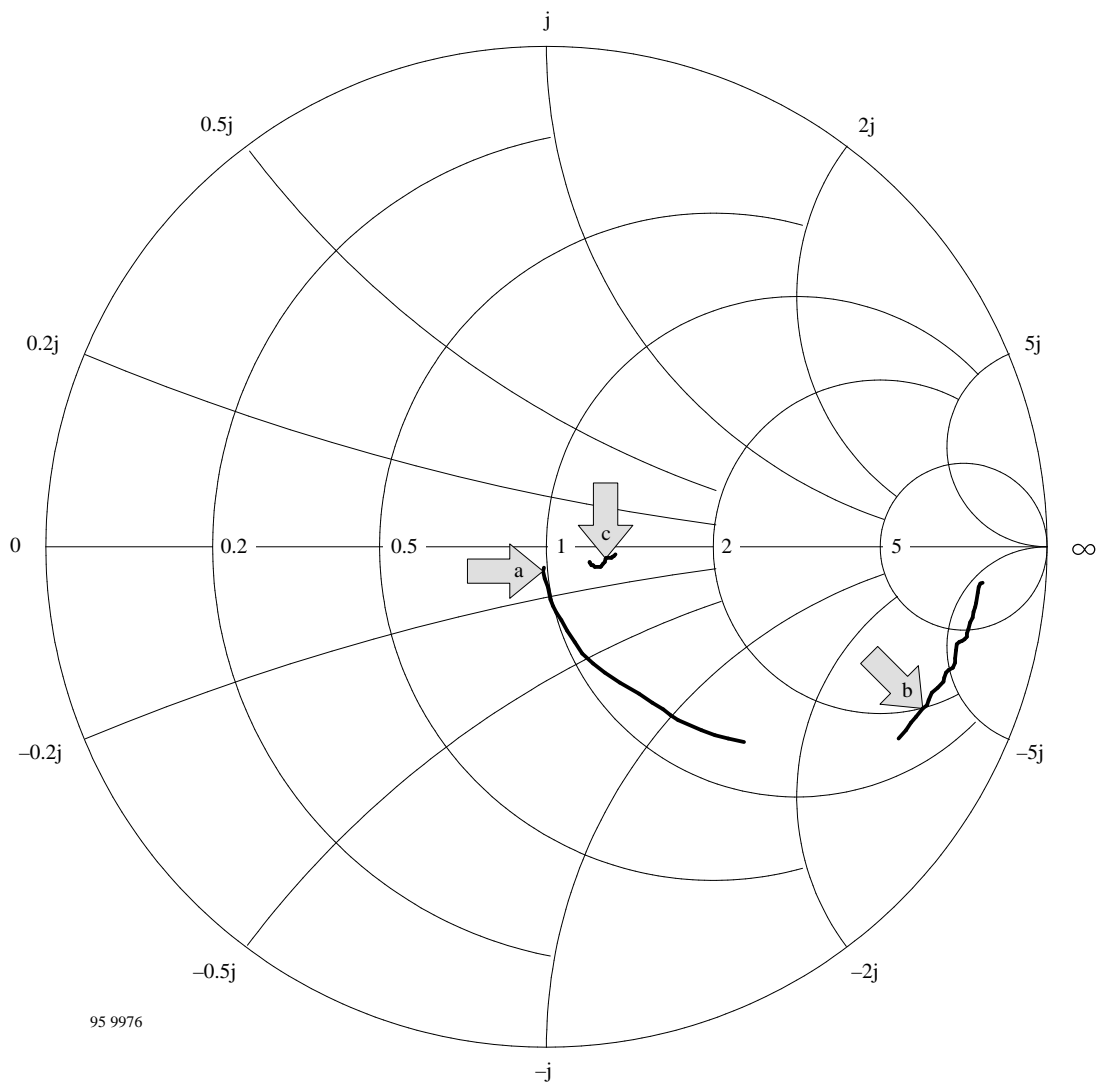
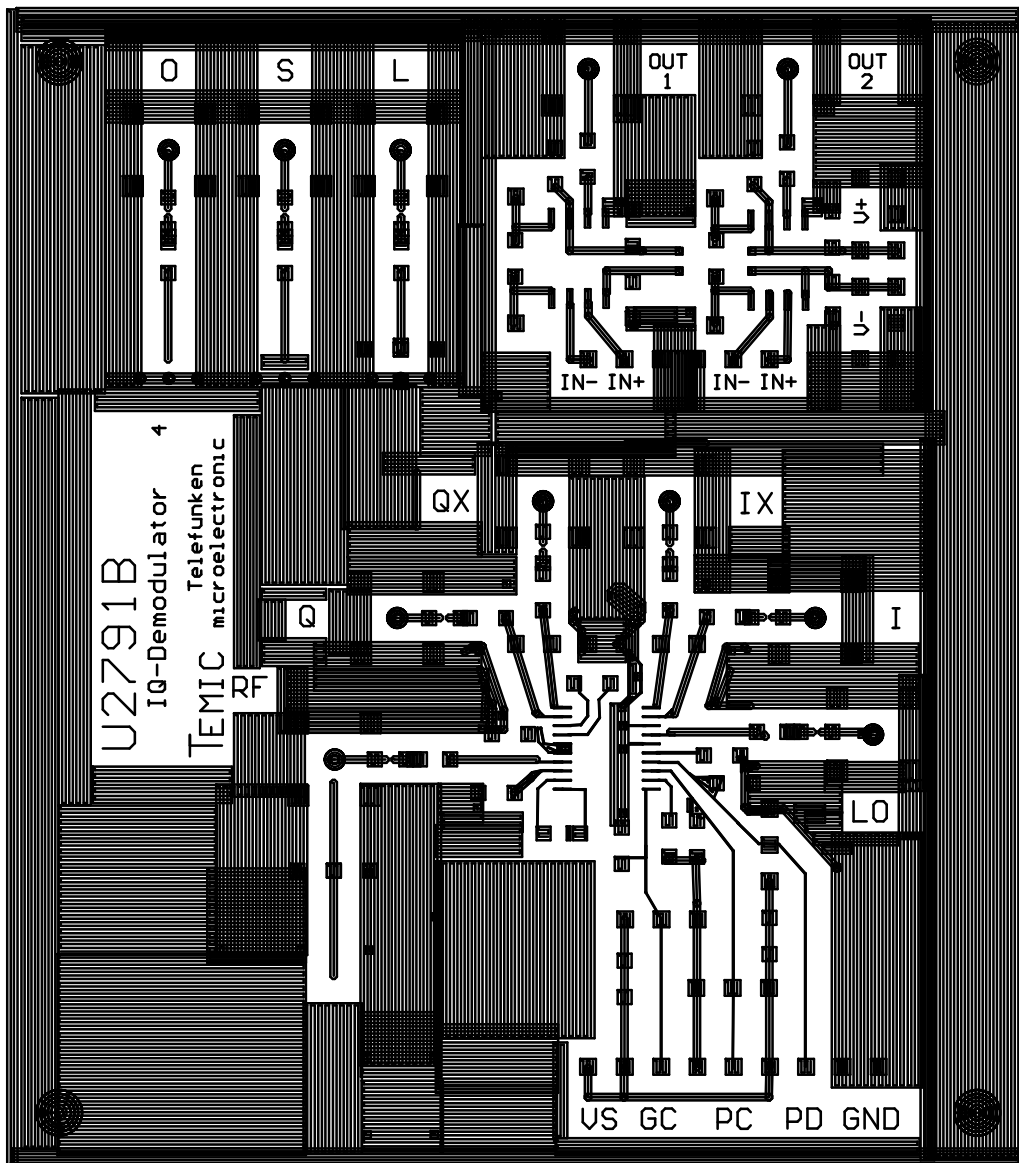


Figure 6. Typical S11 frequency response of the  
 a: LO input, LO frequency from 100 MHz to 1100 MHz, marker: 950 MHz  
 b: RF input, RF frequency from 100 MHz to 1100 MHz, marker: 950 MHz  
 c: I/Q outputs, baseband frequency from 5 MHz to 55 MHz, marker: 25 MHz

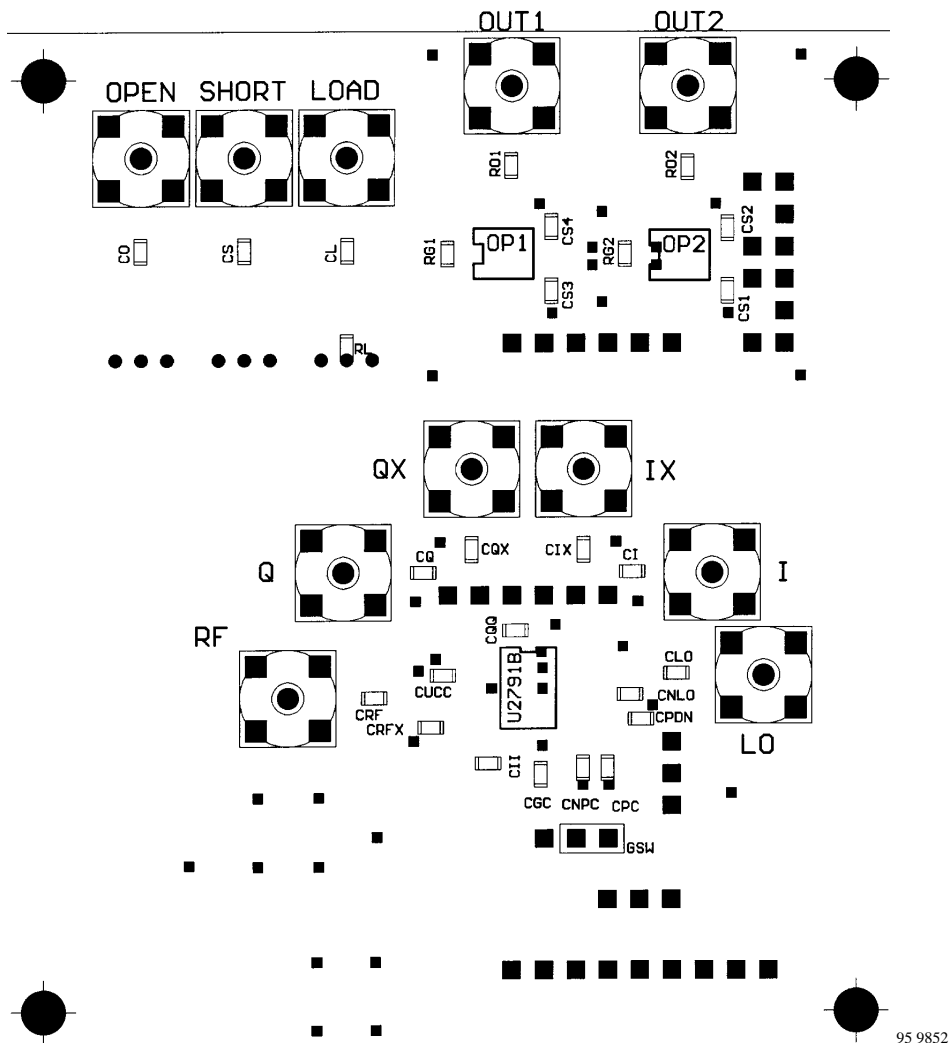
## Board Layout



94 9698



## Board Layout



95 9852

### External Components

CUCC	100 nF
CRFX	1 nF
CLO	100 pF
CNLO	0 $\Omega$
CRF	100 pF
CII, CQO	optional external lowpass filters
T3	transmission line for RF-input matching to connect optionally
CI, CIX,	optional for ac-coupling at
CQ, CQX	baseband outputs
CPDN	100 pF
CGC	100 pF
CPC	100 pF

CNPC	100 pF
GSW	gain switch

### Calibration Part

CO, CS, CL	100 pF
RL	50 $\Omega$

### Conversion to Single Ended Output

OP1, OP2	AD620
RG1, RG2	prog. gain, see datasheet, for 5.6 k $\Omega$ a gain of 1 to 50 $\Omega$ is achieved together with RD1 and RD2
RD1, RD2	450 $\Omega$
CS1, CS2	100 nF
CS3, CS4,	100 nF

## U2791B

### Description of Evaluation Board

Board material: epoxy;  $\epsilon_r = 4.8$ , thickness = 0.5 mm  
 transmission lines:  $Z_0 = 50 \Omega$

#### The board offers the following functions

- The test circuit for the U2791B:

- The supply voltage and the control inputs GC, PC and PD are connected via a plug strip. The control input voltages can be generated via external potentiometers; then the inputs should be ac-grounded (time requirements in burst-mode for power up have to be considered).
- The outputs I, IX, Q, QX are dc coupled via an plug strip or can be ac-connected via SMB plugs for high frequency tests e.g. noise figure or s-parameter measurement. The pins II, IIX, QQ, QQX allow user definable filtering with 2 external capacitors CII, CQQ.

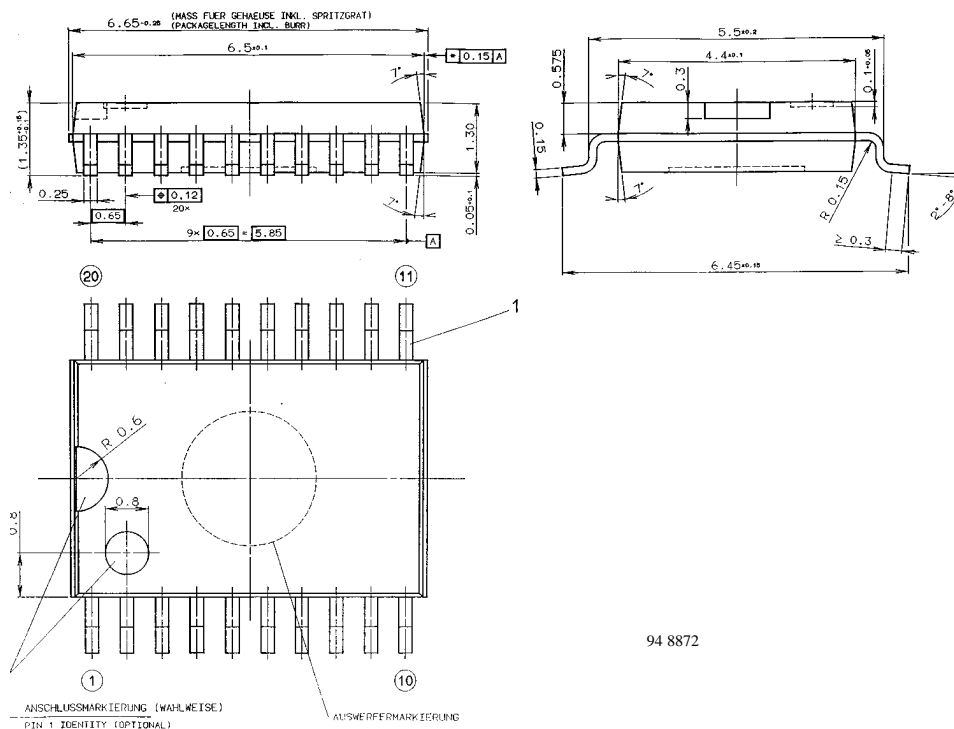
- Also the offsets of both channels can be adjusted with two pots or resistors.
- The LO- and the RF-inputs are ac-coupled and connected via SMB plugs. If transmission line T3 is connected to the RF-input and ac-grounded at the other end, gain and noise performance can be improved (input matching to  $50 \Omega$ ).
- The complementary RF-input is ac-coupled to GND (CRFX = 1 nF).
- A calibration part, which allows to calibrate an s-parameter analyzer directly to the in- and output-signal ports of the U2791B.
- For single ended measurements at the demodulator outputs, two OP's (e.g., AD620 or other) can be configured with programmable gain; together with an output-divider network  $RD = 450 \Omega$  to  $RL = 50 \Omega$ , direct measurements with  $50 \Omega$  load-impedances are possible at frequencies  $< 100$  kHz.

### Ordering Information

Extended Type Number	Package	Remarks
U2791B-FS	SS0 20	

### Dimensions in mm

Package: SSO 20



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