EXAR

Microprocessor Compatible, Double-Buffered, 12-Bit Digital-to-Analog Converter

FEATURES

- Lower Data Bus Feedthrough @ $\overline{CS}$ = 1
- Stable, More Accurate Segmented DAC Approach
- Ultra Stable
  - 0.2 ppm/°C Linearity Tempco
  - 2 ppm/°C Max. Gain Error Tempco
- Low Sensitivity to Amplifier V_{OS}
- C_{OUT1} = 80 pF at Full Scale, Gives Fastest Settling Times and Larger, Stable Bandwidth
- Lower Glitch Energy
- Four Quadrant Multiplication
- Low Feedthrough Error
- Low Power Consumption
- TTL/5 V CMOS Compatible
- Latch-Up Free
- Use MP1230A/1231A/1232A for New Designs

GENERAL DESCRIPTION

The MP1230/31/32 are 12-bit Digital-to-Analog Converters with 8/4 bit latched inputs for direct interface to the 8-bit data bus. All data loading and data transfer operations are identical to the WRITE cycle of a static RAM.

The MP1230 series uses a unique circuit which significantly reduces transients in the supplies during DATA bus transitions at $\overline{CS}$= 1.

The MP1230 series is manufactured using advanced thin film resistors on a double metal CMOS process. The MP1230 series incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal trimming. Outstanding features include:

- Stability: Both integral and differential linearity are rated at 0.2 ppm/°C typical, and monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. Scale factor is a low 2 ppm/°C maximum.

- Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at I_{OUT1} is a low 80pF / 40pF and 25pF / 65 pF at I_{OUT2} for the conditions of full scale/zero. This is over twice less than the National DAC1230 Series. Lower capacitance allows the MP1230 series to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available for a given amplifier loop gain because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.

- Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP1208/1230 series over conventional R-2R DACs, to 330µV per millivolt of offset.

ORDERING INFORMATION

Package Type	Temperature Range	Part No.	INL (LSB)	DNL (LSB)	Gain Error (% FSR)
Plastic Dip	-40 to +85°C	MP1231JN	±1	±1	±0.4
Plastic Dip	-40 to +85°C	MP1230KN	±1/2	±3/4	±0.4
Plastic Dip	-40 to +85°C	MP1232HN	±2	±2	±0.4
SOIC	-40 to +85°C	MP1231JS	±1	±1	±0.4
Ceramic Dip	-40 to +85°C	MP1231AD	±1	±1	±0.4
Ceramic Dip	-40 to +85°C	MP1230BD	±1/2	±3/4	±0.4
Ceramic Dip	-40 to +85°C	MP1232ZD	±2	±2	±0.4
Ceramic Dip	-55 to +125°C	MP1231SD*	±1	±1	±0.4

*Contact factory for non-compliant military processing