

FUNCTIONAL BLOCK DIAGRAM

Refer to the functional block diagram in Figure 2, below, and the Pin Description Table on page 3.

Power is transferred to the transformer primary by the N-MOSFET, driven by the MOSFET gate driver out of pin NDR. The P-MOSFET resets the primary field, driven by pin PDR. The usual design results in approximately 50% duty cycle at full lamp intensity. Terminating the NDR signal earlier than the full brightness lamp pulse width performs lamp dimming, using the analog dimming. The voltages on pins HCLMP and LCLMP set a threshold voltage for the ramp comparator setting the maximum duty cycle for NDR.

A pulse generator circuit creates the clock signal with the frequency determined by an external, constant current setting resistor (RT) and timing capacitor (CT).

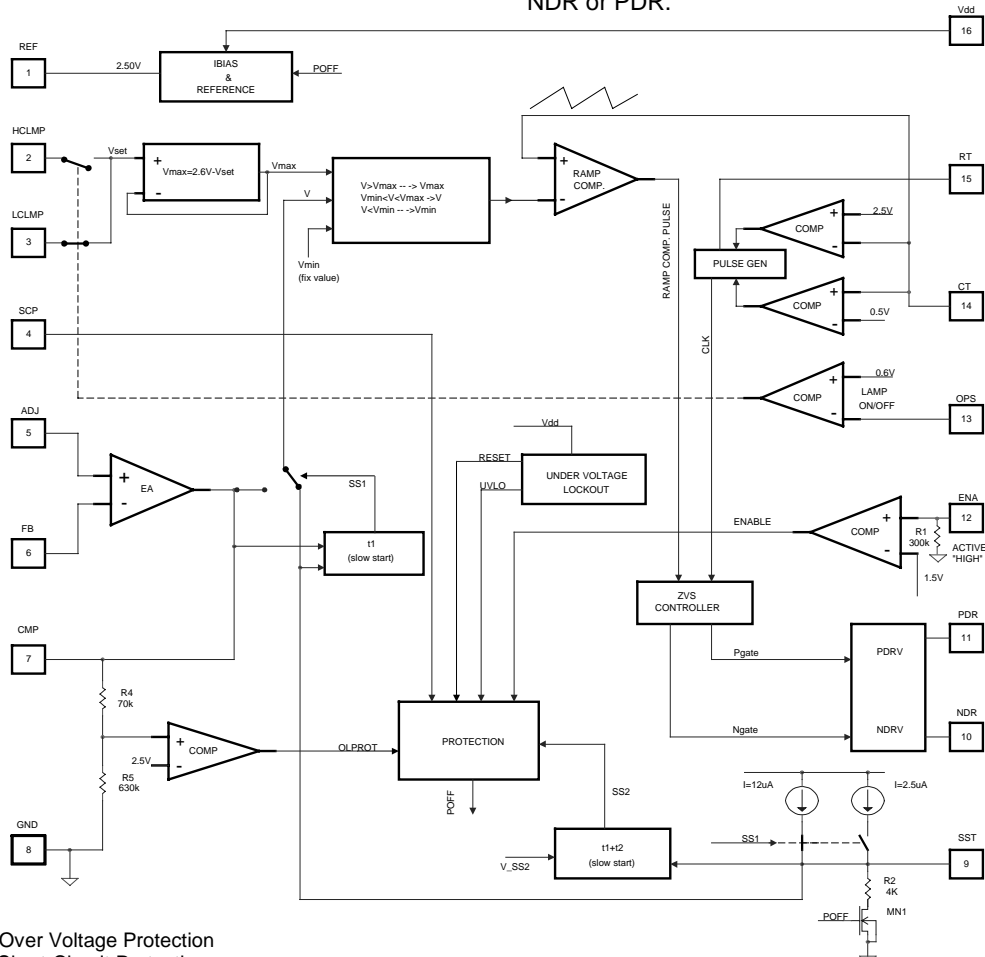
The “soft-start” circuit ensures a reliable and long lamp life starting condition.

“Soft start” gradually increases the energy delivered to the secondary.

When the OZ965 is enabled at pin ENA, the capacitor on pin SST determines the duration of the “soft-start” period, gradually increasing the NDR pulse width to the regulated brightness. The “soft-start” period provides sufficient time for the lamp to ignite.

For system reliability there are several circuit protections provided. To ensure a controlled output, the secondary current is monitored on pin FB and is compared to a reference voltage on pin ADJ. The NDR signal is shortened or lengthened dependent upon this feedback. Protection is provided by the resultant signal, CMP, monitoring for a lamp removal condition. Short circuit protection is provided at pin SCP. The OPS signal selects either HCLMP or LCLMP providing current protection against an “Open Lamp” condition at start-up. The OPS signal also allows adjustment to different transformer models.

To reduce power dissipation, the switch (MOSFET) drive signals are “break-before-make” with a short, fixed off time between activation of NDR or PDR.



Note:
 OVP – Over Voltage Protection
 SCP – Short-Circuit Protection
 UVL – Under Voltage Lockout

Figure 2. Functional Block Diagram

PIN DESCRIPTION

Names	Pin No.	I/O	Description
REF	1	O	Reference voltage output. Nominal voltage is 2.5 V.
HCLMP	2	I	Clamping maximum duty cycle under normal operation.
LCLMP	3	I	Clamping maximum duty cycle under open-lamp condition.
SCP	4	I	Short-circuit protection input ($V_{TH}=0.6V$)
ADJ	5	I	Reference voltage input for dimming control.
FB	6	I	Current sense feedback.
CMP	7	O	Compensation for the current sense feedback.
GND	8	GND	Ground.
SST	9	I	Soft-start ensures lamp current pulses gradually increases to its normal value
PDR	10	O	Gate drive output for the P-MOSFET.
NDR	11	O	Gate drive output for the N-MOSFET.
ENA	12	I	Enable input, active high ($V_{TH}=1.5V$)
OPS	13	I	Output current sense ($V_{TH}=0.6V$)
CT	14	I/O	Timing capacitor. CT and RT set the clock frequency.
RT	15	I/O	Timing resistor. $Fosc = 1.91 / (Rt \cdot Ct)$
VDD	16	PWR	Supply voltage input.

ABSOLUTE MAXIMUM RATINGS

VDD	5.5V
GND	+/- 0.3V
Logic inputs	-0.3 V to VDD+0.3V

	OZ965	OZ965I
Power dissipation		
- 16-pin SOP	.720W	.580W
- 16-pin TSSOP	.690W	.550W
Thermal Impedance		
- 16-pin SOP	111°C/W	111°C/W
- 16-pin TSSOP	115°C/W	115°C/W

	OZ965	OZ965I
Operating temp.	0°C to 70°C	-40°C to 85°C

Operating junction temp.	150°C
Storage temp.	-55°C to 150°C

RECOMMENDED OPERATING RANGE

VDD	5.0 V +/- 5%
Fosc	30 KHz to 200 KHz
Rosc	50 k to 150 k

FUNCTIONAL SPECIFICATIONS

Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
4.75 V < VDD < 5.25 V						
Reference Voltage						
Nominal voltage	Vref	I _{load} = 0.1 mA,	2.37	2.50	2.63	V
Line regulation			-	6	-	mV/V
Load regulation		I _{load} = 0.2 mA to 1.0 mA	-	1	-	mV/mA
Oscillator						
Initial accuracy	fosc	Ct = 470 pF, Rt = 49.9 k		81		KHz
Ramp peak			-	2.54	-	V
Ramp valley			-	0.48	-	V
Temp. stability		TA = -40°C to 85°C	-	-	200	ppm/°C
Error Amplifier						
Input bias current		ADJ=FB=2.0 V	-	0.25	-	uA
Input offset voltage		VFB = 4.0 V		5	10	mV
Input voltage range			0	-	VDD-1.5	V
Open loop voltage gain			-	65	-	dB
Unity gain bandwidth			-	1.5	-	MHz
Power supply rejection			-	60	-	dB
Under-Voltage Lockout						
Positive-going threshold voltage			See Table 1, page 5			
Negative-going threshold voltage			See Table 1, page 5			
Supply						
Supply current - Enable Low	I _{OFF}		-	195	-	μA
Supply current - Enable High	I _{ON}	VDD = 5.0 V	-	1.0	-	mA
NDR output						
Output high voltage	V _{OH}	I _{source} = 10 mA, VDD = 5V	-	4.75	-	V
Output low voltage	V _{OL}	I _{sink} = 10 mA, VDD = 5V	-	0.25	0.5	V
Output resistance	R _{OUT}		-	10	-	Ω
PDR output						
Output high voltage	V _{OH}	I _{source} = 10 mA, VDD = 5V	-	4.7	-	V
Output low voltage	V _{OL}	I _{sink} = 10 mA, VDD = 5V	-	0.5	-	V
Output resistance	R _{OUT}		-	15	-	Ω
Break-Before-Make						
Qn off to Qp on delay	T _{HL}		-	250	-	ns
Qp off to Qn on delay	T _{LH}		-	220	-	Ns
High Clamp						
Duty cycle of NDR	HCLMP	OPS=1 V, V _{HCLMP} =0V	92	94	96	%
		OPS=1 V, V _{HCLMP} =1.8V	-	14	-	
Low Clamp						
Duty cycle of NDR	LCLMP	OPS=0 V, V _{LCLMP} =0V	92	94	96	%
		OPS=0 V, V _{LCLMP} =1.8V	-	14	-	
Max. / Min. Duty cycle						
Duty cycle of NDR			6	-	95	%

Parameter	Test Conditions	OZ965				OZ965I			
		Limits			Unit	Limits			Unit
		Min	Typ	Max		Min	Typ	Max	
Under-Voltage Lockout									
Positive-going threshold voltage	4.75V < VDD < 5.25V	-	3.9	4.3	V	-	3.9	4.5	V
Negative-going threshold voltage		3.2	3.4	-	V	3.0	3.4	-	V

Table 1. Under-Voltage Lockout for OZ965 and OZ965I

PACKAGE INFORMATION

