ECL DIGITAL DELAY LINES

E10 SERIES - ECL10K INTERFACED

E100 SERIES - ECL100K INTERFACED

RESISTORS•CAPACITORS•COILS•DELAY LINES

RoHS Term.W is RoHS compliant & 260°C compatible

- Industry's widest selection! 5nS - 200nS (500nS avail.)
- Economical cost, prompt delivery
- Fast 2nSec rise time typical
- Standard 16 pin DIP on ECL 10K, 24 pin DIP on ECL 100K
- Surface mount design available
- Delay Line Application Guide available
- High-speed CMOS design available

TEST CONDITIONS @ 25°C

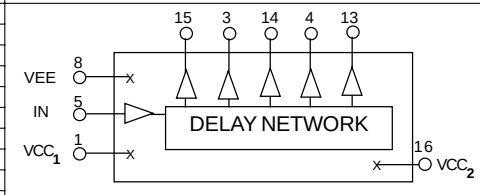
Pulse Width	2X Total Delay
Pulse Spacing	5X Total Delay
Pulse Amplitude	-1.0V provided by open emitter ECL 10K gate
Supply Voltage (VEE)	5.2 VDC ECL10K, -4.5 VDC EC 100K
Ground (VCC)	0V

ECL10K (ECL100K) outputs connected to external pull down 100Ω (50Ω) resistor to -2V.
Total Delay and Tap tolerance: ±5% or ±1nS, whichever is greater.

TYPE E105 - ECL 10K 5 TAP

Total Delay (nS)	Tap Delay (nS)
10	2
15	3
20	4
25	5
30	6
40	8
50	10
60	12
80	16
100	20

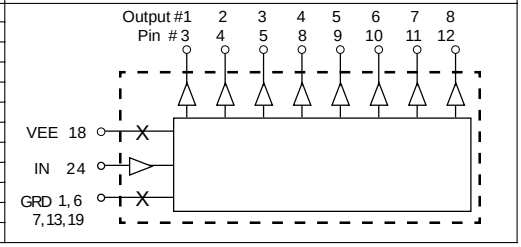
SCHEMATIC



TYPE E1008 - ECL 100K 8 TAP

Total Delay (nS)	Tap Delay (nS)
8	1
16	2
24	3
32	4
40	5
48	6
56	7
64	8
72	9
80	10
160	20
200	25

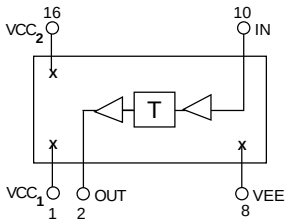
SCHEMATIC



TYPE E101 - ECL 10K SINGLE OUTPUT

Delay (nS)
5
10
15
20
25
50
75
100

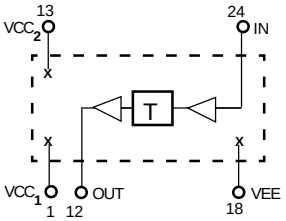
SCHEMATIC



TYPE E1001 - ECL 100K SINGLE OUTPUT

Delay (nS)
5
10
15
20
25
50
75
100
150
200

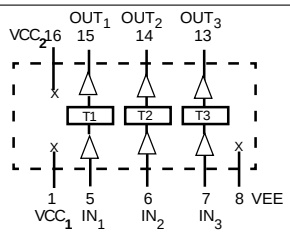
SCHEMATIC



TYPE E103 - ECL10K 3 INDEPENDENT DELAYS*

Delay(nS)
5
10
15
20
25
50

SCHEMATIC

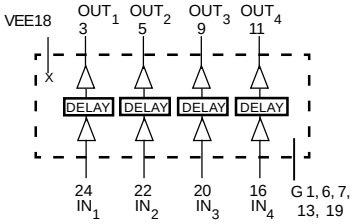


***Also available in a double delay output**

TYPE E1004 - ECL100K 4 INDEPENDENT DELAYS

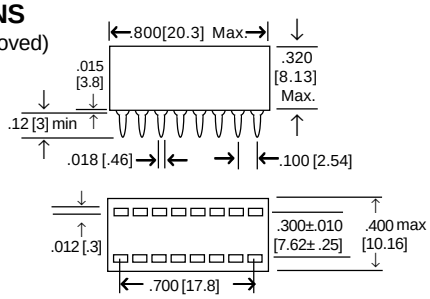
Delay (nS)
5
10
15
20
25
50
75
100

SCHEMATIC



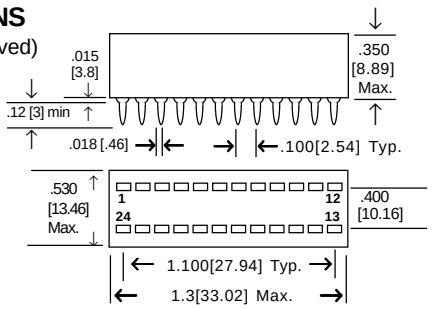
10K ECL DIMENSIONS

(unused pins may be removed)



100K ECL DIMENSIONS

(unused pins may be removed)



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