

## 55-60GHz Low Noise / Medium Power Amplifier

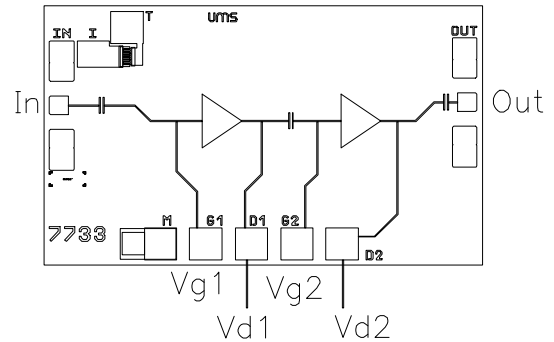
### GaAs Monolithic Microwave IC

*preliminary*

#### Description

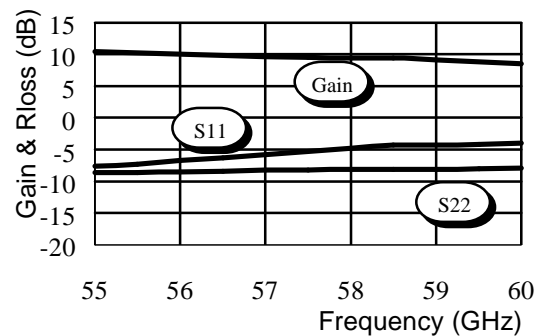
The CHA2157 is a two stages low noise and medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a HEMT process, 0.15µm gate length, via holes through the substrate, air bridges and electron beam gate lithography. It is available in chip form.



#### Main Features

- 3.5 dB noise figure
- 10 dB ± 1dB gain
- 15 dBm output power (-1dB gain comp.)
- DC power consumption, 80mA @ 3.3V
- Chip size : 1.71 x 1.04 x 0.10 mm



Typical on Wafer Measurements

#### Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	55		60	GHz
G	Small signal gain	8	10	12	dB
NF	Noise figure		3.5	4.5	dB
P1dB	Output power at 1dB gain compression	13	15		dBm
Id	Bias current		80	150	mA

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

## Electrical Characteristics for Broadband Operation

Tamb = +25°C, Vd = 3.3V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	55		60	GHz
G	Small signal gain (1)	8	10	12	dB
ΔG	Small signal gain flatness (1)		±1.0	±2.0	dB
Is	Reverse isolation (1)	20	25		dB
NF	Noise figure		3.5	4.5	dB
P1dB	CW output power at 1dB compression (1)	13	15		dBm
VSWRin	Input VSWR (1)		3.0:1	6.0:1	
VSWRout	Output VSWR (1)		3.0:1	6.0:1	
Vd	DC Voltage		3.3	3.8	V
Id	Bias current		80	150	mA

(1) These values are representative for CW on-wafer measurements that are made without bonding wires at the RF ports.

A wire bond of typically 0.1 to 0.15 nH will improve the input and output matching.

## Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.0	V
Id	Drain bias current	150	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Pin	Maximum peak input power overdrive (2)	TBD	
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +155	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

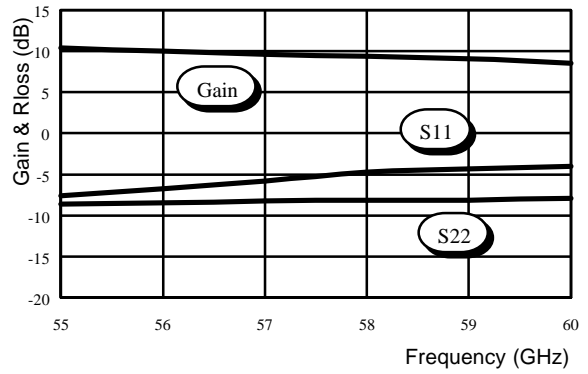
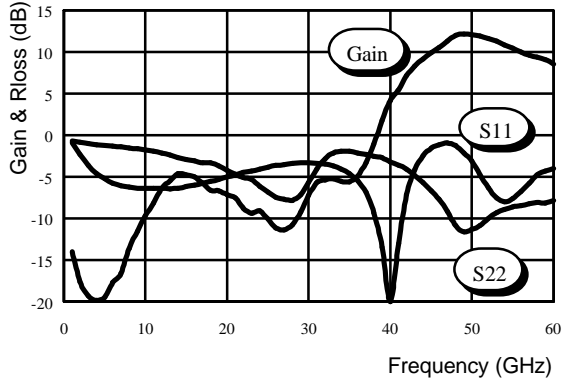
(2) Duration < 1s.

**Typical On Wafer Scattering Parameters**Bias Conditions :  $V_d = +3.3V$ ,  $V_{g1} = V_{g2}$  to have  $I_d = 80 \text{ mA}$ 

F(GHz)	S11 dB	S11 deg	S12 dB	S12 deg	S21 dB	S21 deg	S22 dB	S22 deg
15	-6,19	168,5	-53,85	104,2	-4,75	-110,1	-2,94	146,8
16	-6,01	163,4	-53,05	83,1	-5,02	-126	-3,07	142,5
17	-5,78	158,3	-55,51	61,9	-5,8	-141,7	-3,32	138,2
18	-5,57	152,8	-63,53	136,7	-6,59	-154,4	-3,34	134,5
19	-5,32	148,7	-49,37	58,7	-6,68	-164,3	-3,7	127,7
20	-5,04	142,7	-51,91	58,7	-7,14	-174	-4,2	123,4
21	-4,8	137,4	-51,32	48,4	-7,51	172,8	-4,71	120,3
22	-4,5	131,6	-52,83	40,4	-8,77	162,3	-5,05	118
23	-4,32	125,4	-50,9	67	-9,37	162,4	-5,33	114
24	-4,06	119,8	-49,33	39,6	-9,09	150,7	-6,14	111,7
25	-3,83	113,1	-49,97	36,3	-10,11	142,7	-6,85	111,1
26	-3,65	106,5	-49,38	37,1	-11,13	139,8	-7,43	113,4
27	-3,56	99,7	-47,44	39,9	-11,39	143,2	-7,66	116,1
28	-3,42	93,1	-45,59	23,7	-10,79	145,5	-7,83	120,6
29	-3,33	85,6	-46,24	25	-9,24	145,2	-7,15	127,2
30	-3,32	78,1	-43,98	12,4	-7,26	139,8	-5,72	129,5
31	-3,35	70,4	-42,56	2	-5,66	125,3	-4,07	126,3
32	-3,47	62,2	-41,07	-12,4	-5,35	110,7	-2,81	117,8
33	-3,69	53,6	-40,29	-28,3	-5,21	98,9	-2,13	107,8
34	-4,05	44,7	-40,08	-46,4	-5,56	91,8	-1,91	97,8
35	-4,58	35	-40,8	-63,2	-5,61	88,6	-1,95	88,9
36	-5,45	24,5	-41,16	-70,6	-4,92	89,3	-2,12	80,9
37	-6,88	13,9	-41,12	-84,2	-3,29	88	-2,3	73,4
38	-9,34	3,7	-42,27	-89,6	-1,05	83,8	-2,51	66,2
39	-13,51	-1,3	-41,21	-108,8	1,77	74,4	-2,7	58,2
40	-21,64	49,9	-41,07	-130,8	4,18	55,5	-3,22	50,2
41	-13,04	95,8	-47,32	-151,5	5,47	38,5	-3,59	43,3
42	-7,18	87,7	-50,87	-74,5	7,16	20,8	-4,06	34,9
43	-4,19	70,7	-42,36	-79,2	8,35	-0,2	-4,88	26,9
44	-2,48	53,6	-38,05	-96,4	9,2	-19,7	-5,68	20
45	-1,56	37,1	-35,54	-113,9	9,96	-39,3	-6,66	12,8
46	-1,13	22	-34,48	-122,1	10,55	-58,1	-7,73	6,5
47	-0,93	6	-32,16	-127,2	11,32	-77	-9,16	0,1
48	-1,23	-8,5	-28,67	-156,4	11,99	-98	-10,87	0,2
49	-2,14	-22	-28,47	176,8	12,18	-121	-11,61	6,6
50	-3,09	-34,3	-29,18	157,7	12,1	-142,7	-11,33	7,5
51	-4,76	-42,4	-29,48	147,1	11,94	-163,6	-10,87	5,3
52	-6,29	-45,5	-27,33	127,2	11,65	176,6	-10,03	2,7
53	-7,54	-46,3	-27,27	99,4	11,31	156,8	-9,34	-6,2
54	-7,99	-42,1	-27,59	81,8	10,87	137,9	-8,91	-16,1
55	-7,63	-39	-27,52	64,5	10,44	119,9	-8,6	-27
56	-6,75	-39,3	-27,7	50,7	10	102,2	-8,49	-37,5
57	-5,78	-43,8	-26,84	38,4	9,64	84,8	-8,27	-48,9
58	-4,75	-51,4	-26,96	22,3	9,39	67,5	-8,12	-59,8
59	-4,31	-63,3	-26,49	4,2	9,1	46,8	-8,13	-69,7
60	-4,01	-71,9	-26,42	-10,1	8,56	30,1	-7,89	-80,5

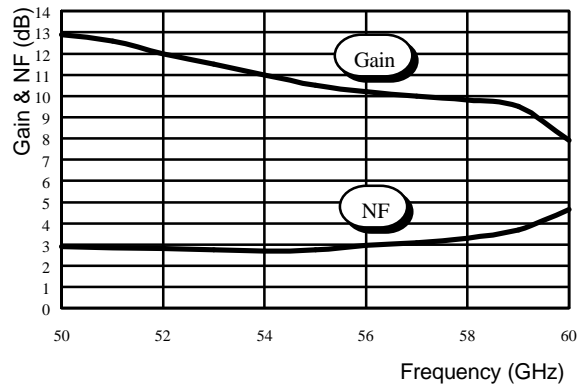
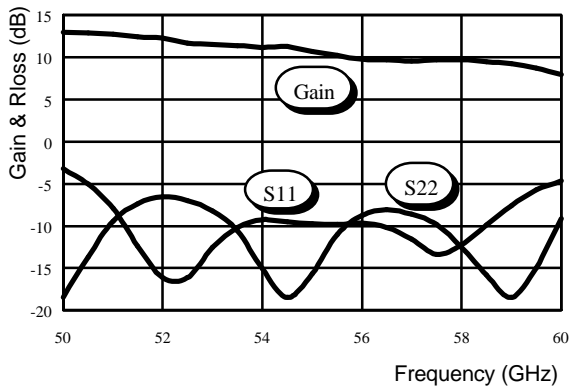
**Typical on Wafer Measurements**

Bias conditions:  $T_{amb} = +25^{\circ}C$ ,  $V_d = 3.3V$ ,  $V_{g1} = V_{g2}$  to have  $I_d = 80mA$

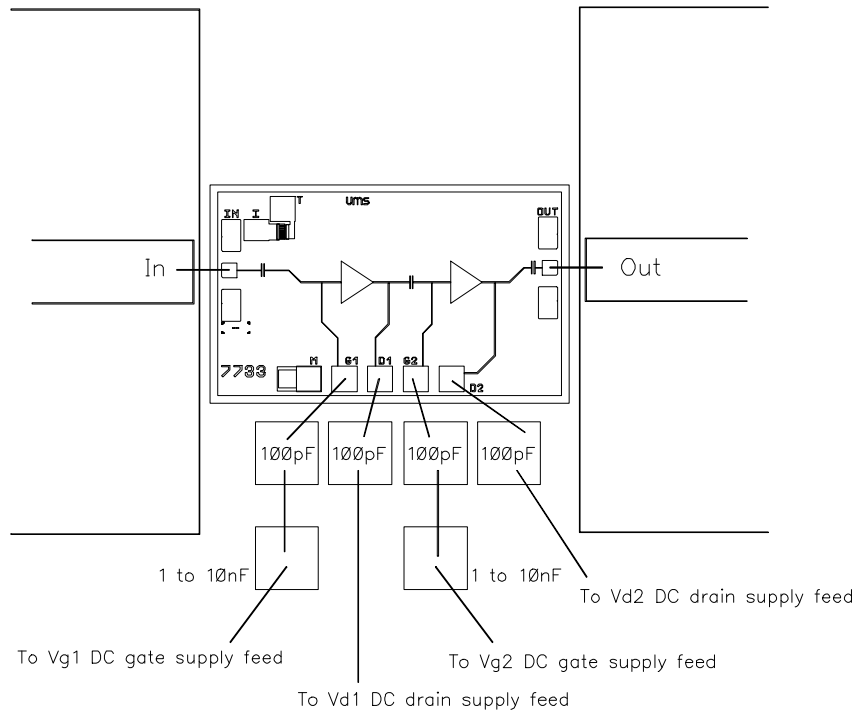


**Typical packaged Measurements**

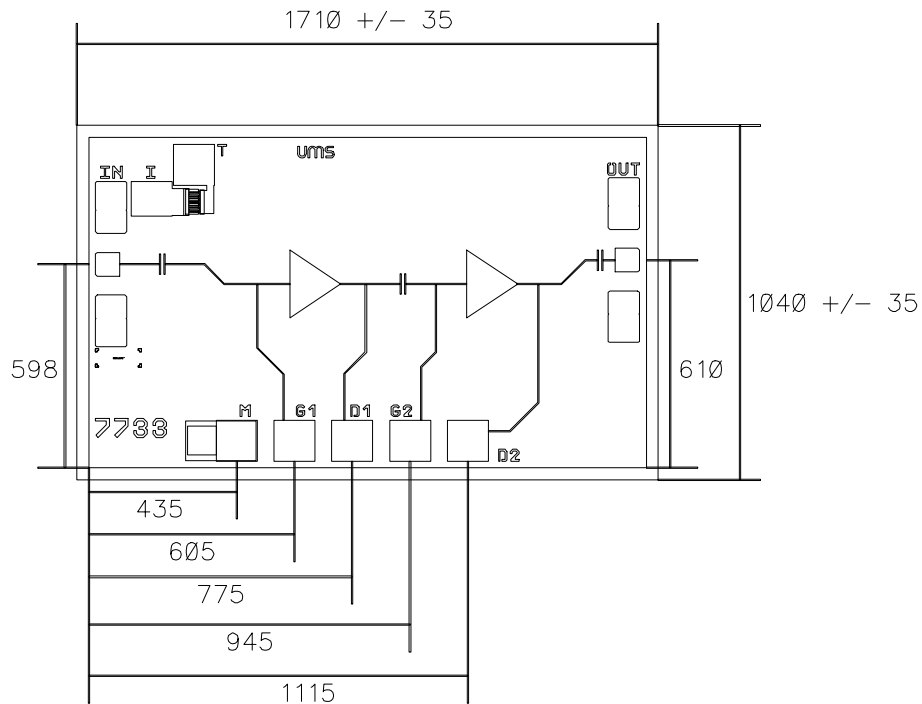
Bias conditions:  $T_{amb} = +25^{\circ}C$ ,  $V_d = 3.3V$ ,  $V_{g1} = V_{g2}$  to have  $I_d = 80mA$



Chip Assembly and Mechanical Data



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.



**Bonding pad positions.**

( Chip thickness : 100µm. All dimensions are in micrometers )

## Ordering Information

Chip form : CHA2157-99F/00

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