1GB – 128Mx64 DDR2 SDRAM UNBUFFERED, SO-DIMM

FEATURES

- 200-pin, Small-Outline DIMM (SO-DIMM), Raw Card "B"
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 Mb/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$ to $3.6V$
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- DLL to align DQ and DQS transitions with CK
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5* and 6*
- Adjustable data-output drive strength
- On-Die Termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Single Rank
- RoHS Compliant
- JEDEC Package option
  - 200 Pin (SO-DIMM)
  - PCB – 29.20mm (1.150") TYP

DESCRIPTION

The W3HG128M64EEU is a 128Mx64 Double Data Rate 2 SDRAM memory module based on 1Gb DDR2 SDRAM components. The module consists of eight 128Mx8, in FBGA package mounted on a 200 pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-6400*	PC2-5300*	PC2-4200	PC2-3200
Clock Speed	400MHz	333MHz	266MHz	200MHz
CL-t_{RCD}-t_{RP}	6-6-6	5-5-5	4-4-4	3-3-3

* Consult factory for availability

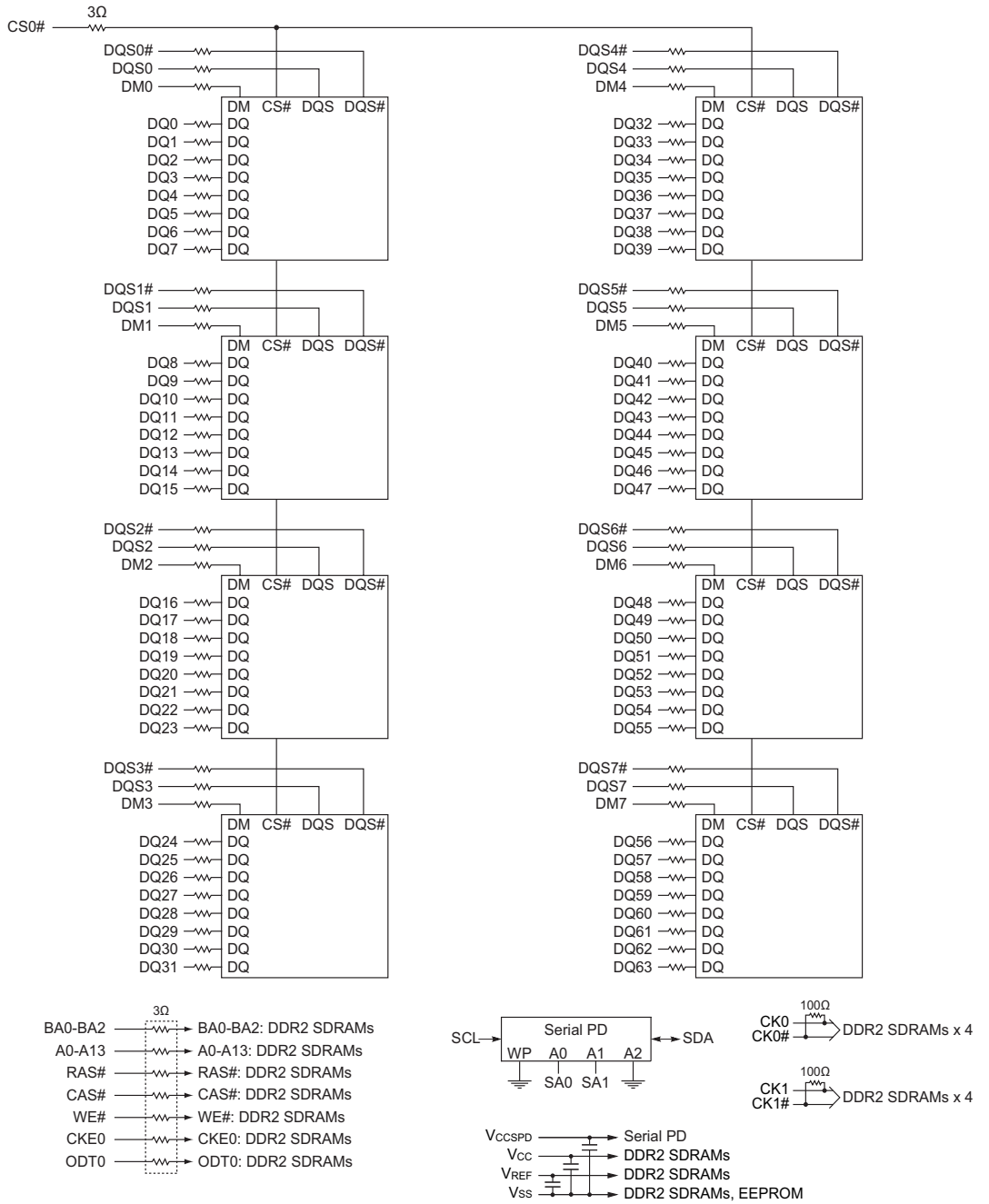
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	51	DQS2	101	A1	151	DQ42
2	V_{SS}	52	DM2	102	A0	152	DQ46
3	V_{SS}	53	V_{SS}	103	V_{CC}	153	DQ43
4	DQ4	54	V_{SS}	104	V_{CC}	154	DQ47
5	DQ0	55	DQ18	105	A10/AP	155	V_{SS}
6	DQ5	56	DQ22	106	BA1	156	V_{SS}
7	DQ1	57	DQ19	107	BA0	157	DQ48
8	V_{SS}	58	DQ23	108	RAS#	158	DQ52
9	V_{SS}	59	V_{SS}	109	WE#	159	DQ49
10	DM0	60	V_{SS}	110	CS0#	160	DQ53
11	DQS0#	61	DQ24	111	V_{CC}	161	V_{SS}
12	V_{SS}	62	DQ28	112	V_{CC}	162	V_{SS}
13	DQS0	63	DQ25	113	CAS#	163	NC
14	DQ6	64	DQ29	114	ODT0	164	CK1
15	V_{SS}	65	V_{SS}	115	NC	165	V_{SS}
16	DQ7	66	V_{SS}	116	A13	166	CK1#
17	DQ2	67	DM3	117	V_{CC}	167	DQS6#
18	V_{SS}	68	DQS3#	118	V_{CC}	168	V_{SS}
19	DQ3	69	NC	119	NC	169	DQS6
20	DQ12	70	DQS3	120	NC	170	DM6
21	V_{SS}	71	V_{SS}	121	V_{SS}	171	V_{SS}
22	DQ13	72	V_{SS}	122	V_{SS}	172	V_{SS}
23	DQ8	73	DQ26	123	DQ32	173	DQ50
24	V_{SS}	74	DQ30	124	DQ36	174	DQ54
25	DQ9	75	DQ27	125	DQ33	175	DQ51
26	DM1	76	DQ31	126	DQ37	176	DQ55
27	V_{SS}	77	V_{SS}	127	V_{SS}	177	V_{SS}
28	V_{SS}	78	V_{SS}	128	V_{SS}	178	V_{SS}
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
30	CK0	80	NC	130	DM4	180	DQ60
31	DQS1	81	V_{CC}	131	DQS4	181	DQ57
32	CK0#	82	V_{CC}	132	V_{SS}	182	DQ61
33	V_{SS}	83	NC	133	V_{SS}	183	V_{SS}
34	V_{SS}	84	NC	134	DQ38	184	V_{SS}
35	DQ10	85	BA2	135	DQ34	185	DM7
36	DQ14	86	NC	136	DQ39	186	DQS7#
37	DQ11	87	V_{CC}	137	DQ35	187	V_{SS}
38	DQ15	88	V_{CC}	138	V_{SS}	188	DQS7
39	V_{SS}	89	A12	139	V_{SS}	189	DQ58
40	V_{SS}	90	A11	140	DQ44	190	V_{SS}
41	V_{SS}	91	A9	141	DQ40	191	DQ59
42	V_{SS}	92	A7	142	DQ45	192	DQ62
43	DQ16	93	A8	143	DQ41	193	V_{SS}
44	DQ20	94	A6	144	V_{SS}	194	DQ63
45	DQ17	95	V_{CC}	145	V_{SS}	195	SDA
46	DQ21	96	V_{CC}	146	DQS5#	196	V_{SS}
47	V_{SS}	97	A5	147	DM5	197	SCL
48	V_{SS}	98	A4	148	DQS5	198	SA0
49	DQS2#	99	A3	149	V_{SS}	199	V_{CCSPD}
50	NC	100	A2	150	V_{SS}	200	SA1

PIN NAMES

SYMBOL	DESCRIPTION
A0 - A13	Address input
ODT0	On-Die Termination
CK0, CK0#	Differential Clock Inputs
CK1, CK1#	Differential Clock inputs
CKE0	Clock Enable input
CS0#	Chip select
RAS#, CAS#, WE#	Command Inputs
BA0 - BA2	Bank Address Inputs
DM0 - DM7	Input Data Mask
DQ0 - DQ63	Data Input/Output
DQS0 - DQS7 DQS0#-DQS7#	Data Strobe
SCL	Serial Clock for Presence Detect
SA0-SA1	Presence Detect Address Inputs
SDA	Serial Presence Detect Data
V_{CC}	Power Supply
V_{REF}	SSTL_18 reference voltage
V_{SS}	Ground
V_{CCSPD}	Serial EEPROM Power Supply
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



NOTE: 1. All resistor values are 22 ohm unless otherwise specified.

ABSOLUTE MAXIMUM DC CHARACTERISTICS

Symbol	Parameter		Min	Max	Units
V_{CC}	V_{CC} Supply Voltage Relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any Pin Relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	°C
T_{CASE}	DDR2 SDRAM Device Operating Temperature*		0	85	°C
T_{OPR}	Operating Temperature (Ambient)		0	65	°C
I_I	Input Leakage Current; Any input 0V ≤ V_{IN} ≤ V_{CC}; V_{REF} input 0V ≤ V_{IN} ≤0.95V; (All other pins not under test = 0V)	Command/Address, RAS#, CAS#, WE# S#, CKE	-40	40	µA
		CK, CK#	-20	20	
		DM	-5	5	
I_{OZ}	Output Leakage Current; 0V ≤ V_{OUT} ≤ $V_{CC}Q$; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	µA
I_{VREF}	V_{REF} Leakage Current; V_{REF} = Valid V_{REF} level		-16	16	µA

* T_{CASE} specifies as the temperature at the top center of the memory devices.

RECOMMENDED DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units	Notes
Supply Voltage	V_{CC}	1.7	1.9	V	-
I/O Reference Voltage	V_{REF}	0.49 x V_{CC}	0.51 x V_{CC}	V	1
I/O Termination Voltage (system)	V_{TT}	V_{REF} - 40	V_{REF} + 40	mV	2

NOTE:

1. V_{REF} is expected to equal V_{CCQ}/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (non-common mode) on V_{REF} may not exceed ±1 percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed ±2 percent of V_{REF} (DC). This measurement is to be taken at the nearest V_{REF} bypass capacitor.
2. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF} and must track variations in the DC level of V_{REF}.

CAPACITANCE

T_A = 25°C, f = 100MHz, V_{CC} = 1.8V, V_{REF} = V_{SS}

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C_{IN1}	35	pF
Input Capacitance (RAS#,CAS#,WE#)	C_{IN2}	35	pF
Input Capacitance (CKE0)	C_{IN3}	31	pF
Input Capacitance (CK0, CK0#)	C_{IN4}	15	pF
Input Capacitance (CS0#)	C_{IN5}	31	pF
Input Capacitance (DQS0#-DQS17#)	C_{IN6}	6	pF
Input Capacitance (BA0-BA1)	C_{IN7}	35	pF
Data input/output Capacitance (DQ0-DQ63)	C_{OUT}	6	pF

NOTE:

* These capacitance values are based on worst case component values in conjunction with the circuit boards associated parasitic net capacitance.

DDR2 I_{CC} SPECIFICATIONS AND CONDITIONS

DDR2 SDRAM components only

V_{CC} = +1.8V ± 0.1V

Parameter	Symbol	Condition		806	665	534	403	Units
Operating one device bank active-precharge current;	I_{CC0}	$t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ MIN (I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	800	640	640	mA
Operating one device bank active-read-precharge current;	I_{CC1}	I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ MIN (I_{CC}), $t_{RCD} = t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC4W}.		TBD	1,160	760	760	mA
Precharge power-down current;	I_{CC2P}	All device banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		TBD	56	40	40	mA
Precharge quiet standby current;	I_{CC2Q}	All device banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.		TBD	480	328	280	mA
Precharge standby current;	I_{CC2N}	All device banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	520	360	280	mA
Active power-down current;	I_{CC3P}	All device banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MR[12] = 0	TBD	320	240	200	mA
			Slow PDN Exit MR[12] = 1	TBD	80	80	80	mA
Active standby current;	I_{CC3N}	All device banks open; $t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$ MAX (I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	560	400	320	mA
Operating burst write current;	I_{CC4W}	All device banks open, Continuous burst writes; BL = 4, CL = CL (I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$ MAX (I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	1,440	1,040	960	mA
Operating burst read current;	I_{CC4R}	All device banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL (I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$ MAX (I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	1,640	1,160	1,080	mA
Burst refresh current;	I_{CC5}	$t_{CK} = t_{CK}(I_{CC})$; Refresh command at every t_{RFC} (I_{CC}) interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		TBD	2,160	2,000	1,920	mA
Self refresh current;	I_{CC6}	CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.		TBD	56	40	40	mA
Operating device bank interleave read current;	I_{CC7}	All device banks interleaving reads, I_{OUT}= 0mA; BL = 4, CL = CL (I_{CC}), AL = t_{RCD} (I_{CC})-1 x t_{CK} (I_{CC}); $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, $t_{RCD} = t_{RCD}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING		TBD	2,720	2,360	2,360	mA

Note:

- I_{CC} specification is based on MICRON components. Other DRAM manufacturers specification may be different.

DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATION

V_{CC} = +1.8V ±0.1V

	AC Characteristics		Symbol	806		665		534		403		Units	Notes
	Parameter			Min	Max	Min	Max	Min	Max	Min	Max		
Clock	Clock cycle time	CL = 6	^{t}CK (6)	3,000	8,000	-	-	-	-	-	-	ps	
		CL = 5	^{t}CK (5)	3,000	8,000	3,000	8,000	-	-	-	-	ps	16, 22, 36, 38
		CL = 4	^{t}CK (4)	3,000	8,000	3,750	8,000	3,750	8,000	5,000	8,000	ps	
		CL = 3	^{t}CK (3)	-	-	5,000	8,000	5,000	8,000	5,000	8,000	ps	
	CK high-level width		$^{t}CH_{AVG}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK	45
	CK low-level width		$^{t}CL_{AVG}$	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	^{t}CK	
	Half clock period		^{t}HP	MIN (t_{CH},t_{CL})		MIN (t_{CH},t_{CL})		MIN (t_{CH},t_{CL})		MIN (t_{CH},t_{CL})		ps	46
Clock (Absolute)	Absolute tCk		$^{t}CK_{abs}$	^{t}CKAVG(MIN)+ ^{t}JITPER(MIN)	^{t}CKAVG(MAX)+ ^{t}JITPER(MAX)	^{t}CKAVG(MIN)+ ^{t}JITPER(MIN)	^{t}CKAVG(MAX)+ ^{t}JITPER(MAX)	^{t}CKAVG(MIN)+ ^{t}JITPER(MIN)	^{t}CKAVG(MAX)+ ^{t}JITPER(MAX)	^{t}CKAVG(MIN)+ ^{t}JITPER(MIN)	^{t}CKAVG(MAX)+ ^{t}JITPER(MAX)	ps	
	Absolute CK high-level width		$^{t}CH_{abs}$	^{t}CKAVG(MIN)*^{t}CHAVG+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)*^{t}CHAVG+^{t}JITDTY(MAX)	^{t}CKAVG(MIN)*^{t}CHAVG+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)*^{t}CHAVG+^{t}JITDTY(MAX)	^{t}CKAVG(MIN)*^{t}CHAVG+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)*^{t}CHAVG+^{t}JITDTY(MAX)	^{t}CKAVG(MIN)*^{t}CHAVG+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)*^{t}CHAVG+^{t}JITDTY(MAX)	ps	
	Absolute CK low-level width		$^{t}CL_{abs}$	^{t}CKAVG(MIN)* ^{t}CLAVG(MIN)+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)* ^{t}CLAVG(MAX)+ ^{t}JITDTY(MIN)	^{t}CKAVG(MIN)* ^{t}CLAVG(MIN)+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)* ^{t}CLAVG(MAX)+ ^{t}JITDTY(MIN)	^{t}CKAVG(MIN)* ^{t}CLAVG(MIN)+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)* ^{t}CLAVG(MAX)+ ^{t}JITDTY(MIN)	^{t}CKAVG(MIN)* ^{t}CLAVG(MIN)+^{t}JITDTY(MIN)	^{t}CKAVG(MAX)* ^{t}CLAVG(MAX)+ ^{t}JITDTY(MIN)	ps	
Clock jitter	Clock jitter - period		$^{t}JIT_{PER}$	-125	125	-125	125	-125	125	-125	125	ps	39
	Clock jitter - half period		$^{t}JIT_{DUTY}$	-125	125	-125	125	-125	125	-150	150	ps	40
	Clock jitter - cycle to cycle		$^{t}JIT_{CC}$	250		250		250		250		ps	41
	Cumulative jitter error, 2 cycles		$^{t}ERR_{2per}$	-175	175	-175	175	-175	175	-175	175	ps	42
	Cumulative jitter error, 3 cycles		$^{t}ERR_{3per}$	-225	225	-225	225	-225	225	-225	225	ps	42
	Cumulative jitter error, 4 cycles		$^{t}ERR_{4per}$	-250	250	-250	250	-250	250	-250	250	ps	42
	Cumulative jitter error, 5cycles		$^{t}ERR_{5per}$	-250	250	-250	250	-250	250	-250	250	ps	42, 48
	Cumulative jitter error, 6-10 cycles		$^{t}ERR_{6-10per}$	-350	350	-350	350	-350	350	-350	350	ps	42, 48
	Cumulative jitter error, 11-50 cycles		$^{t}ERR_{11-50per}$	-450	450	-450	450	-450	450	-450	450	ps	42

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specification may be different.

DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATION (continued)

V_{CC} = +1.8V ±0.1V

	AC Characteristics	Symbol	806		665		534		403		Units	Notes
	Parameter		Min	Max	Min	Max	Min	Max	Min	Max		
Data	DQ output access time from CK/CK#	^tAC	-450	+450	-450	+450	-500	+500	-600	+600	ps	43
	Data-out high-impedance window from CK/CK#	^tHZ		^tAC (MAX)		^tAC (MAX)		^tAC (MAX)		^tAC (MAX)	ps	8, 9, 43
	Data-out low-impedance window from CK/CK#	$^tLZ1$	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	^tAC (MIN)	^tAC (MAX)	ps	8, 10, 43
	Data-out low-impedance window from CK/CK#	$^tLZ2$	2*^tAC (MIN)	^tAC (MAX)	2*^tAC (MIN)	^tAC (MAX)	2*^tAC (MIN)	^tAC (MAX)	2*^tAC (MIN)	^tAC (MAX)	ps	8, 10, 43
	DQ and DM input setup time relative to DQS	^tDS_a	300		300		350		400		ps	7, 15, 19
	DQ and DM input hold time relative to DQS	^tDH_a	300		300		350		400		ps	7, 15, 19
	DQ and DM input setup time relative to DQS	^tDS_b	100		100		100		150		ps	7, 15, 19
	DQ and DM input hold time relative to DQS	^tDH_b	175		175		225		275		ps	7, 15, 19
	DQ and DM input pulse width (for each input)	^tDIPW	0.35		0.35		0.35		0.35		^tCK	37
	Data hold skew factor	^tQHS		340		340		400		450	ps	47
	DQ–DQS hold, DQS to first DQ to go nonvalid, per access	^tQH	^tHP-^tQHS		^tHP-^tQHS		^tHP-^tQHS		^tHP-^tQHS		ps	15, 17, 47
	Data valid output window (DVW)	^tDVW	^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		^tQH - ^tDQSQ		ns	15, 17
Data Strobe	DQS input high pulse width	^tDQSH	0.35		0.35		0.35		0.35		^tCK	37
	DQS input low pulse width	^tDQSL	0.35		0.35		0.35		0.35		^tCK	37
	DQS output access time from CK/CK#	^tDQSCK	-400	+400	-400	+400	-450	+450	-500	+500	ps	40
	DQS falling edge to CK rising – setup time	^tDSS	0.2		0.2		0.2		0.2		^tCK	37
	DQS falling edge from CK rising – hold time	^tDSH	0.2		0.2		0.2		0.2		^tCK	37

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specification may be different.

DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATION (continued)

V_{CC} = +1.8V ±0.1V

	AC Characteristics	Symbol	806		665		534		403		Units	Notes
	Parameter		Min	Max	Min	Max	Min	Max	Min	Max		
Data Strobe	DQS–DQ skew, DQS to last DQ valid, per group, per access	t_{DQSQ}		240		240		300		350	ps	15, 17
	DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	33, 37, 43
	DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	33, 34, 37, 43
	DQS write preamble setup time	t_{WPRES}	0		0		0		0		ps	12, 13,
	DQS write preamble	t_{WPRE}	0.35		0.35		0.25		0.25		t_{CK}	37
	DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	11, 37
	Write command to first DQS latching transition	t_{DQSS}	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}	37
Command and Address	Address and control input pulse width for each input	t_{IPW}	0.6		0.6		0.6		0.6		t_{CK}	37
	Address and control input setup time	t_{IS_a}	400		400		500		600		ps	6, 19
	Address and control input hold time	t_{IH_a}	400		400		500		600		ps	6, 19
	Address and control input setup time	t_{IS_b}	200		200		250		350		ps	6, 19
	Address and control input hold time	t_{IH_b}	275		275		375		475			6, 19
	CAS# to CAS# command delay	t_{CCD}	2		2		2		2		t_{CK}	37
	ACTIVE to ACTIVE (same bank) command	t_{RC}	54		55		55		55		ns	31, 37
	ACTIVE bank a to ACTIVE bank b command	t_{RRD} (x8)	7.5		7.5		7.5		7.5		ns	25, 37
	ACTIVE to READ or WRITE delay	t_{RCD}	12		15		15		15		ns	37
	Four Bank Activate period	t_{FAW} (x8)	37.5		37.5		37.5		37.5		ns	28, 37
	ACTIVE to PRECHARGE command	t_{RAS}	40	70,000	40	70,000	40	70,000	40	70,000	ns	18, 31, 37
	Internal READ to precharge command delay	t_{RTP}	7.5		7.5		7.5		7.5		ns	21, 25. 37
	Write recovery time	t_{WR}	15		15		15		15		ns	25, 37
	Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		$t_{WR} + t_{RP}$		ns	20
	Internal WRITE to READ command delay	t_{WTR}	7.5		7.5		7.5		10		ns	25, 37
	PRECHARGE command period	t_{RP}	12		15		15		15		ns	29, 37
	PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		$t_{RP} + t_{CK}$		ns	29
	LOAD MODE command cycle time	t_{MRD}	2		2		2		2		t_{CK}	37

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specification may be different.

DDR2 SDRAM COMPONENT AC TIMING PARAMETERS & SPECIFICATION (continued)

V_{CC} = +1.8V ±0.1V

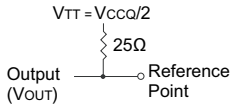
	AC Characteristics	Symbol	806		665		534		403		Units	Notes
	Parameter		Min	Max	Min	Max	Min	Max	Min	Max		
Refresh	CKE low to CK,CK# uncertainty	^{t}DELAY	$^{t}IS + ^{t}CK + ^{t}IH$		$^{t}IS + ^{t}CK + ^{t}IH$		$^{t}IS + ^{t}CK + ^{t}IH$		$^{t}IS + ^{t}CK + ^{t}IH$		ns	26
	REFRESH to ACTIVE or REFRESH to REFRESH command interval	^{t}RFC	127.5	70,000	127.5	70,000	127.5	70,000	127.5	70,000	ns	14, 37
	Average periodic refresh interval (commercial)	^{t}REFI		7.8		7.8		7.8		7.8	µs	14, 37
	Average periodic refresh interval (industrial)	$^{t}REFI_{IT}$		3.9		3.9		3.9		3.9	µs	14, 37
Self Refresh	Exit self refresh to non-READ command	^{t}XSNR	^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		^{t}RFC (MIN) + 10		ns	
	Exit self refresh to READ command	^{t}XSRD	200		200		200		200		^{t}CK	37
	Exit self refresh timing reference	^{t}ISXR	^{t}IS		^{t}IS		^{t}IS		^{t}IS		ps	6, 27
ODT	ODT turn-on delay	^{t}AOND	2	2	2	2	2	2	2	2	^{t}CK	37
	ODT turn-on	^{t}AOND	^{t}AC (MIN)	^{t}AC (MAX) + 700)	^{t}AC (MIN)	^{t}AC (MAX) + 700)	^{t}AC (MIN)	^{t}AC (MAX) + 1,000)	^{t}AC (MIN)	^{t}AC (MAX) + 1,000)	ps	23, 43
	ODT turn-off delay	^{t}AOFD	2.5	2.5	2.5	2.5	2.5	2.5	2.5	2.5	^{t}CK	35, 37
	ODT turn-off	^{t}AOF	^{t}AC (MIN)	^{t}AC (MAX + 600)	^{t}AC (MIN)	^{t}AC (MAX + 600)	^{t}AC (MIN)	^{t}AC (MAX + 600)	^{t}AC (MIN)	^{t}AC (MAX + 600)	ps	24, 44
	ODT turn-on (power-down mode)	^{t}AONPD	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT turn-off (power-down mode)	$_{t}$AOFPD	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	^{t}AC (MIN) + 2,000	2.5 x ^{t}CK + ^{t}AC (MAX) + 1,000	ps	
	ODT to power-down entry latency	^{t}ANPD	3		3		3		3		^{t}CK	37
	ODT power-down exit latency	^{t}AXPD	8		8		8		8		^{t}CK	37
	ODT enable from MRS command	^{t}MOD	12		12		12		12		ns	37, 49
Power Down	Exit active power-down to READ command, MR[bit12=0]	^{t}XARD	2		2		2		2		^{t}CK	37
	Exit active power-down to READ command, MR[bit12=1]	^{t}XARDS	7 - AL		7 - AL		6 - AL		6 - AL			37
	Exit precharge power-down to any non-READ command.	^{t}XP	2		2		2		2		^{t}CK	37
	CKE minimum high/low time	^{t}CKE	3		3		3		3		^{t}CK	32, 37

Note:

- AC specification is based on MICRON components. Other DRAM manufactures specifications may be different.

Notes:

1. All voltages referenced to VSS.
2. Tests for AC timing, I_{CC}, and electrical AC and DC characteristics may be conducted at nominal reference / supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified. ODT is disabled for all measurements that are not ODT-specific.
3. Outputs measured with equivalent load:



4. AC timing and I_{CC} tests may use a V_{IL}-to-V_{IH} swing of up to 1.0V in the test environment and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The slew rate for the input signals used to test the device is 1.0V/ns for signals in the range between V_{IL} (AC) and V_{IH} (AC). Slew rates less than 1.0V/ns require the timing parameters to be derated as specified.
5. The AC and DC input level specifications are as defined in the SSTL_18 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [HIGH] level).
6. There are two sets of values listed for Command/Address: t_{ISa}, t_{IHa} and t_{ISb}, t_{IHb}. The t_{ISa}, t_{IHa} values (for reference only) are equivalent to the baseline values of t_{ISb}, t_{IHb} at V_{REF} when the slew rate is 1V/ns. The baseline values, t_{ISb}, t_{IHb}, are the JEDEC defined values, referenced from the logic trip points. t_{ISb} is referenced from V_{IH} (AC) for a rising signal and V_{IL} (AC) for a falling signal, while t_{IHb} is referenced from V_{IL} (DC) for a rising signal and V_{IH} (DC) for a falling signal. If the Command/Address slew rate is not equal to 1 V/ns, then the baseline values must be derated.
7. The values listed are for the differential DQS strobe (DQS and DQS#) with a differential slew rate of 2 V/ns (1 V/ns for each signal). There are two sets of values listed: ^{t}DSa, ^{t}DHa and ^{t}DSb, ^{t}DHb. The ^{t}DSa, ^{t}DHa values (for reference only) are equivalent to the baseline values of ^{t}DSb, ^{t}DHb at V_{REF} when the slew rate is 2 V/ns, differentially. The baseline values, ^{t}DSb, ^{t}DHb, are the JEDEC-defined values, referenced from the logic trip points. ^{t}DSb is referenced from V_{IH} (AC) for a rising signal and V_{IL} (AC) for a falling signal, while ^{t}DSb is referenced from V_{IL} (DC) for a rising signal and V_{IH} (DC) for a falling signal. If the differential DQS slew rate is not equal to 2 V/ns, then the baseline values must be derated. If the DQS differential strobe feature is not enabled, then the DQS strobe is single-ended, the baseline values not applicable, and timing is not referenced to the logic trip points. Single-ended DQS data timing is referenced to DQS crossing V_{REF}.
8. ^{t}HZ and ^{t}LZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (^{t}HZ) or begins driving (^{t}LZ).
9. This maximum value is derived from the referenced test load. ^{t}HZ (MAX) will prevail over ^{t}DQSCK (MAX) + ^{t}RPST (MAX) condition.
10. ^{t}LZ (MIN) will prevail over a ^{t}DQSCK (MIN) + ^{t}RPRE (MAX) condition
11. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be high, low or High-Z and that any signal transition within the input switching region must follow valid input requirements. That is if DQS transitions high (above V_{IH}DC(min) then it must not transition low (below V_{IH}(DC) prior to ^{t}DQSH(min).
12. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
13. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on ^{t}DQSS.
14. The refresh period is 64ms (commercial) or 32ms (industrial). This equates to an average refresh rate of 7.8125µs (commercial) or 3.9607µs (industrial). However, a REFRESH command must be asserted at least once every 70.3µs or ^{t}RFC (MAX). To ensure all rows of all banks are properly refreshed, 8,192 REFRESH commands must be issued every 64ms.
15. Referenced to each output group: x4 = DQS with DQ0–DQ3; x8 = DQS with DQ0–DQ7; x16 = LDQS with DQ0–DQ7; and UDQS with DQ8–DQ15.
16. CK and CK# input slew rate is referenced at 1 V/ns (2 V/ns if measured differentially).
17. The data valid window is derived by achieving other specifications - ^{t}HP. (^{t}CK/2), ^{t}DQSQ, and ^{t}QH (^{t}QH = ^{t}HP - ^{t}QHS). The data valid window derates in direct proportion to the clock duty cycle and a practical data valid window can be derived.
18. READs and WRITEs with auto precharge are allowed to be issued before ^{t}RAS(MIN) is satisfied since ^{t}RAS lockout feature is supported in DDR2 SDRAM.
19. V_{IL}/V_{IH} DDR2 overshoot/undershoot.
20. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK). Each of these terms, if not already an integer, should be rounded up to the next integer. ^{t}CK refers to the application clock period; nWR refers with ^{t}WR programmed to four clocks would have ^{t}DAL = 4 + (15ns/3.75ns) clocks = 4 + (4) clocks = 8 clocks.
21. The minimum internal READ to PRECHARGE time. This is the time from the last 4-bit prefetch begins to when the PRECHARGE command can be issued. A 4-bit prefetch is when the READ command internally latches the READ so that data will output CL later. This parameter is only applicable when ^{t}RTP/(2x ^{t}CK) > 1, such as frequencies faster than 533 MHz when tRTP = 7.5ns. If tRTP/ (2x ^{t}CK) ≤ 1, then equation AL + BL/2 applies. tRAS (MIN) also has to be satisfied as well. The DDR2 SDRAM will automatically delay the internal PRECHARGE command until ^{t}RAS (MIN) has been satisfied.
22. Operating frequency is only allowed to change during self refresh mode, precharge power-down mode, and system reset condition.
23. ^{t}DAL = (nWR) + (^{t}RP/^{t}CK): For each of the terms above, if not already an integer, round to the next highest integer. ^{t}CK refers to the application clock period; AC Operation Condition Notes: nWR refers to the ^{t}WR parameter stored in the MR[11,10,9]. Example: For -533Mb/s at ^{t}CK = 3.75 ns with ^{t}WR programmed to four clocks. ^{t}DAL = 4 + (15 ns/3.75 ns) clocks = 4 +(4) clocks = 8 clocks.
24. ODT turn-off time ^{t}AOF (MIN) is when the device starts to turn off ODT resistance. ODT turn off time ^{t}AOF (MAX) is when the bus is in high-Z. Both are measured from ^{t}AOFD.
25. This parameter has a two clock minimum requirement at any ^{t}CK.
26. ^{t}DELAY is calculated from ^{t}IS + ^{t}CK + ^{t}IH so that CKE registration LOW is guaranteed prior to CK, CK# being removed in a system RESET condition.
27. ^{t}ISXR is equal to ^{t}IS and is used for CKE setup time during self refresh exit.
28. No more than 4 bank ACTIVE commands may be issued in a given ^{t}FAW(min) period. ^{t}RRD(min) restriction still applies. The ^{t}FAW(min) parameter applies to all 8 bank DDR2 devices, regardless of the number of banks already open or closed.
29. ^{t}RPA timing applies when the PRECHARGE(ALL) command is issued, regardless of the number of banks already open or closed. If a single-bank PRECHARGE command is issued, ^{t}RP timing applies. ^{t}RPA(MIN) applies to all 8-bank DDR2 devices.
30. Value is minimum pulse width, not the number of clock registrations.
31. This is applicable to Read cycles only. Write cycles generally require additional time due to ^{t}WR during auto precharge.
32. ^{t}CKE (MIN) of 3 clocks means CKE must be registered on three consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the 3 clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of ^{t}IS + 2 x ^{t}CK + ^{t}IH.
33. This parameter is not referenced to a specific voltage level, but specified when the device output is no longer driving (^{t}RPST) or beginning to drive (^{t}RPRE).
34. When DQS is used single-ended, the minimum limit is reduced by 100ps.
35. The half-clock of ^{t}AOFD's 2.5 ^{t}CK assumes a 50/50 clock duty cycle. This half-clock value must be derated by the amount of half-clock duty cycle error. For example, if the clock duty cycle was 47/53, ^{t}AOFD would actually be 2.5 - 0.03, or 2.47 for ^{t}AOF (MIN) and 2.5 + 0.03 or 2.53 for ^{t}AOF (MAX).
36. The clock's ^{t}CK$_{AVG}$ is the average clock over any 200 consecutive clocks and

$^{t}CK_{AVG}$(MIN) is the smallest clock rate allowed, except a deviation due to allowed clock jitter. Input clock jitter is allowed provided it does not exceed values specified. Also, the jitter must be of a random Gaussian distribution in nature.

37. The inputs to the DRAM must be aligned to the associated clock; that is, the actual clock that latches it in. However, the input timing (in ns) references to the $^{t}CK_{AVG}$ when determining the required number of clocks. The following input parameters are determined by taking the specified percentage times the tCKAVG rather thank ^{t}CK: ^{t}IPW, $^{t}DIPW$, $^{t}DQSS$, $^{t}DQSH$, $^{t}DQSL$, ^{t}DSS, ^{t}DH, $^{t}WPST$, and $^{t}WPRE$.
38. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread spectrum at a sweep rate in the range 20–60 KHz with additional one percent of $^{t}CK_{AVG}$ as a long-term jitter component; however, the spread spectrum may not use a clock rate below $^{t}CK_{AVG}$(MIN) or above $^{t}CK_{AVG}$(MAX).
39. The period jitter ($^{t}JIT_{PER}$) is the maximum deviation in the clock period from the average or nominal clock allowed in either the positive or negative direction. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked).
40. The half-period jitter ($^{t}JIT_{DTY}$) applies to either the high pulse of clock or the low pulse of clock; however, the two cumulatively can not exceed $^{t}JIT_{PER}$.
41. The cycle-to-cycle jitter ($^{t}JIT_{CC}$) is the amount the clock period can deviate from one cycle to the following cycle. JEDEC specifies tighter jitter numbers during DLL locking time. During DLL lock time, the jitter values should be 20 percent less than noted in the table (DLL locked).
42. The cumulative jitter error ($^{t}ERR_{nPER}$) where n is 2, 3, 4, 5, 6–10, or 11–50, is the amount of clock time allowed to consecutively accumulate away from the average clock over any number of clock cycles.
43. The DRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present; this will result in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}ERR_{5PER}$(MAX): ^{t}AC(MIN), $^{t}DQSCK$(MIN), ^{t}HZ(MIN), $^{t}LZ_{DQ}$(MIN), ^{t}AON(MIN); while these following parameters are required to be derated by subtracting $^{t}ERR_{5PER}$(MIN): ^{t}AC(MAX), $^{t}DQSCK$(MAX), ^{t}HZ(MAX), $^{t}LZ_{DQ}$(MAX), ^{t}AON(MAX). The parameter $^{t}RPRE$(MIN) is derated by subtracting $^{t}JITPER$(MAX), while $^{t}PRPE$(MAX), is derated by subtracting $^{t}JIT_{PER}$(MAX) . The parameter $^{t}RPST$(MAX), is dated by subtracting $^{t}JIT_{DTY}$(MIN).
44. Half-clock output parameters must be derated by the actual $^{t}ERR_{5PER}$ and $^{t}JIT_{DTY}$ when input clock jitter is present; this will result in each parameter becoming larger. The parameter ^{t}AOF(MIN) is required to be derated by subtracting both $^{t}ERR_{5PER}$(MAX) and $^{t}JIT_{PER}$(MAX). The parameter ^{t}AOF(MAX) is required to be derated by subtracting both $^{t}ERR_{5PER}$(MIN) and $^{t}JIT_{DTY}$(MIN).
45. MIN(^{t}CL, ^{t}CH) refers to the smaller of the actual clock LOW time and the actual clock HIGH time driven to the device. The clock's half period must also be of a Gaussian distribution; $^{t}CH_{AVG}$ and $^{t}CL_{AVG}$ must be met with or with our clock jitter and with or without duty cycle jitter. $^{t}CH_{AVG}$ and $^{t}CL_{AVG}$ are the average of any 200 consecutive CK falling edges.
46. ^{t}HP (MIN) is the lesser of ^{t}CL and ^{t}CH actually applied to the device CK and CK# inputs; thus, ^{t}HP(MIN) ≥ the lesser of $^{t}CL_{ABS}$(MIN) and $^{t}CH_{ABS}$(MIN).
47. $^{t}QH = {}^{t}HP - {}^{t}QHS$; the worst case ^{t}QH would be the smaller of $^{t}CL_{ABS}$(MAX) or $^{t}CH_{ABS}$(MAX) times $^{t}CK_{ABS}$(MIN) - ^{t}QHS. Minimizing the amount of $^{t}CH_{AVG}$ offset and value of $^{t}JIT_{DTY}$ will provide a larger ^{t}QH, which in turn will provide a larger valid data out window.
48. JEDEC specifies using $^{t}ERR_{6\text{-}10PER}$ when derating clock-related output timing (notes 43–44). Micron requires less derating by allowing $^{t}ERR_{5PER}$ to be used.
49. Requires 8 ^{t}CK for backward compatibility.

ORDERING INFORMATION FOR D4

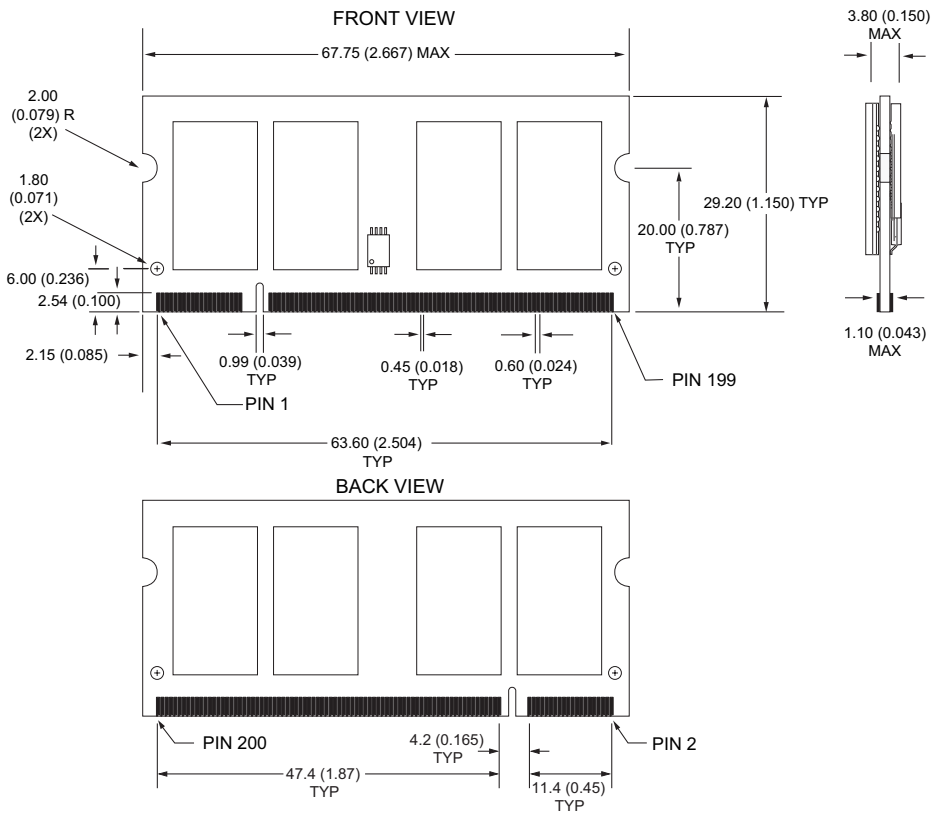
Part Number	Clock/Data Rate Frequency	CAS Latency	t_{RCD}	t_{RP}	Height*
W3HG128M64EEU806D4xxG**	400MHz/800Mb/s	6	6	6	29.20mm (1.150") TYP
W3HG128M64EEU665D4xxG*	333MHz/667Mb/s	5	5	5	29.20mm (1.150") TYP
W3HG128M64EEU534D4xxG	266MHz/533Mb/s	4	4	4	29.20mm (1.150") TYP
W3HG128M64EEU403D4xxG	200MHz/400Mb/s	3	3	3	29.20mm (1.150") TYP

** Consult Factory for availability

NOTES:

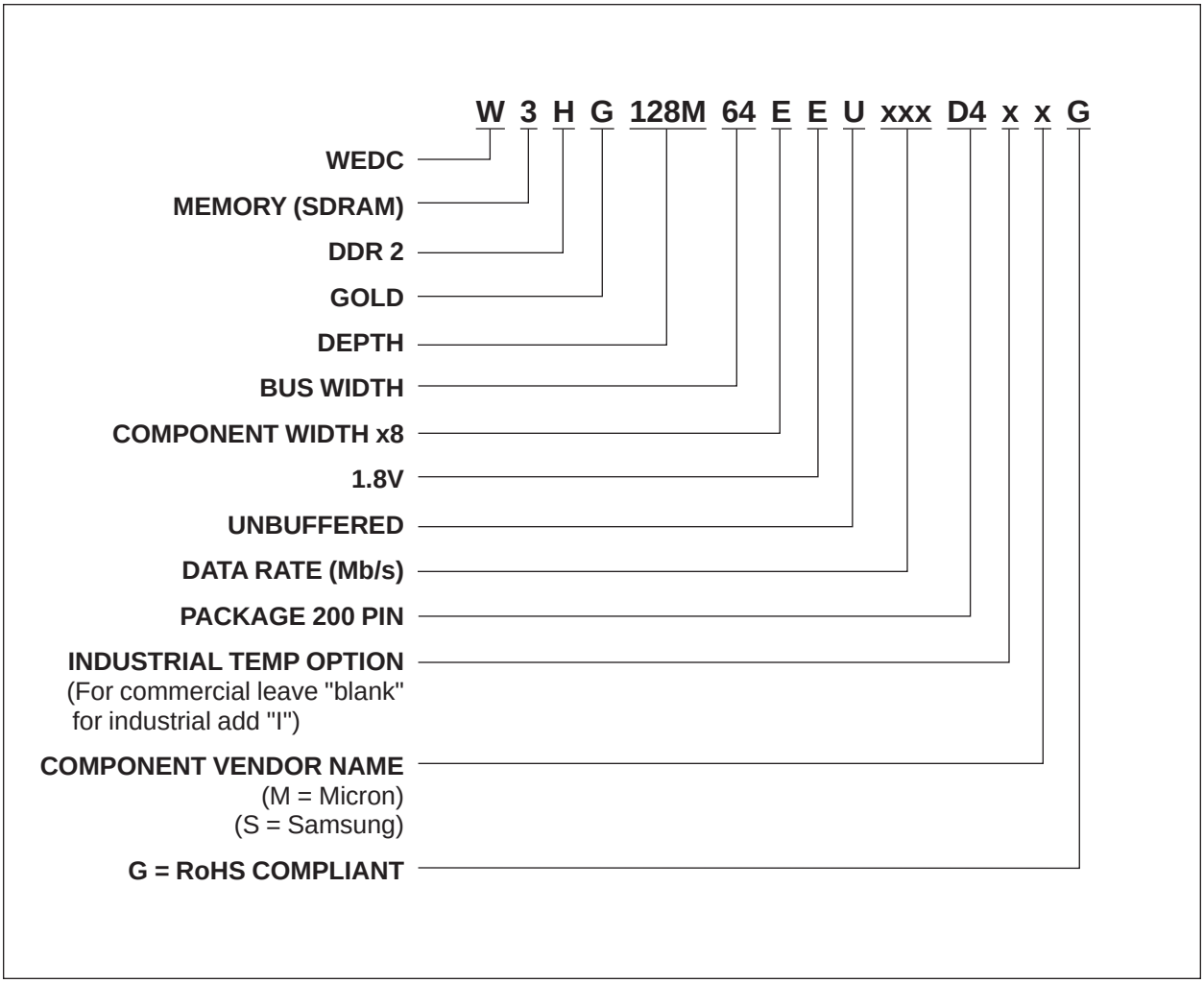
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D4



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

1GB – 128Mx64 DDR2 SDRAM UNBUFFERED

DRAM DIE OPTIONS:

- SAMSUNG: A-Die, will move to B-Die Q3'06
- MICRON: U38A:A, will move to U38Z:D Q4'06, and U48B:E Q2'07

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	3-06	Advanced
Rev 1	1.0 Update part number guide	4-06	Advanced
	1.1 Added indicator "x" in part number for industrial temp option		
	1.2 Added DRAM die option		
Rev 2	2.0 Updated AC title to indicate component AC specs only	11-06	Advanced