

## 2N5020, 2N5021

## P-Channel Silicon Junction Field-Effect Transistor

## • Analog Switches

Absolute maximum ratings at  $T_A = 25^\circ\text{C}$ 

Reverse Gate Source & Reverse Gate Drain Voltage	- 50 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	500 mW
Power Derating	4 mW/°C
Storage Temperature Range	- 65°C to + 200°C

At 25°C free air temperature:

## Static Electrical Characteristics

		2N5020		2N5021		Unit	Process PJ32	
		Min	Max	Min	Max		Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GDO}$	25		25		V	$I_G = 1\ \mu\text{A}, V_{DS} = 0\text{V}$	
Gate Reverse Current	$I_{GSS}$		1		1	nA	$V_{GS} = 15\text{V}, V_{DS} = 0\text{V}$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	0.3	1.5	0.5	2.5	V	$V_{DS} = -15\text{V}, I_D = 1\ \text{nA}$	
Drain Saturation Current (Pulsed)	$I_{DSS}$	- 0.3	- 1.2	- 1	- 3.5	mA	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$	

## Dynamic Electrical Characteristics

Common Source Forward Transconductance	$g_{fs}$	1	3.5	1.5	6	mS	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$	
Common Source Output Conductance	$g_{os}$		20		20	$\mu\text{S}$	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$	
Common Source Input Capacitance	$C_{iss}$		25		25	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ f = 1 MHz	
Common Source Reverse Transfer Capacitance	$C_{rss}$		7		7	pF	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$ f = 1 MHz	

## TO-18 Package

Dimensions in Inches (mm)

## Pin Configuration

1 Source 1, 2 Gate &amp; Case, 3 Drain

## Surface Mount

SMP5020, SMP5021



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