128Mb SDRAM Specification

P2V28S20DTP-7,-75,-8
P2V28S30DTP-7,-75,-8
P2V28S40DTP-7,-75,-8

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P2V28S20ATP-7,-75,-8 (4-BANK x 8,388,608-WORD x 4-BIT)
P2V28S30ATP-7,-75,-8 (4-BANK x 4,194,304-WORD x 8-BIT)
P2V28S40ATP-7,-75,-8 (4-BANK x 2,097,152-WORD x 16-BIT)

PRELIMINARY Some of contents are described for general products and are subject to change without notice.

DESCRIPTION

P2V28S20ATP is organized as 4-bank x 8,388,608-word x 4-bit Synchronous DRAM with LVTTL interface and P2V28S30ATP is organized as 4-bank x 4,194,304-word x 8-bit and P2V28S40ATP is organized as 4-bank x 2,097,152-word x 16-bit. All inputs and outputs are referenced to the rising edge of CLK.

P2V28S20ATP,P2V28S30ATP and P2V28S40ATP achieve very high speed data rates up to 166MHz, and are suitable for main memories or graphic memories in computer systems.

FEATURES

ITEM				P2V28S20/30/40ATP		
				-7	-75	-8
tCLK	Clock Cycle Time	(Min.)	CL=2	-	10ns	10ns
			CL=3	7ns	7.5ns	8ns
tRAS	Active to Precharge Command Period	(Min.)		45ns	45ns	48ns
tRCD	Row to Column Delay	(Min.)		20ns	20ns	20ns
tAC	Access Time from CLK	(Max.)	CL=2	-	6ns	6ns
			CL=3	5.4ns	5.4ns	6ns
tRC	Ref /Active Command Period	(Min.)		63ns	67.5ns	70ns
Icc1	Operation Current (Single Bank)	(Max.)	V28S20D	85mA	85mA	85mA
			V28S30D	85mA	85mA	85mA
			V28S40D	85mA	85mA	85mA
Icc6	Self Refresh Current	(Max.)	-7,-75,-8	1mA	1mA	1mA

- Single 3.3V ±0.3V power supply
- Max. Clock frequency -7:143MHz<3-3-3>/-75:133MHz<3-3-3>/-8:100MHz<2-2-2>
- Fully synchronous operation referenced to clock rising edge
- 4-bank operation controlled by BA0,BA1(Bank Address)
- /CAS latency- 2/3 (programmable)
- Burst length- 1/2/4/8/FP (programmable)
- Burst type- Sequential and interleave burst (programmable)
- Byte Control- DQML and DQMU (P2V28S40ATP)
- Random column access
- Auto precharge / All bank precharge controlled by A10
- Auto and self refresh
- 4096 refresh cycles /64ms
- LVTTL Interface
- Package

  P2V28S20ATP/30ATP/40ATP

  400-mil, 54-pin Thin Small Outline (TSOP II) with 0.8mm lead pitch

PIN CONFIGURATION (TOP VIEW)

P2V28S20ATP

P2V28S30ATP

P2V28S40ATP

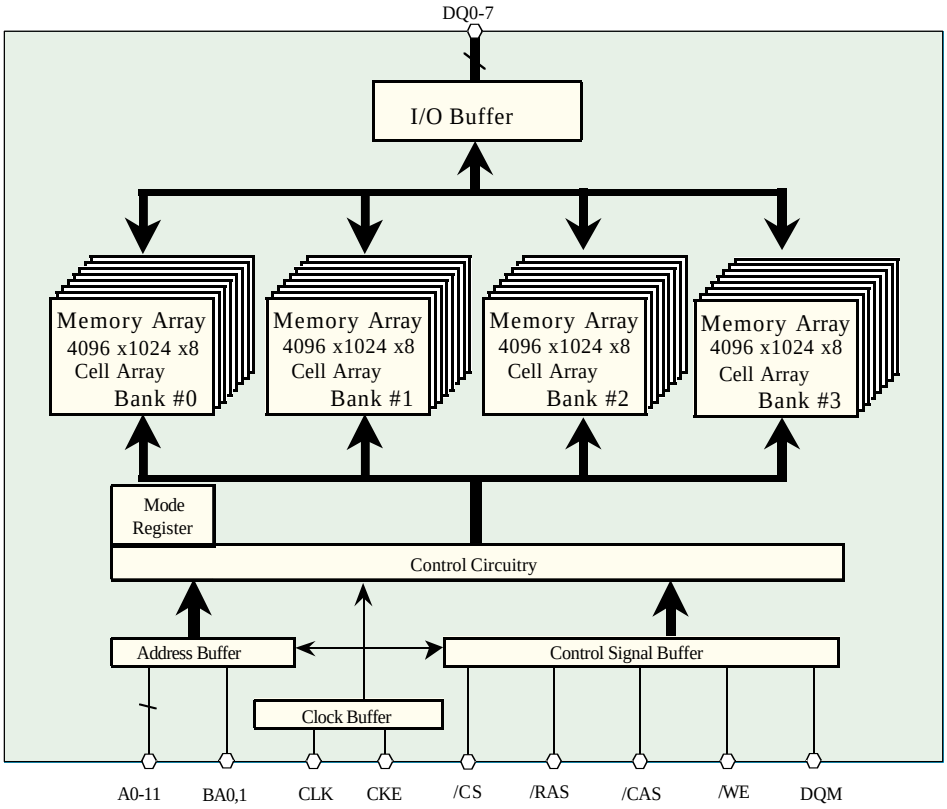
PIN CONFIGURATION (TOP VIEW)

Vdd	Vdd	Vdd	1	54	Vss	Vss	Vss
NC	DQ0	DQ0	2	53	DQ15	DQ7	NC
VddQ	VddQ	VddQ	3	52	VssQ	VssQ	VssQ
NC	NC	DQ1	4	51	DQ14	NC	NC
DQ0	DQ1	DQ2	5	50	DQ13	DQ6	DQ3
VssQ	VssQ	VssQ	6	49	VddQ	VddQ	VddQ
NC	NC	DQ3	7	48	DQ12	NC	NC
NC	DQ2	DQ4	8	47	DQ11	DQ5	NC
VddQ	VddQ	VddQ	9	46	VssQ	VssQ	VssQ
NC	NC	DQ5	10	45	DQ10	NC	NC
DQ1	DQ3	DQ6	11	44	DQ9	DQ4	DQ2
VssQ	VssQ	VssQ	12	43	VddQ	VddQ	VddQ
NC	NC	DQ7	13	42	DQ8	NC	NC
Vdd	Vdd	Vdd	14	41	Vss	Vss	Vss
NC	NC	DQML	15	40	NC	NC	NC
/WE	/WE	/WE	16	39	DQMU	DQM	DQM
/CAS	/CAS	/CAS	17	38	CLK	CLK	CLK
/RAS	/RAS	/RAS	18	37	CKE	CKE	CKE
/CS	/CS	/CS	19	36	NC	NC	NC
BA0(A13)	BA0(A13)	BA0(A13)	20	35	A11	A11	A11
BA1(A12)	BA1(A12)	BA1(A12)	21	34	A9	A9	A9
A10(AP)	A10(AP)	A10(AP)	22	33	A8	A8	A8
A0	A0	A0	23	32	A7	A7	A7
A1	A1	A1	24	31	A6	A6	A6
A2	A2	A2	25	30	A5	A5	A5
A3	A3	A3	26	29	A4	A4	A4
Vdd	Vdd	Vdd	27	28	Vss	Vss	Vss

400mil 54pin TSOP(II)

CLK	***: Master Clock***	***DQM***	***: Output Disable / Write Mask***
CKE	***: Clock Enable***	***A0-11***	***: Address Input***
/CS	***: Chip Select***	***BA0,1***	***: Bank Address***
/RAS	***: Row Address Strobe***	***Vdd***	***: Power Supply***
/CAS	***: Column Address Strobe***	***VddQ***	***: Power Supply for Output***
/WE	***: Write Enable***	***Vss***	***: Ground***
DQ0-15	***: Data I/O***	***VssQ***	***: Ground for Output***

BLOCK DIAGRAM



Note:This figure shows the P2V28S30ATP
The A2V28S20ATP configuration is 4096x2048x4 of cell array and DQ0-3
The A2V28S40ATP configuration is 4069x512x16 of cell array and DQ0-15

Type Designation Code

P2 V 28 S 3 0 A TP -8

Access Item	-7 : 7 ns (143MHz/3-3-3) -75 : 7.5ns (100MHz/2-2-2 or 133MHz/3-3-3) -8 : 8 ns (100MHz/2-2-2 or 125MHz/3-3-3)
Package Type	TP : TSOP(II)
Process Generation	A : 2nd generation
Function	0 : Random Column
Organization	2 : x4, 3 : x8, 4: x16
Synchronous DRAM	
Density	128 :128Mbit
Interface	V :LVTTL
PSC DRAM	

PIN FUNCTION

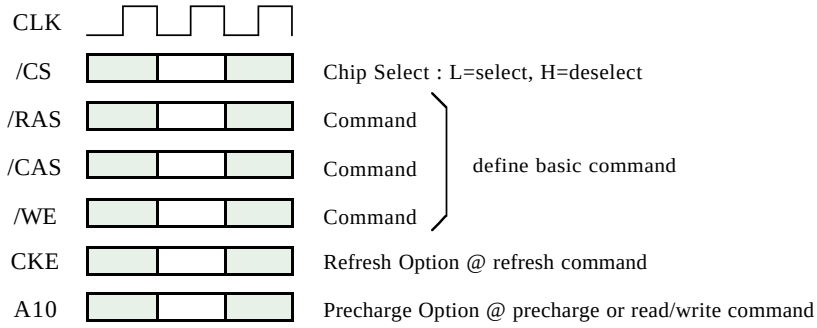
CLK	Input	Master Clock: All other inputs are referenced to the rising edge of CLK
CKE	Input	Clock Enable: CKE controls internal clock.When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self-refresh. After self-refresh mode is started, CKE becomes asynchronous input. Self-refresh is maintained as long as CKE is low.
/CS	Input	Chip Select: When /CS is high, any command means No Operation.
/RAS, /CAS, /WE	Input	Combination of /RAS, /CAS, /WE defines basic commands.
A0-11	Input	A0-11 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-11. The Column Address is specified by A0-9,11(x4)/A0-9(x8)/A0-8(x16). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged.
BA0,1	Input	Bank Address: BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE , READ , WRITE commands.
DQ0-3(x4), DQ0-7(x8), DQ0-15(x16)	Input / Output	Data In and Data out are referenced to the rising edge of CLK.
DQM(x4,x8), DQMU/L(x16)	Input	Din Mask / Output Disable: When DQM(U/L) is high in burst write, Din for the current cycle is masked. When DQM(U/L) is high in burst read, Dout is disabled at the next but one cycle.
Vdd, Vss	Power Supply	Power Supply for the memory array and peripheral circuitry.
VddQ, VssQ	Power Supply	VddQ and VssQ are supplied to the Output Buffers only.

BASIC FUNCTIONS

The P2V28S20 , 30 and 40ATP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS, /CAS and /WE at CLK rising edge. In addition to 3 signals, /CS ,CKE and A10 are used as chip select, refresh opt ion, and precharge option, respectively .

To know the detailed definition of commands, please see the command truth table.



Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**).

Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	BA0,1	A11	A10	A0-9
Deselect	DESEL	H	X	H	X	X	X	X	X	X	X
No Operation	NOP	H	X	L	H	H	H	X	X	X	X
Row Address Entry & Bank Active	ACT	H	X	L	L	H	H	V	V	V	V
Single Bank Precharge	PRE	H	X	L	L	H	L	V	X	L	X
Precharge All Banks	PREA	H	X	L	L	H	L	X	X	H	X
Column Address Entry &Write	WRITE	H	X	L	H	L	L	V	V	L	V
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	V	H	V
Column Address Entry & Read	READ	H	X	L	H	L	H	V	V	L	V
Column Address Entry & Read with Auto-Precharge	READA	H	X	L	H	L	H	V	V	H	V
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	X
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	X
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	X
		L	H	L	H	H	H	X	X	X	X
Burst Terminate	TBST	H	X	L	H	H	L	X	X	X	X
Mode Register Set	MRS	H	X	L	L	L	L	L	L	L	V*1

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

NOTE: 1. A7-A9 =0, A0-A6 =Mode Address

FUNCTION TRUTH TABLE

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	Bank Active, Latch RA
	L	L	H	L	BA, A10	PRE / PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	NOP
	L	H	L	H	BA, CA, A10	READ / READA	Begin Read, Latch CA, Determine Auto-Precharge
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Begin Write, Latch CA, Determine Auto-Precharge
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Precharge / Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
READ	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst
	L	H	L	H	BA, CA, A10	READ /READA	Terminate Burst, Latch CA,Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA,Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	Terminate Burst, Latch CA,Begin
	L	H	L	H	BA, CA, A10	READ / READA	Terminate Burst, Latch CA,Begin Read, Determine Auto-Precharge*3
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	Terminate Burst, Latch CA,Begin Write, Determine Auto-Precharge*3
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	Terminate Burst, Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP (Continue Burst to END)
	L	H	H	H	X	NOP	NOP (Continue Burst to END)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ / READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRITE / WRITEA	ILLEGAL
	L	L	H	H	BA, RA	ACT	Bank Active / ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP (Idle after tRP)
	L	H	H	H	X	NOP	NOP (Idle after tRP)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	NOP*4 (Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP (Row Active after tRCD)
	L	H	H	H	X	NOP	NOP (Row Active after tRCD)
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
WRITE RECOVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	BA	TBST	ILLEGAL*2
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL*2
	L	L	H	H	BA, RA	ACT	ILLEGAL*2
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
REFRESHING	H	X	X	X	X	DESEL	NOP (Idle after tRC)
	L	H	H	H	X	NOP	NOP (Idle after tRC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE (continued)

Current State	/CS	/RAS	/CAS	/WE	Address	Command	Action
MODE REGISTER SETTING	H	X	X	X	X	DESEL	NOP (Idle after tRSC)
	L	H	H	H	X	NOP	NOP (Idle after tRSC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA, CA, A10	READ / WRITE	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE / PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE for CKE

Current State	CKE n-1	CKE n	/CS	/RAS	/CAS	/WE	Add	Action
SELF-REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh (Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP (Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP (Maintain Power Down)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State =Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CLK Susspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CLK Susspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CLK Suspend

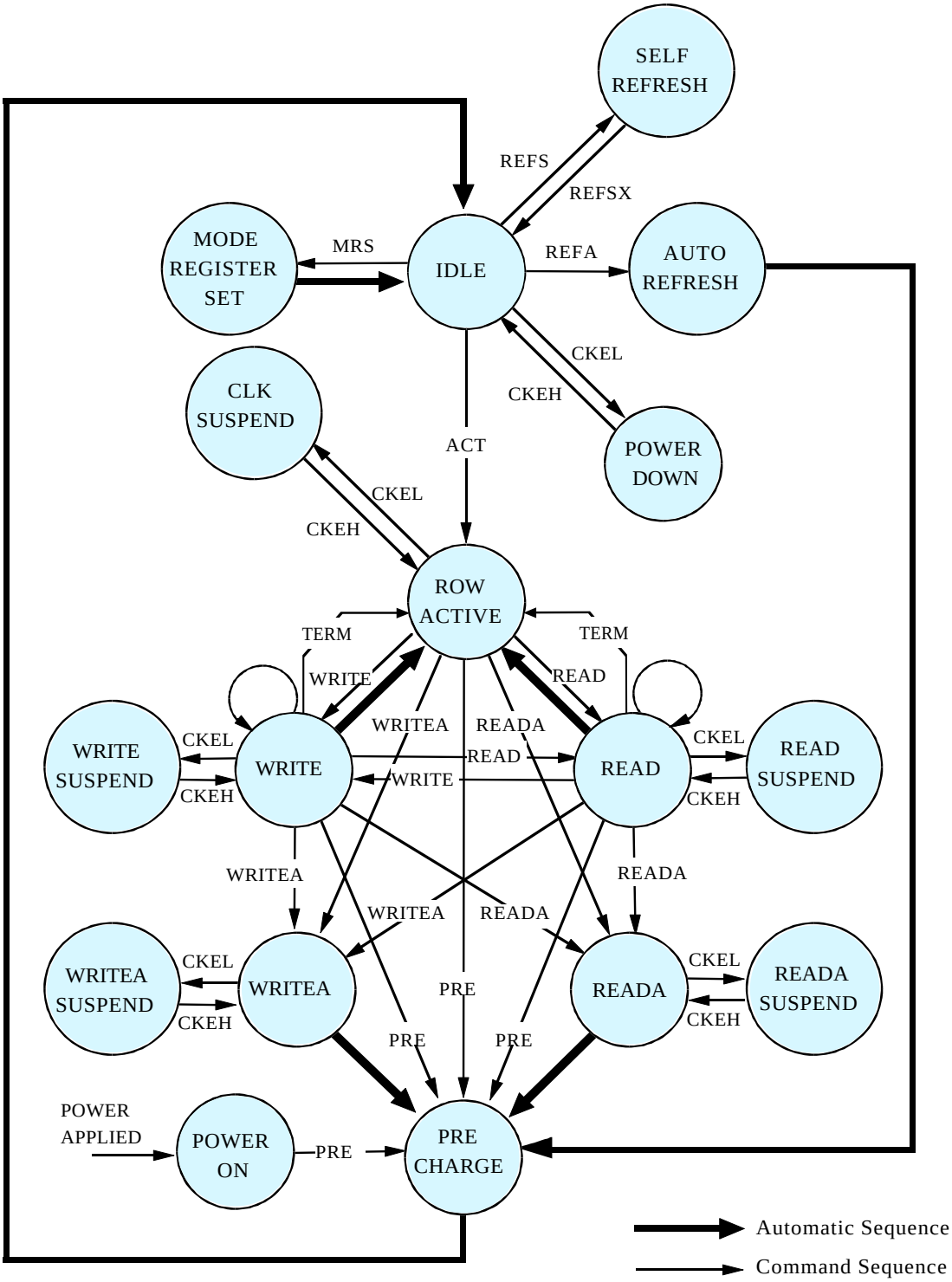
ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

NOTES:

1. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

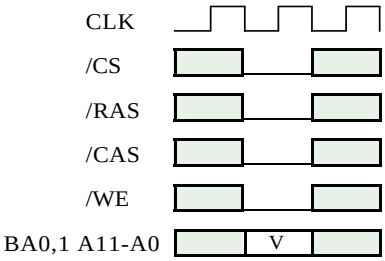
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when all banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	0	0	LTMODE			BT	BL		

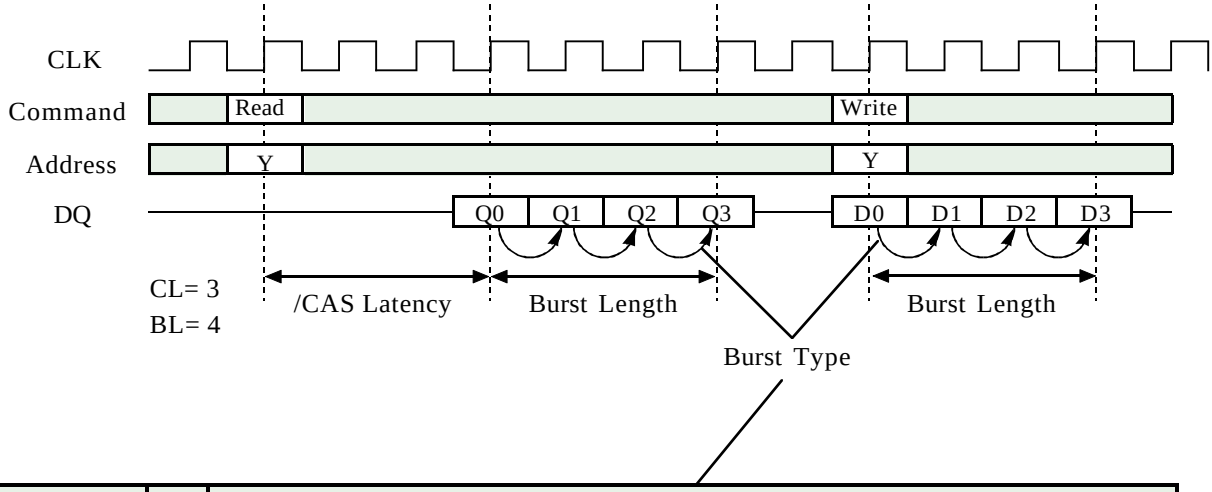
LATENCY MODE	CL	/CAS LATENCY
	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	3
	1 0 0	R
	1 0 1	R
	1 1 0	R
	1 1 1	R

BURST LENGTH	BL	BT= 0	BT= 1
	0 0 0	1	1
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	FP	R

BURST TYPE		
	0	SEQUENTIAL
	1	INTERLEAVED

R: Reserved for Future Use

FP: Full Page



Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATIONAL DESCRIPTION

BANK ACTIVATE

The SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row addresses A0-11. The minimum activation interval between one bank and the other bank is tRRD. Maximum 2 ACT commands are allowed within tRC , although the number of banks which are active concurrently is not limited.

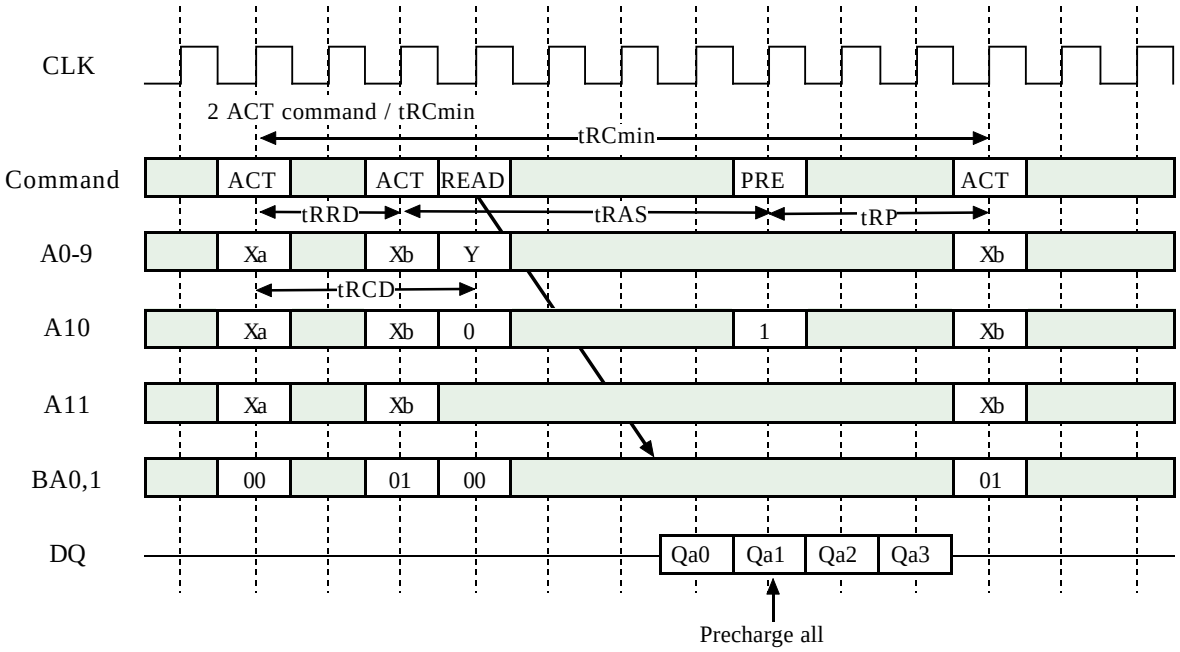
PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA, PRE + A10=H) is available to deactivate them at the same time.
After tRP from the precharge, an ACT command to the same bank can be issued.

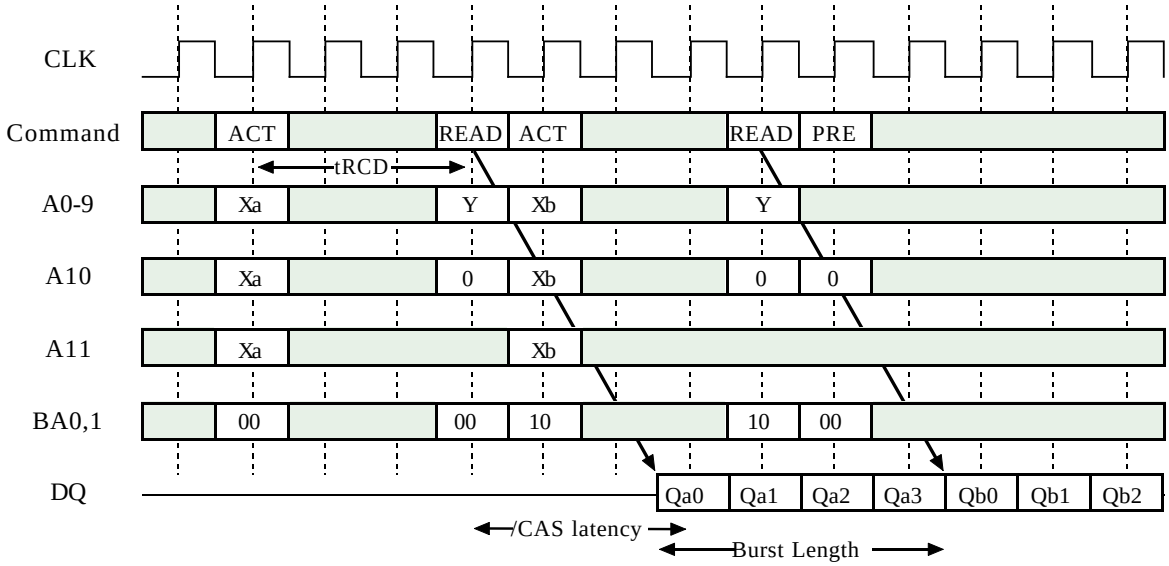
READ

After tRCD from the bank activation, a READ command can be issued. 1st output data is available after the /CAS Latency from the READ, followed by (BL -1) consecutive data when the Burst Length is BL. The start address is specified by A0-A9(x4), A0-8(X8), A0-7 (X16) , and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, TBST, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL after READA. (Need to keep tRAS min.) The next ACT command can be issued after (BL + tRP) from the previous READA.

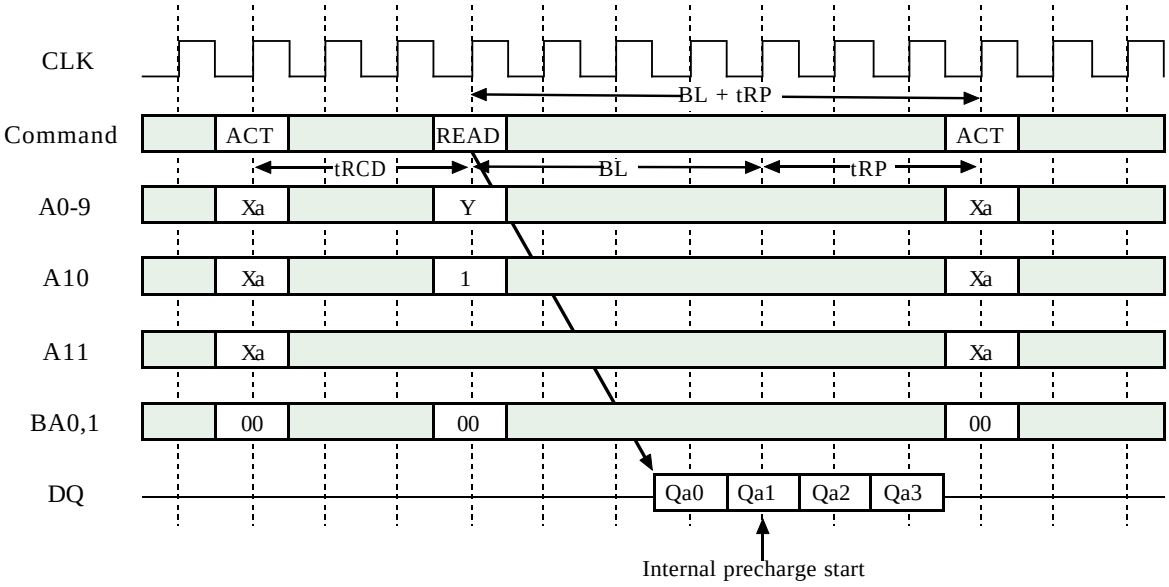
Bank Activation and Precharge All (BL=4, CL=3)



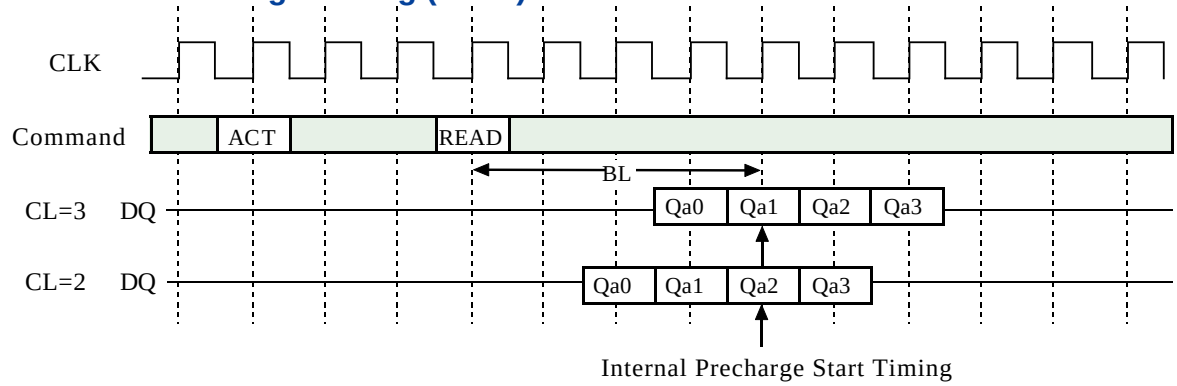
Multi Bank Interleaving READ (BL=4, CL=3)



READ with Auto-Precharge (BL=4, CL=3)



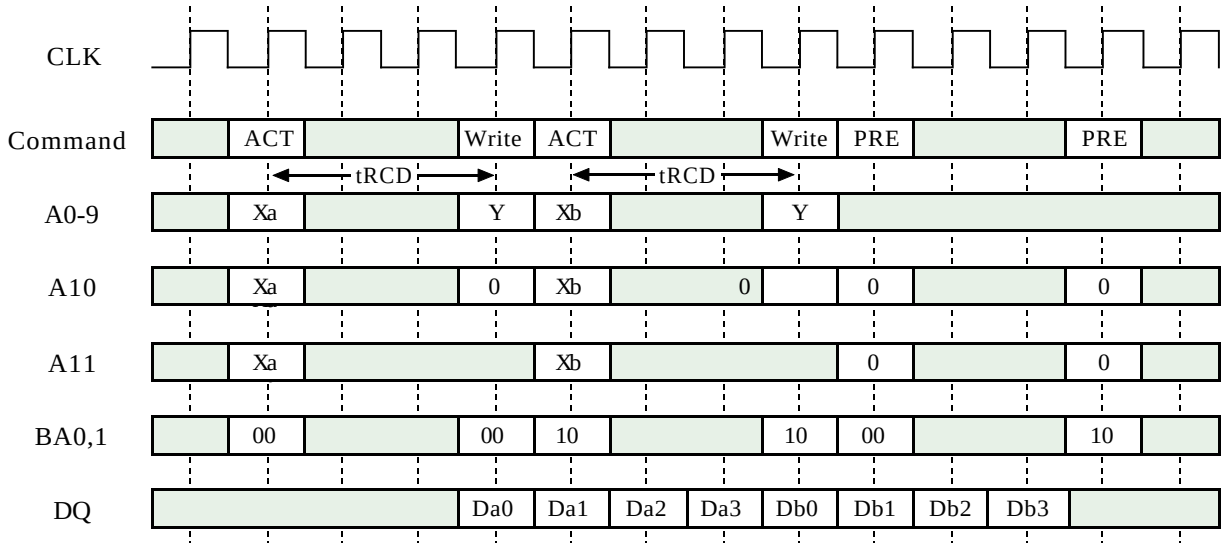
READ Auto-Precharge Timing (BL=4)



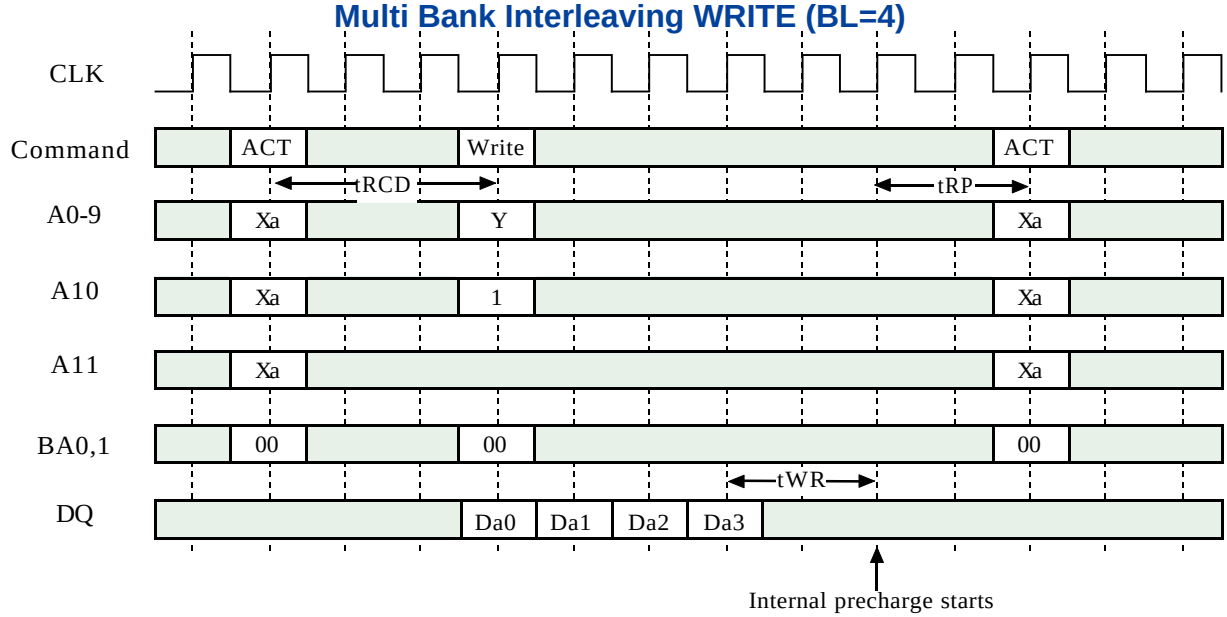
WRITE

After tRCD from the bank activation, a WRITE command can be issued. 1st input data is set at the same cycle as the WRITE. Following (BL -1) data are written into the RAM, when the Burst Length is BL. The start address is specified by A0-A9(x4), A0-8(X8), A0-7(X16) and the address sequence of burst data is defined by the Burst Type. A WRITE command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous input data by interleaving the multiple banks. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, the autoprecharge (WRITEA) is performed. Any command (READ, WRITE, PRE, TBST, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge begins at tWR after the last input data cycle. (Need to keep tRAS min.) The next ACT command can be issued after tRP from the internal precharge timing.

WRITE with Auto-Precharge (BL=4)



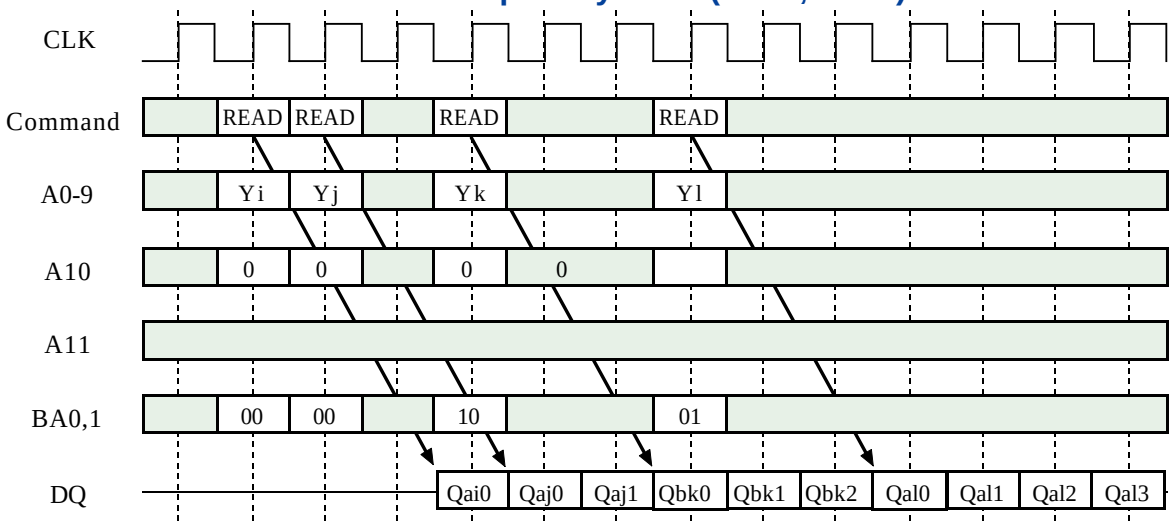
Multi Bank Interleaving WRITE (BL=4)



BURST INTERRUPTION [Read Interrupted by Read]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed READ to READ interval is minimum 1 CLK..

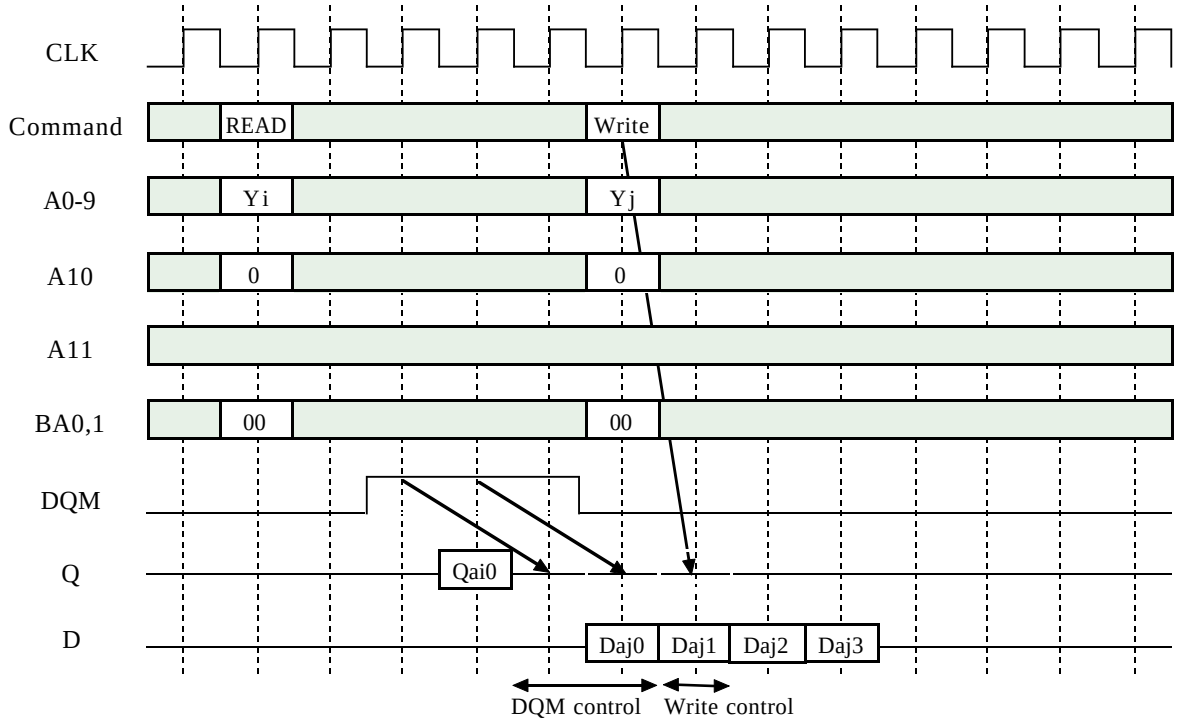
Read Interrupted by Read (BL=4, CL=3)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of any bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 1 cycle after WRITE assertion.

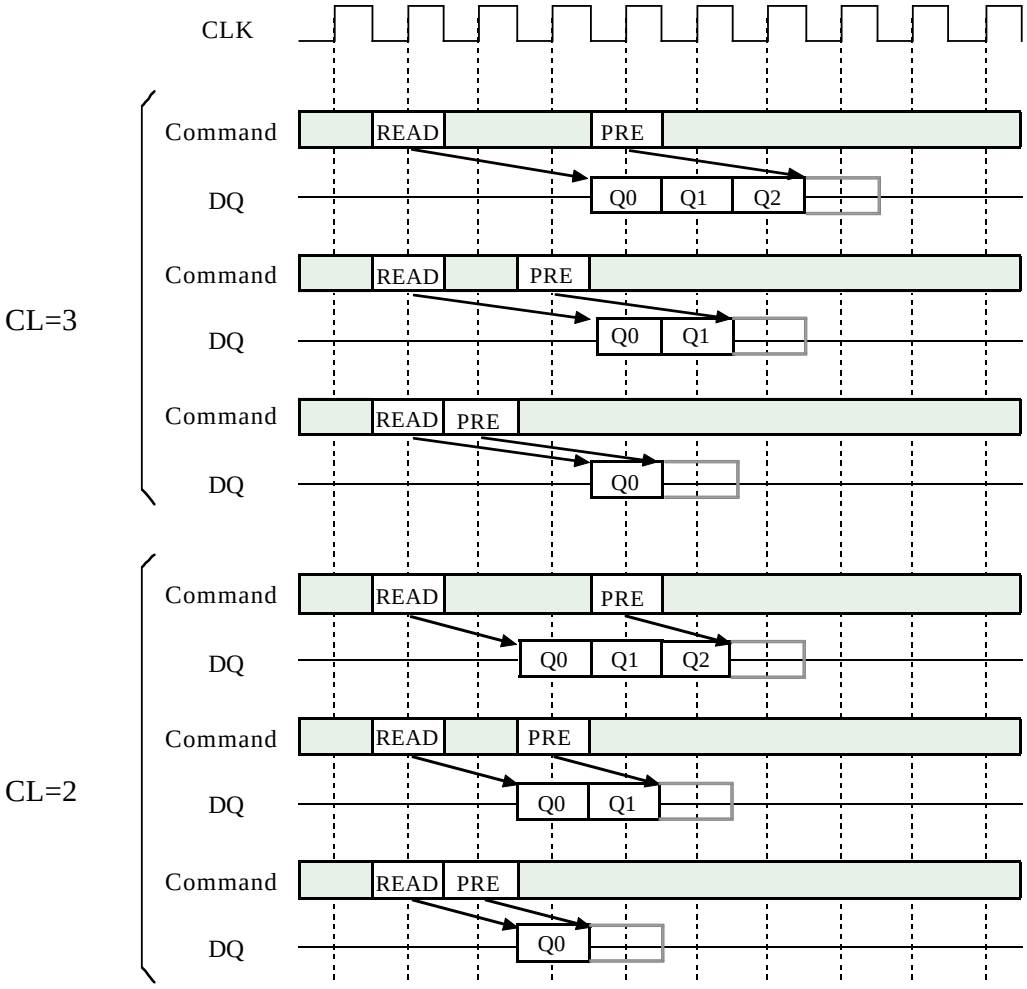
Read Interrupted by Write (BL=4, CL=3)



[Read Interrupted by Precharge]

Burst read operation can be interrupted by precharge of the same bank . READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=4.

Read Interrupted by Precharge (BL=4)

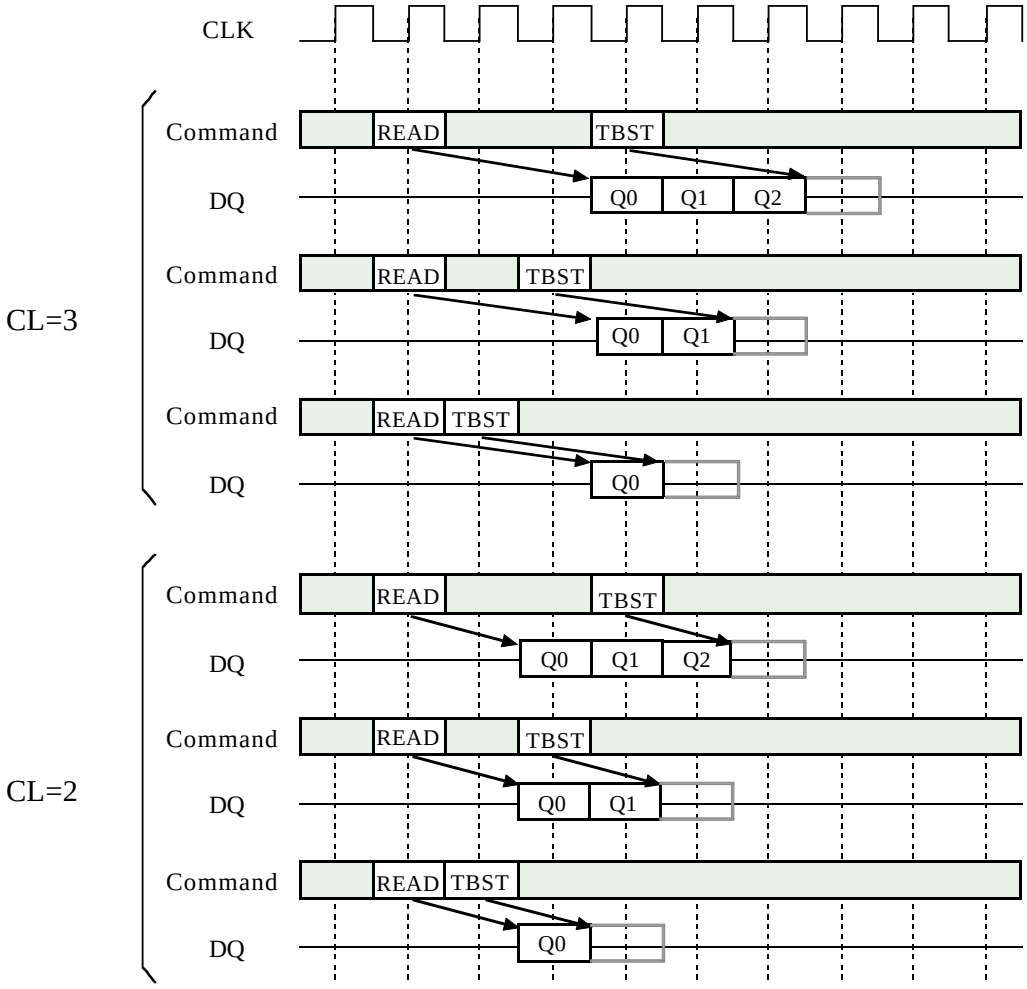


[Read Interrupted by Burst Terminate]

Similarly to the precharge, a burst terminate command can interrupt the burst read operation and disable the data output. The terminated bank remains active.

READ to TBST interval is minimum 1 CLK. A TBST command to output disable latency is equivalent to the /CAS Latency.

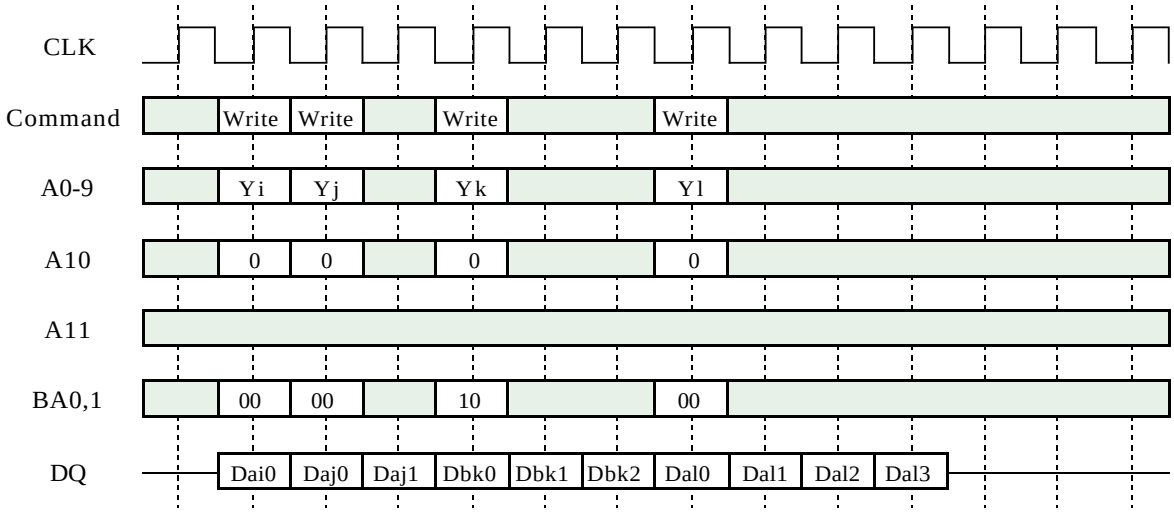
Read Interrupted by Terminate (BL=4)



[Write Interrupted by Write]

Burst write operation can be interrupted by new write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

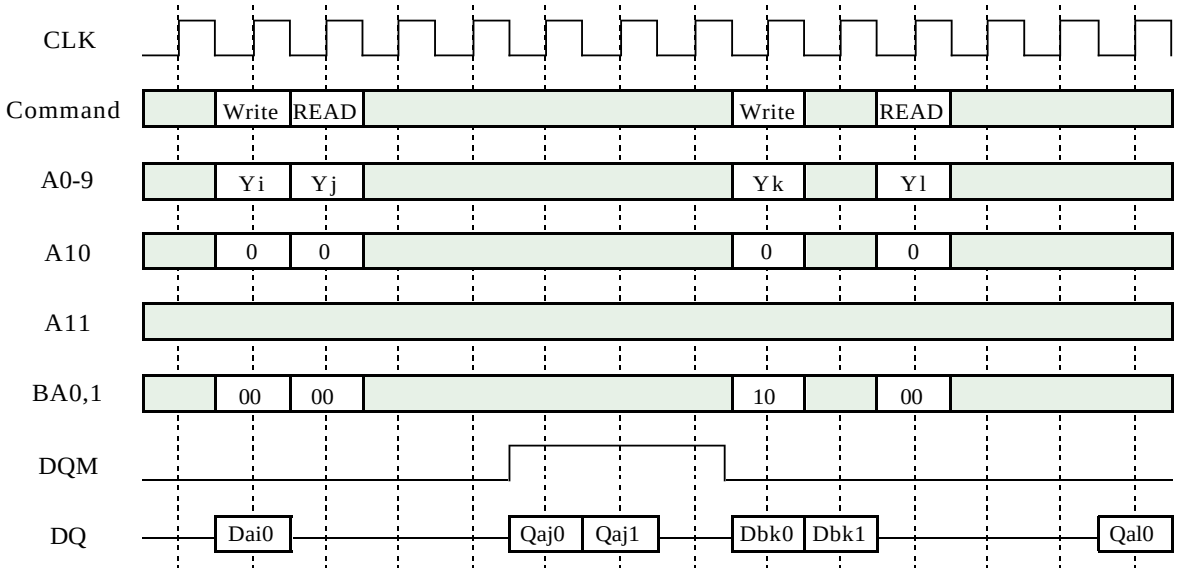
Write Interrupted by Write (CL=3,BL=4)



[Write Interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care".

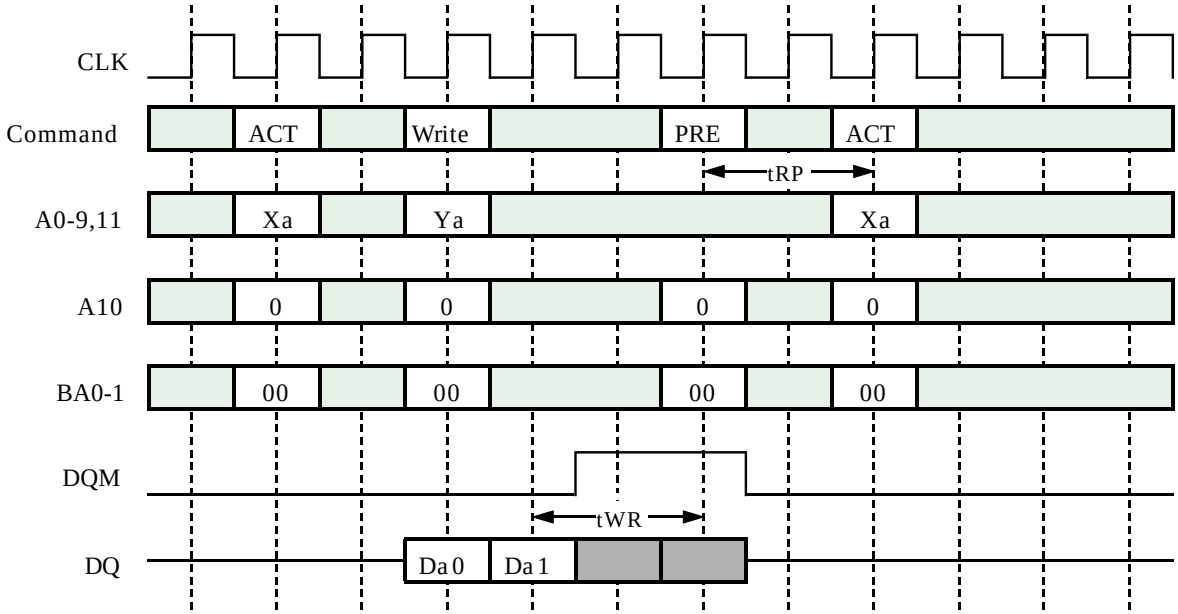
Write Interrupted by Read (CL=3,BL=4)



[Write Interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same bank.Write recovery time(tWR) is required from the last data to PRE command. During write recovery, data inputs must be masked by DQM.

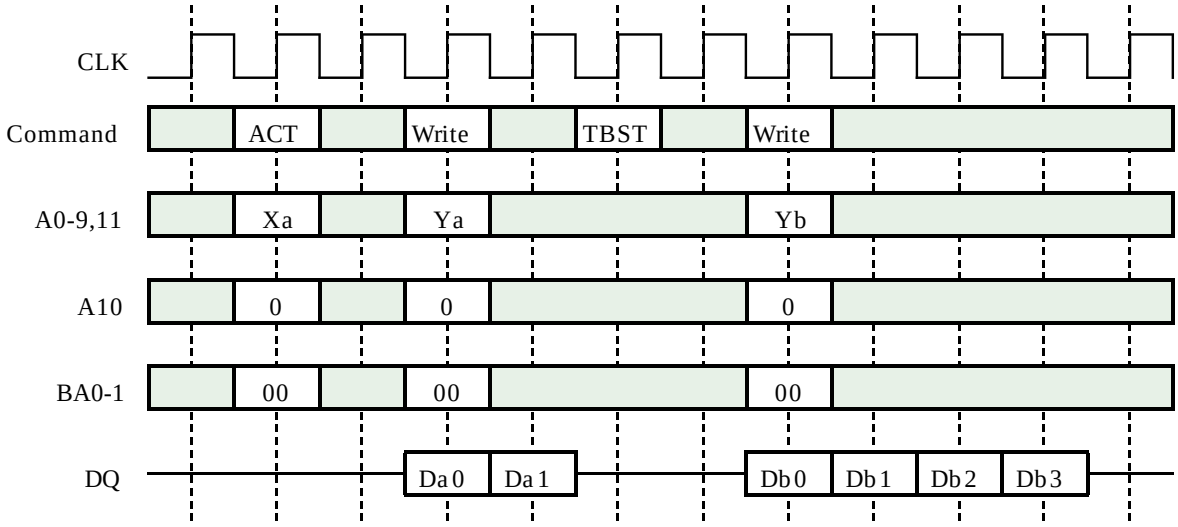
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

Burst terminate command can terminate burst write operation.In this case, the write recovery time is not required and the bank remains active. WRITE to TBST interval is minimum 1 CLK.

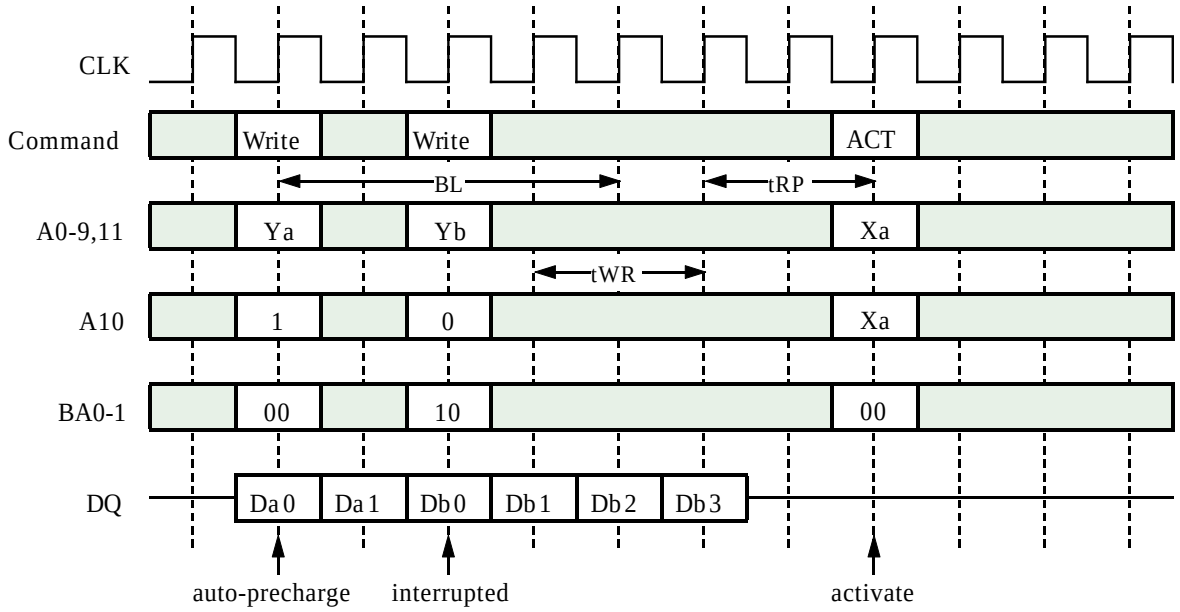
Write Interrupted by Terminate (BL=4)



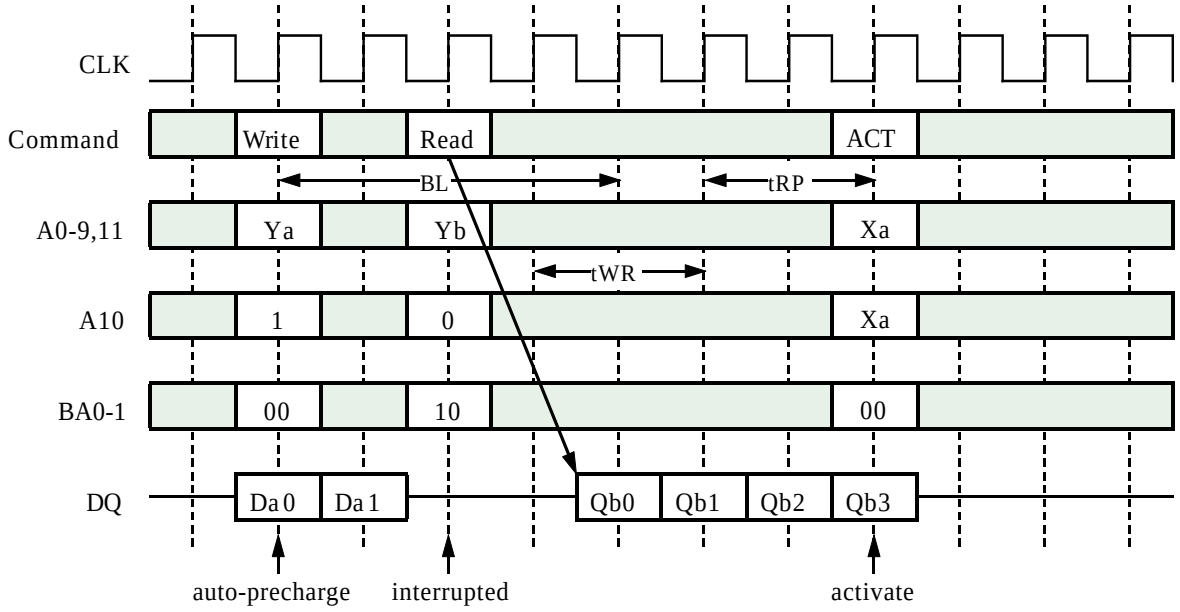
[Write with Auto-Precharge Interrupted by Write or Read to another Bank]

Burst write with auto-precharge can be interrupted by write or read to another bank. Next ACT command can be issued after tRP. Auto-precharge interruption by a command to the same bank is inhibited.

Write Interrupted by WRITE to another bank (BL=4)



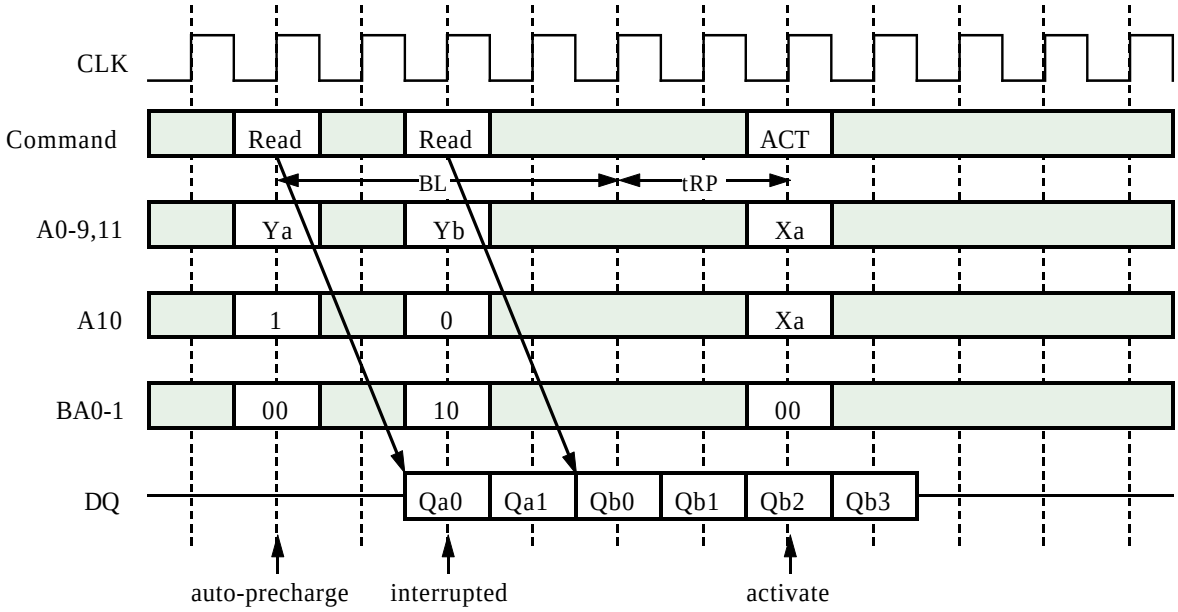
Write Interrupted by READ to another bank (CL=2,BL=4)



[Read with Auto-Precharge Interrupted by Read to another Bank]

Burst write with auto-precharge can be interrupted by write or read to another bank. Next ACT command can be issued after tRP. Auto-precharge interruption by a command to the same bank is inhibited.

Read Interrupted by Read to another bank (CL=2,BL=4)



[Full Page Burst]

Full page burst length is available for only the sequential burst type. Full page burst read or write is repeated untill a Precharge or a Burst Terminate command is issued. In case of the full page burst, a read or write with auto-precharge command is illegal.

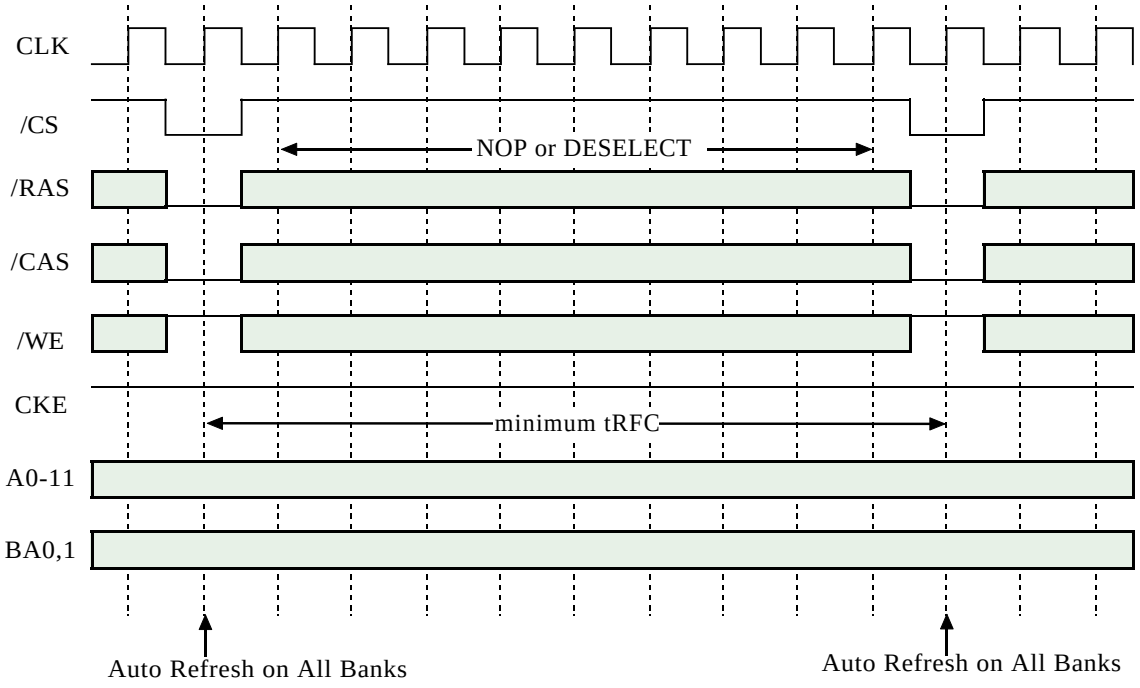
[Single Write]

When single write mode is set, burst length for write is always one, independently of Burst Length defined by (A2-0).

AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA (/CS= /RAS= /CAS= L, /WE= /CKE= H) command. The refresh address is generated internally. 4096 REFA cycles within 64ms refresh 64M bit memory cells. The auto-refresh is performed on 4 banks concurrently. Before performing an auto-refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRC. Any command must not be supplied to the device before tRC from the REFA command.

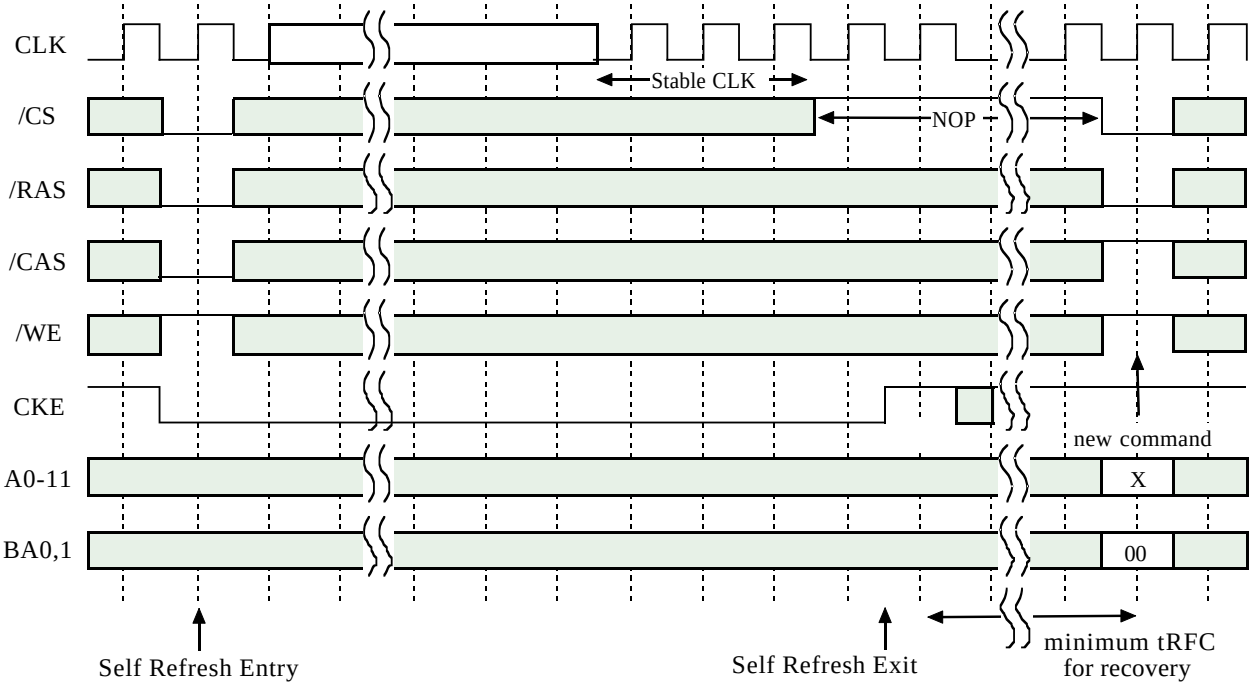
Auto-Refresh



SELF REFRESH

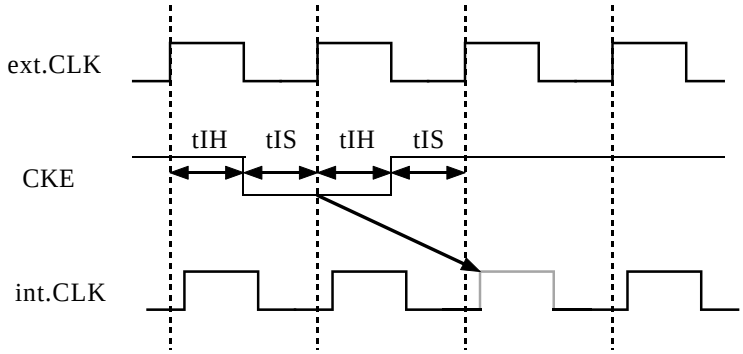
Self-refresh mode is entered by issuing a REFS command (/CS= /RAS= /CAS= L, /WE= H, CKE= L). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input ,all other inputs including CLK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE=H. After tRC from the 1st CLK egde following CKE=H, all banks are in the idle state and a new command can be issued, but DESEL or NOP commands must be asserted till then.

Self-Refresh

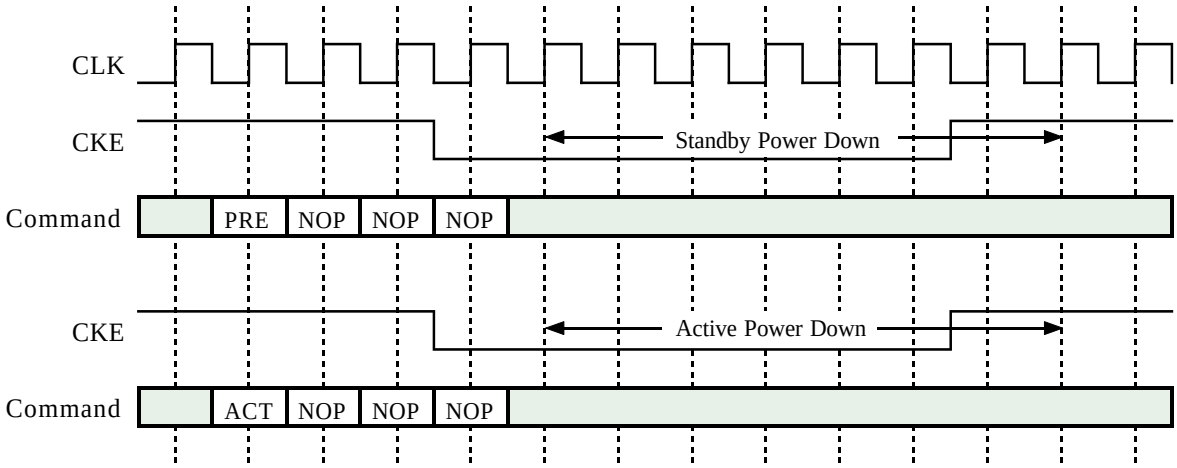


CLK SUSPEND

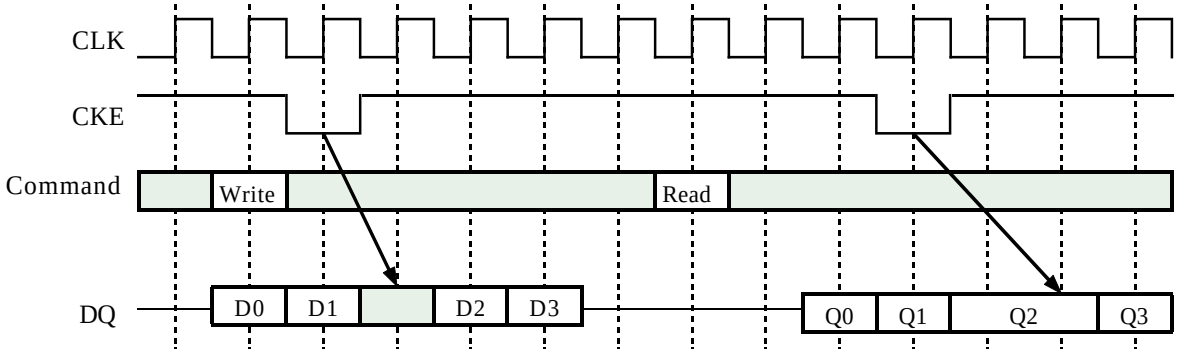
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



Power Down by CKE



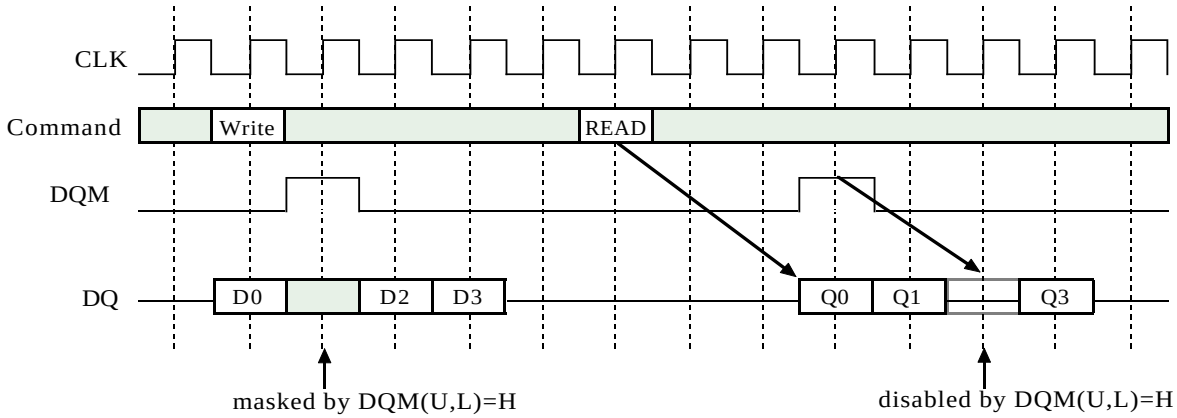
DQ Suspend by CKE (CL=2)



DQM CONTROL

DQM is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQM(U,L) masks input data word by word. DQM(U,L) to write mask latency is 0. During reads, DQM(U,L) forces output to Hi-Z word by word. DQM(U,L) to output Hi-Z latency is 2.

DQM Function(CL=3)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 - 4.6	V
VddQ	Supply Voltage for Output	with respect to VssQ	-0.5 - 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 - 4.6	V
VO	Output Voltage	with respect to VssQ	-0.5 - 4.6	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta = 25˚C	1000	mW
Topr	Operating Temperature		0 - 70	˚C
Tstg	Storage Temperature		-65 - 150	˚C

RECOMMENDED OPERATING CONDITIONS

(Ta=0 - 70 ˚C ,unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0		V
VddQ	Supply Voltage for output	3.0	3.3	3.6	V
VssQ	Supply Voltage for output	0	0	0	V
VIH*1	High-Level Input Voltage all inputs	2.0		VddQ +0.3	V
VIL*2	Low-level Input Voltage all inputs	-0.3		0.8	V

NOTES:
1. VIH(max)=5.5V for pulse width less than 10ns.
2. VIL(min)=-1.0V for pulse width less than 10ns.

CAPACITANCE

(Ta=0 -70˚C,Vdd=VddQ=3.3±0.3V,Vss=VssQ=0V,unless otherwise noted)

Symbol	Parameter	Test Condition	Limits (min.)	Limits (max.)		Unit
				-7	-75/-8	
CI(A)	Input Capacitance, address pin	@ 1MHz 1.4V bias 200mV swing Vcc=3.3V	2.5	3.8	5.0	pF
CI(C)	Input Capacitance, contorl pin		2.5	3.8	5.0	pF
CI(K)	Input Capacitance, CLK pin		2.5	3.5	4.0	pF
CI/O	Input Capacitance, I/O pin		4.0	6.5	6.5	pF

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 - 70˚C, Vdd=VddQ=3.3±0.3V,Vss=VssQ=0V, unless otherwise noted)

ITEM	Symbol		Organi-zation	Limits (max.)			Unit
				-7	-75	-8	
Operating current	Icc1	tRC=min, tCLK=min BL=1,IOL=0mA	x4/x8/x16	100	95	85	mA
Precharge Standby current in Non-Power down mode	Icc2N	CKE=VILmax tCLK=15ns	x4/x8/x16	20	20	20	mA
	Icc2NS	CKE=VIHmin CLK=VILmax(fixed)	x4/x8/x16	15	15	15	mA
Precharge Standby current in Power down mode	Icc2P	CKE=VIHmin tCLK=15ns(Note)	x4/x8/x16	2	2	2	mA
	Icc2PS	CKE=VIHmin tCLK=VILmax(fixed)	x4/x8/x16	1	1	1	mA
Active Standby current	Icc3N	CKE=/CS=VIHmin tCLK=15ns(Note)	x4/x8/x16	30	30	30	mA
	Icc3NS	CKE=VIHmin tCLK=VILmax(fixed)	x4/x8/x16	25	25	25	
Burst current	Icc4	All Bank Active tCLK = min BL=4, CL=3, IOL=0mA	x4/x8/x16	140	130	120	mA
Auto-refresh current	Icc5	tRC=min, tCLK=min	x4/x8/x16	130	130	130	mA
Self-refresh current	Icc6	CKE < 0.2V x4/x8/x16	7,7.5,8	1	1	1	mA

NOTE:

1. Icc(max) is specified at the output open condition.
2. Input signals are changed one time during 30ns.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 - 70˚C, Vdd=VddQ=3.3±0.3V,Vss=VssQ=0V, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits		unit
			Min.	Max.	
VOH (DC)	High-Level Output Voltage (DC)	IOH=-2mA	2.4		V
VOL (DC)	Low-level Output Voltage (DC)	IOL= 2mA		0.4	V
IOZ	Off-state Output Current	Q floating VO=0 -- VddQ	-5	5	µA
I_I	Input Current	VIH = 0 -- VddQ +0.3V	-5	5	µA

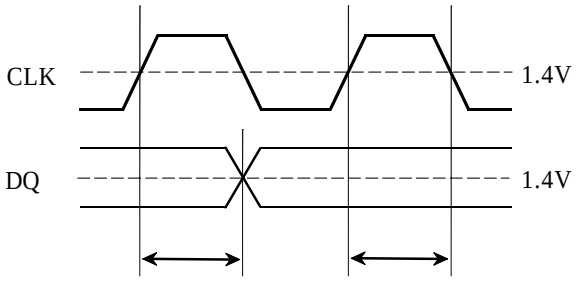
AC TIMING REQUIREMENTS

(Ta=0 - 70˚C, Vdd=VddQ=3.3±0.3V,Vss=VssQ=0V, unless otherwise noted)

Input Pulse Levels:0.8V-2.0V

Input Timing Measurement Level:1.4V

Symbol	Parameter		Limits						Unit
			-7		-75		-8		
			Min.	Max.	Min.	Max.	Min.	Max.	
tCLK	CLK cycle time	CL=2	-		10		10		ns
		CL=3	7		7.5		8		ns
tCH	CLK High pulse width		2.5		2.5		3		ns
tCL	CLK Low pulse width		2.5		2.5		3		ns
tT	Transition time of CLK		1	10	1	10	1	10	ns
tIS	Input Setup time (all inputs)		1.5		1.3		2		ns
tIH	Input Hold time (all inputs)		0.8		0.8		0.8		ns
tRC	Row Cycle time		63		67.5		0 7		ns
tRFC	Refresh Cycle Time		70		75		80		ns
tRCD	Row to Column Delay		20		20		20		ns
tRAS	Row Active time		45	100K	45	100K	48	100K	ns
tRP	Row Precharge time		20		20		20		ns
tWR	Write Recovery time		14		15		20		ns
tRRD	Act to Act Delay time		14		15		20		ns
tRSC	Mode Register Set Cycle time		14		15		20		ns
tREF	Refresh Interval time			64		64		64	ms



Any AC timing is referenced to the input signal passing through 1.4V.

SWITCHING CHARACTERISTICS

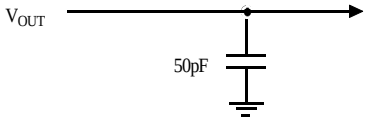
(Ta=0 - 70˚C, Vdd=VddQ=3.3±0.3V,Vss=VssQ=0V, unless otherwise noted)

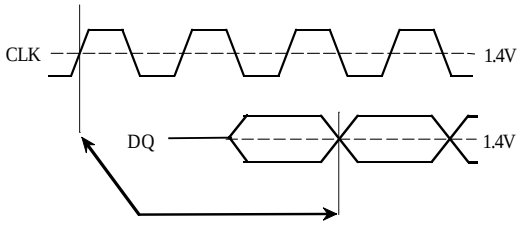
Symbol	Parameter		Limits						Unit	Note
			-7		-7.5		-8			
			Min.	Max.	Min.	Max.	Min.	Max.		
tAC	Access time from CLK	CL=2				6		6	ns	*1
		CL=3		5.4		5.4		6	ns	
tOH	Output Hold time from CLK	CL=2			3		3		ns	
		CL=3	2.7		3		3		ns	
tOLZ	Delay time , output low-impedance from CLK		0		0		0		ns	
tOHZ	Delay time , output high-impedance from CLK		2.7	5.4	3	5.4	3	6	ns	

NOTE:

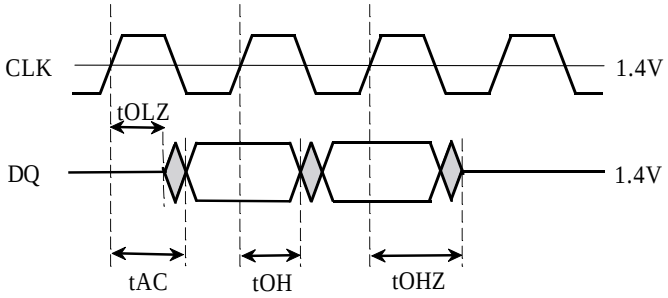
1. If clock rising time is longer than 1ns,(tr/2-0.5ns) should be added to the parameter.

Output Load Condition

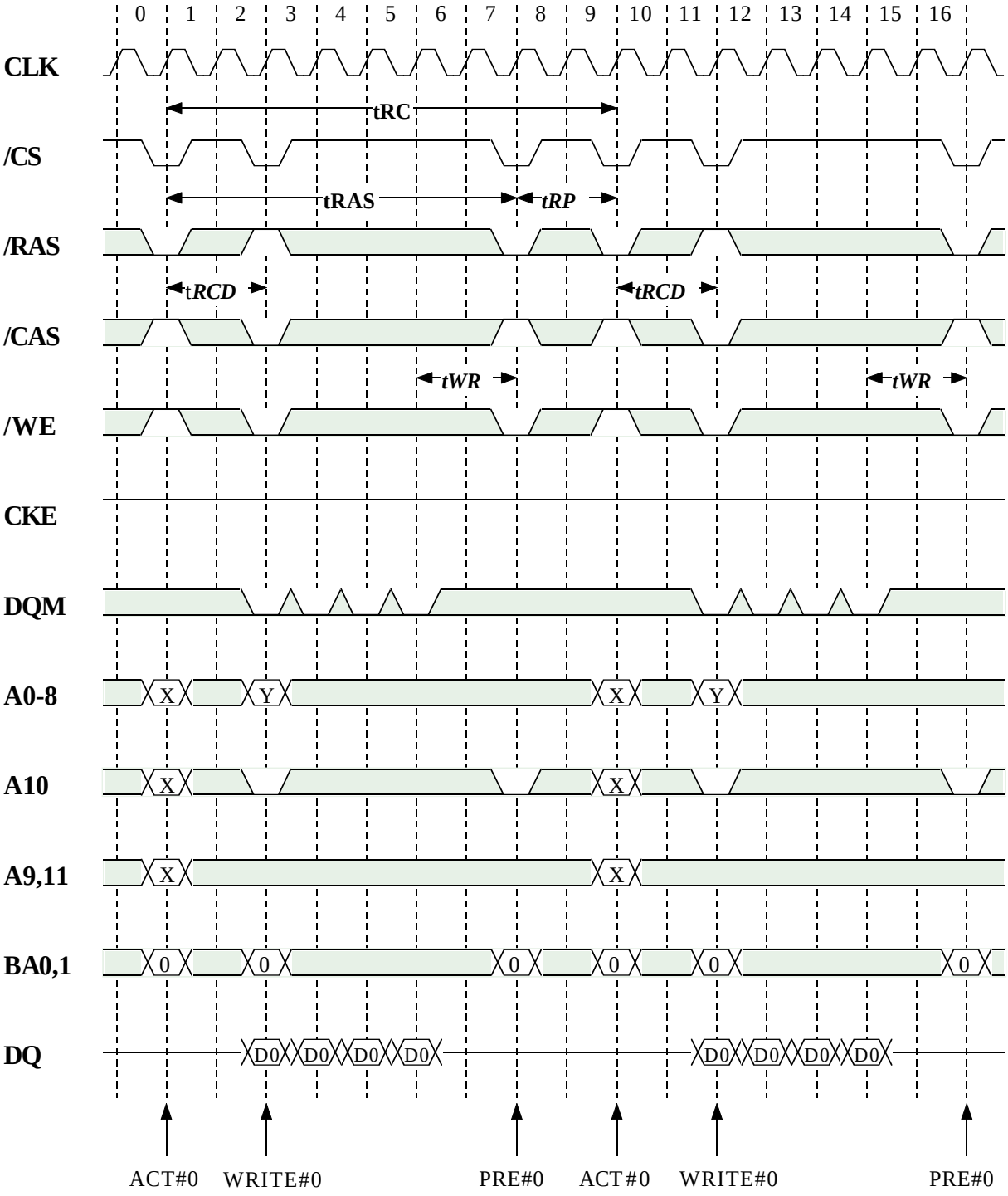




Output Timing Measurement Reference Point

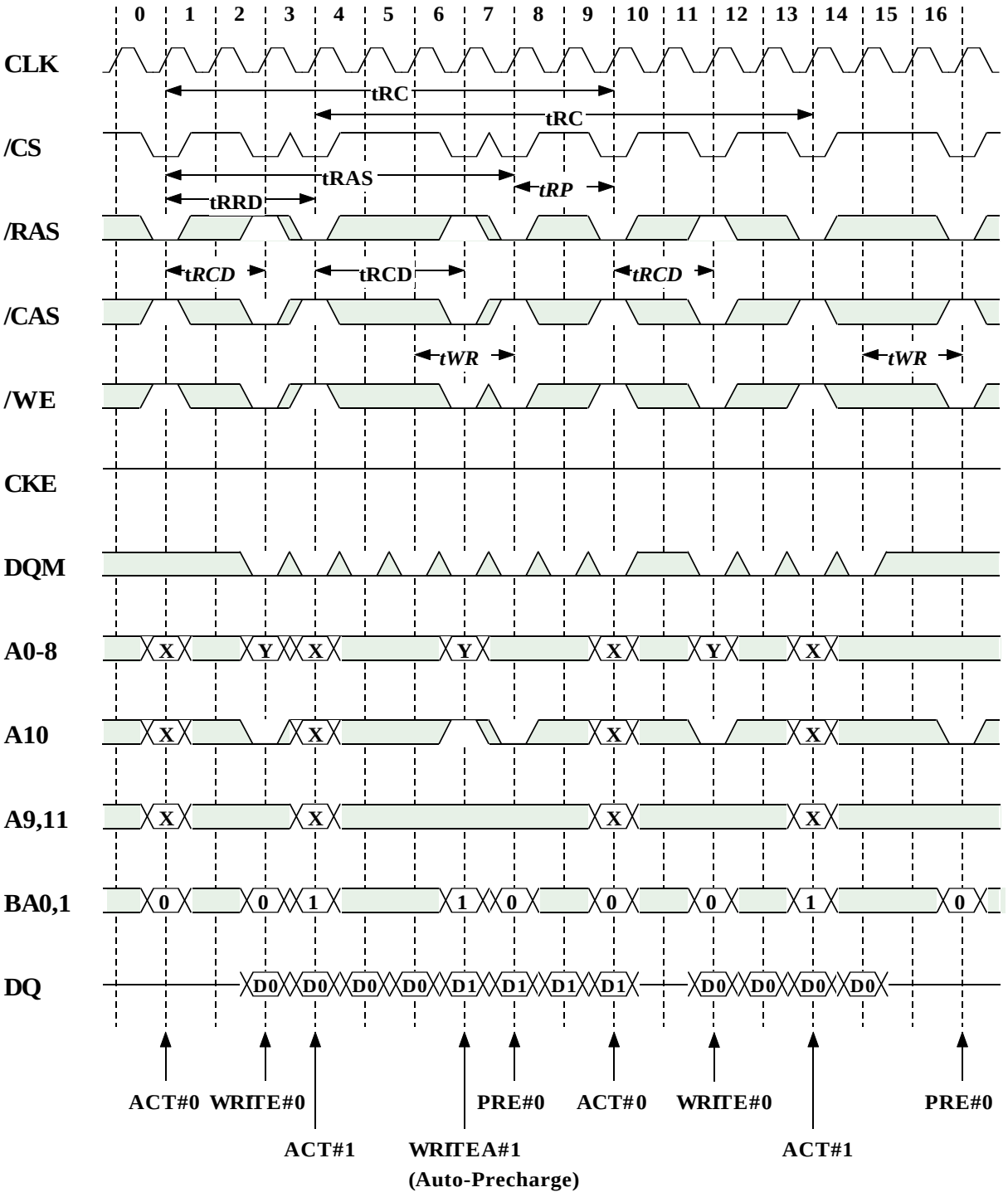


Burst Write (single bank) @BL=4



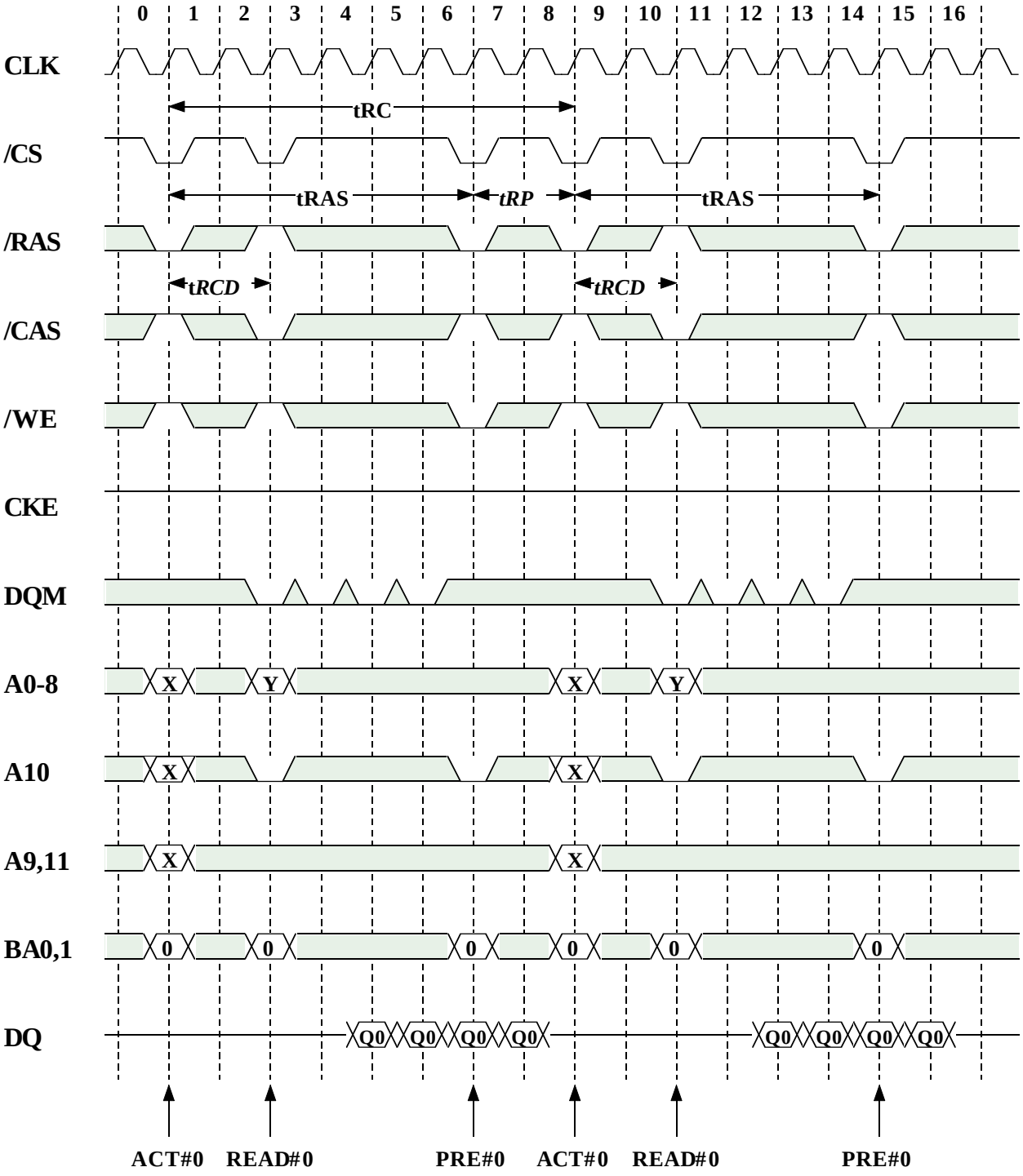
Italic parameter indicates minimum case

Burst Write (multi bank) @BL=4



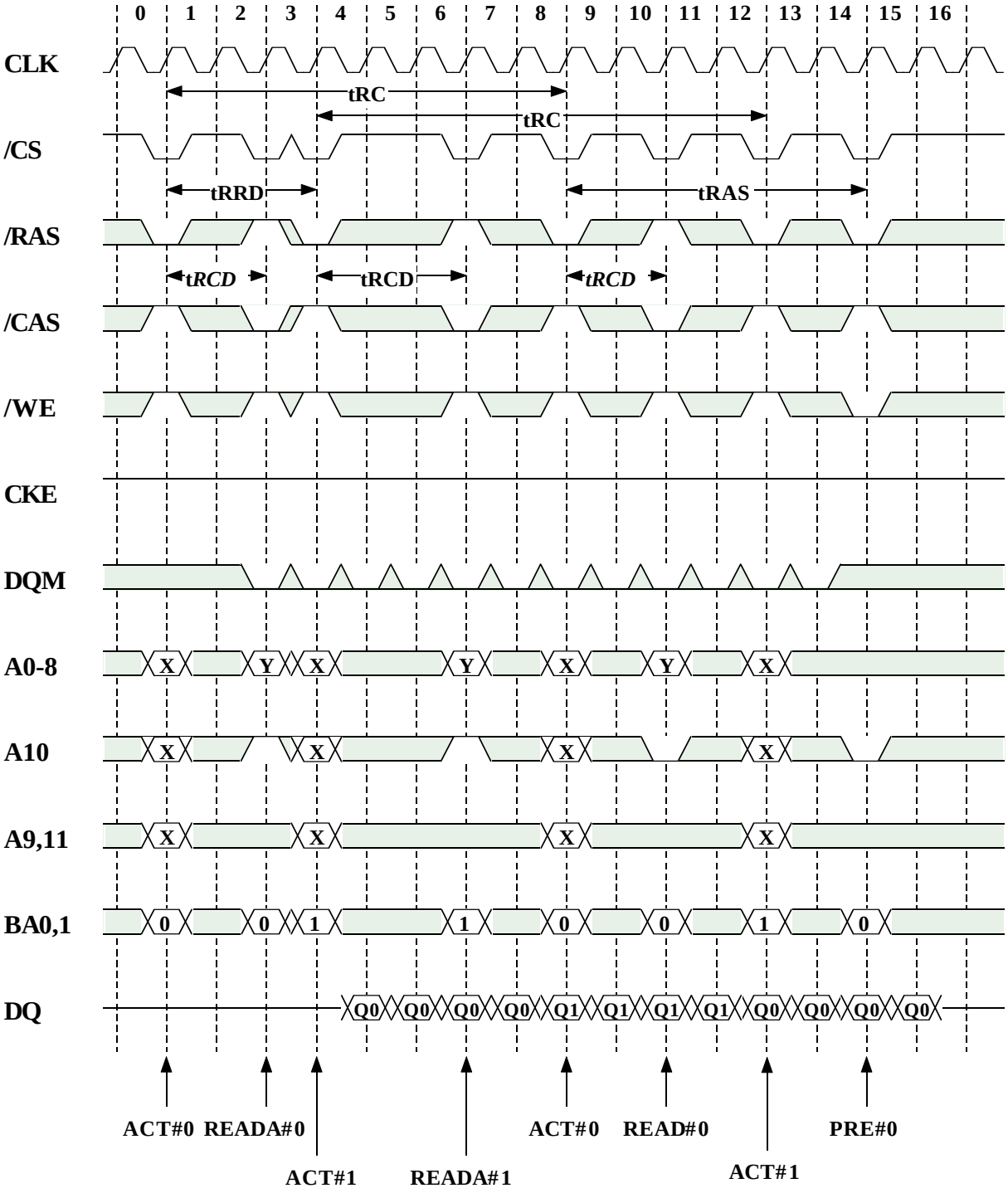
Italic parameter indicates minimum case

Burst Read (single bank) @BL=4 CL=2



Italic parameter indicates minimum case

Burst Read (multiple bank) @BL=4 CL=2



Italic parameter indicates minimum case

Write Interrupted by Write @BL=4

Italic parameter indicates minimum case

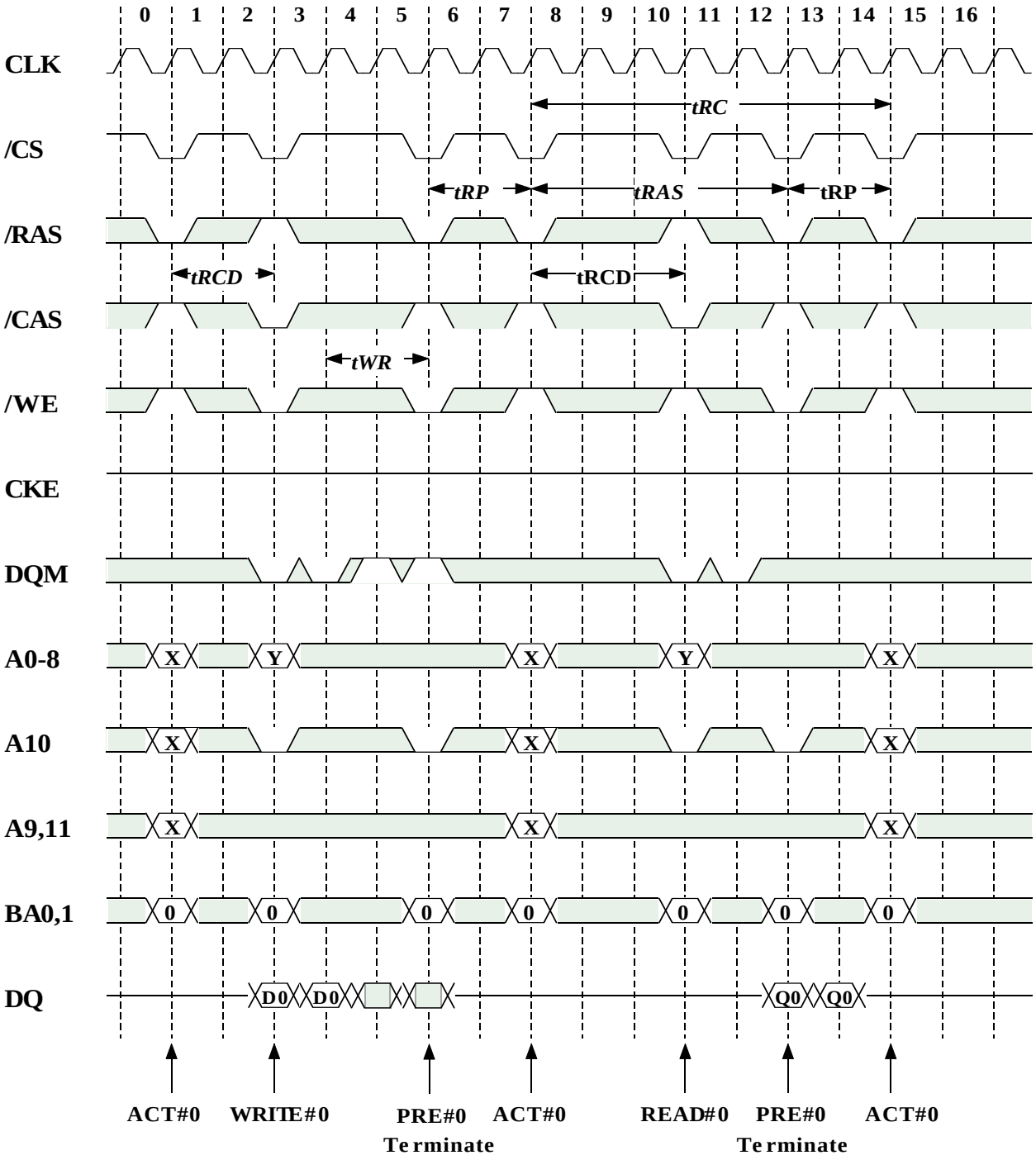
Read Interrupted by Read @BL=4,CL=2

Italic parameter indicates minimum case

Write Interrupted by Read, Read Interrupted by Write @BL=4,CL=2

Italic parameter indicates minimum case

Write/Read Terminated by Precharge @BL=4,CL=2

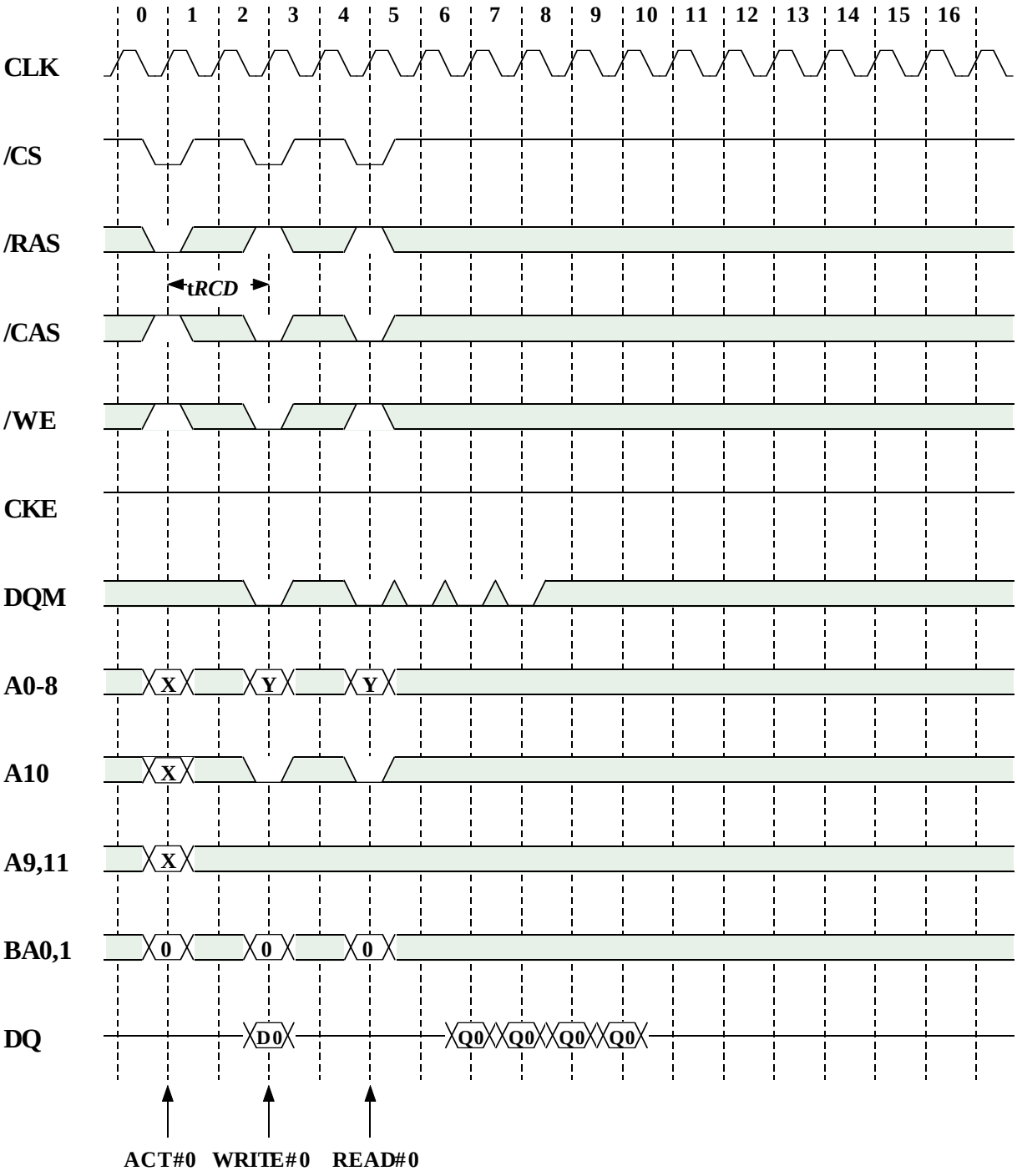


Italic parameter indicates minimum case

Write/Read Terminated by Burst Terminate @BL=4,CL=2

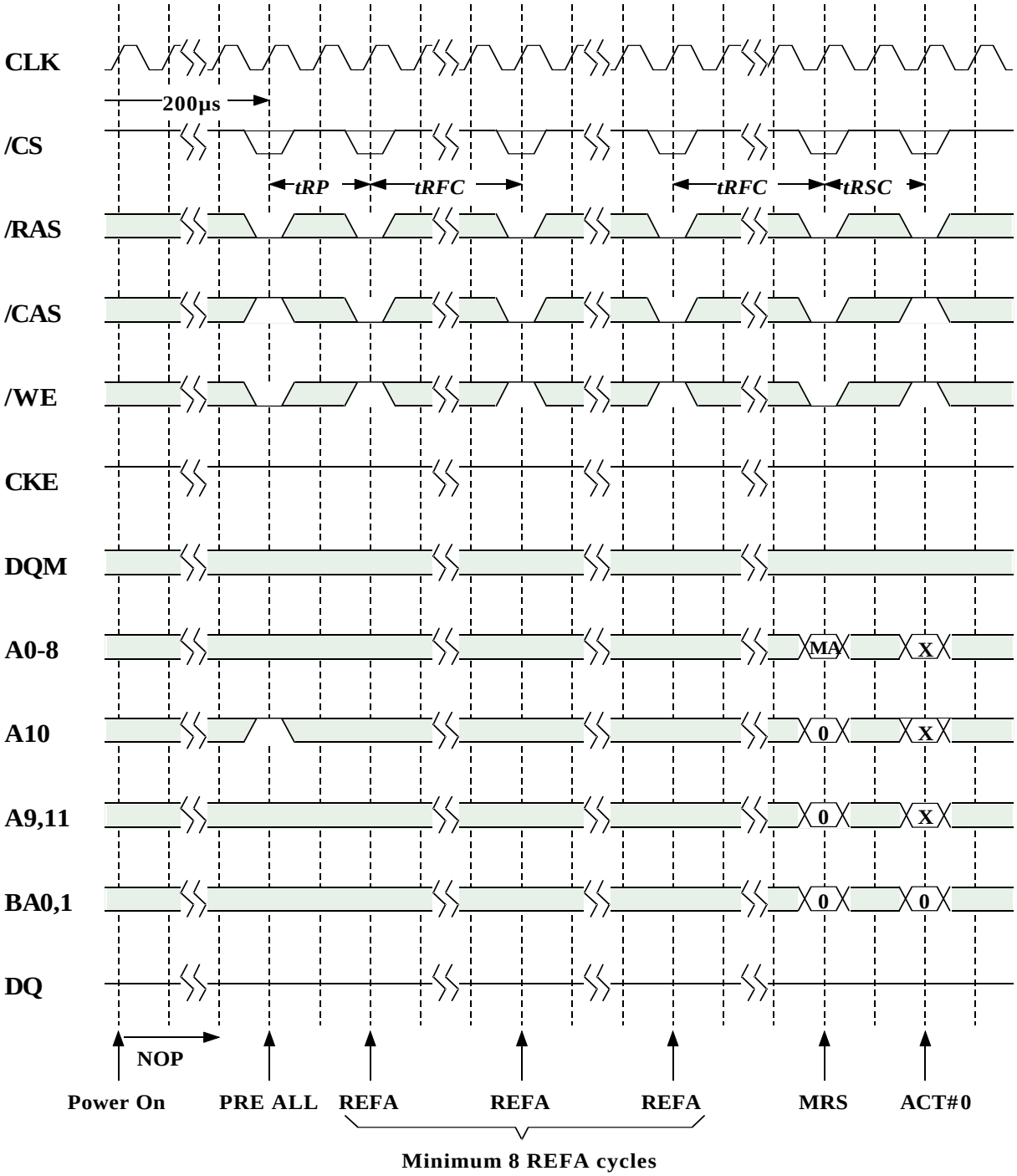
Italic parameter indicates minimum case

Single Write Burst Read @BL=4,CL=2



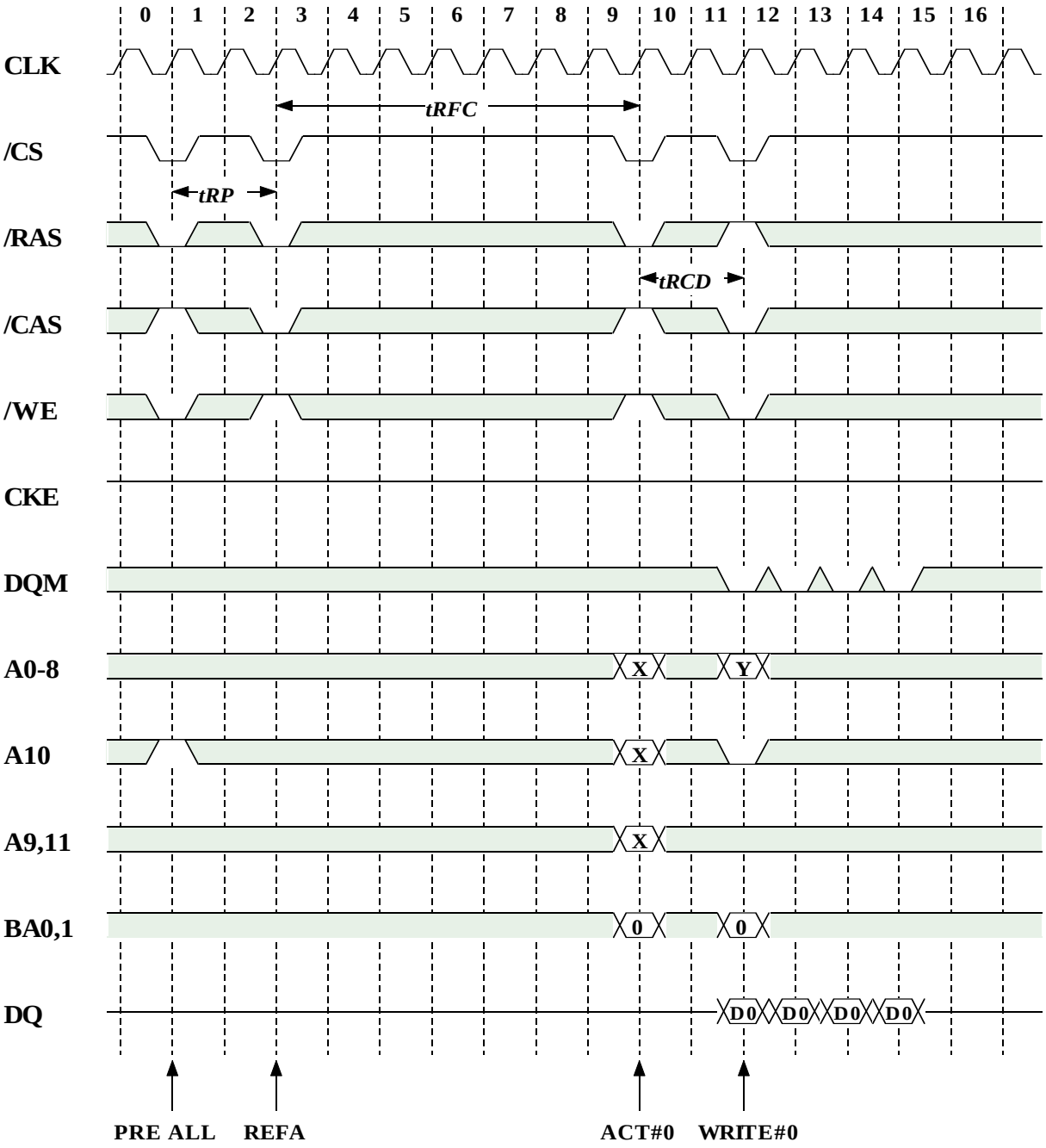
Italic parameter indicates minimum case

Power-Up Sequesce and Intialize



Italic parameter indicates minimum case

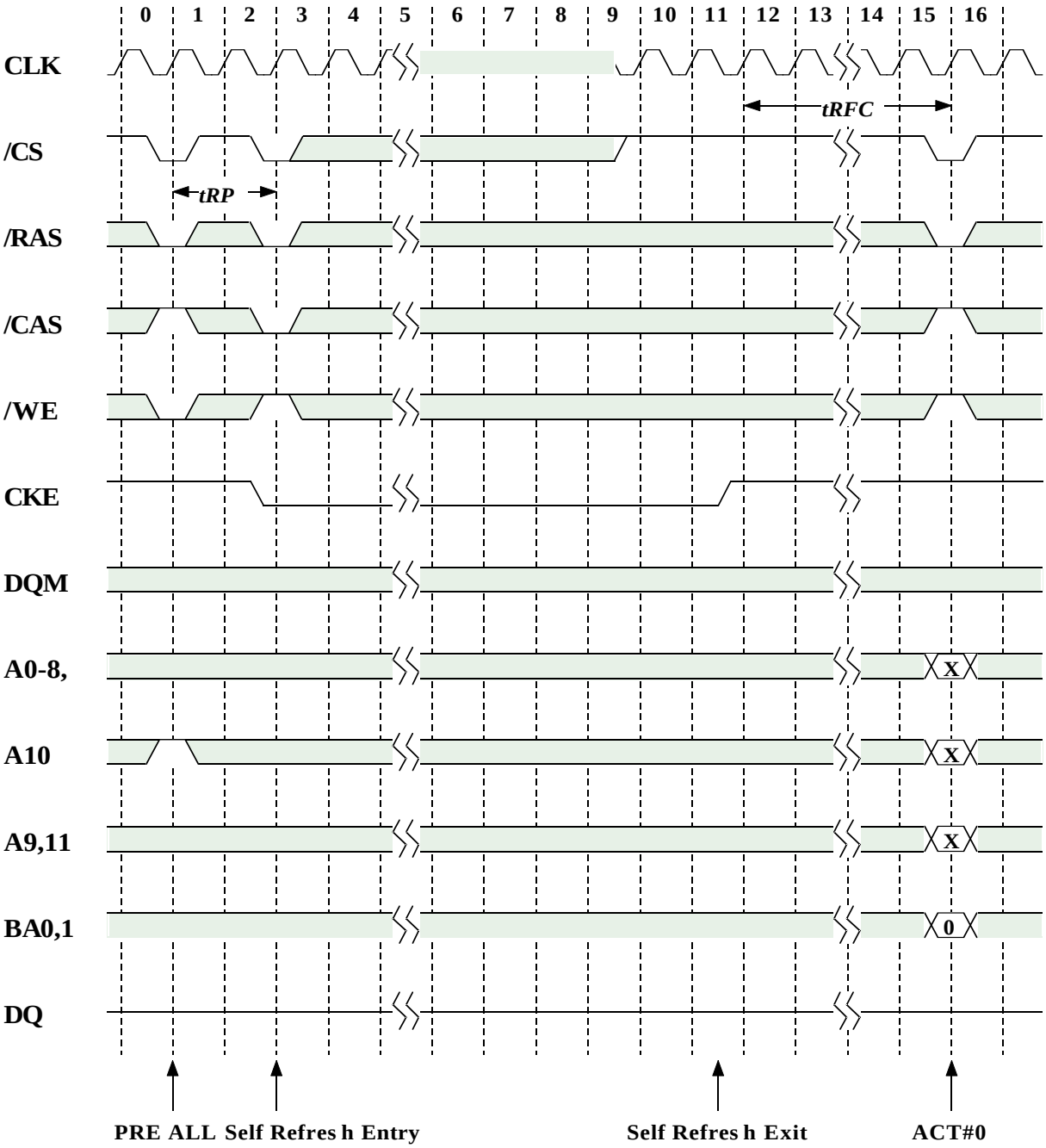
Auto Refresh



All banks must be idle before REFA is issued.

Italic parameter indicates minimum case

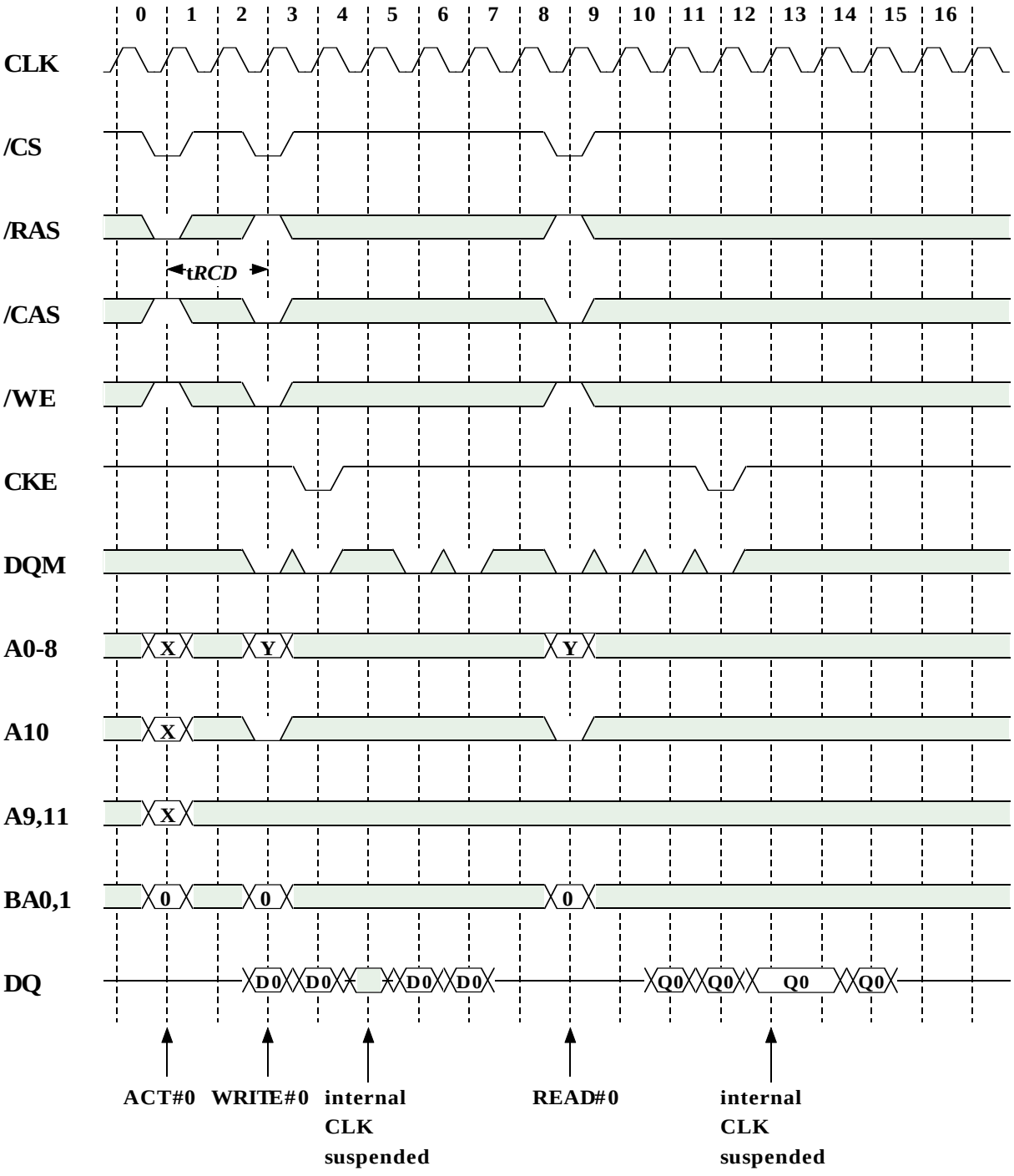
Self Refresh



All banks must be idle before REFS is issued.

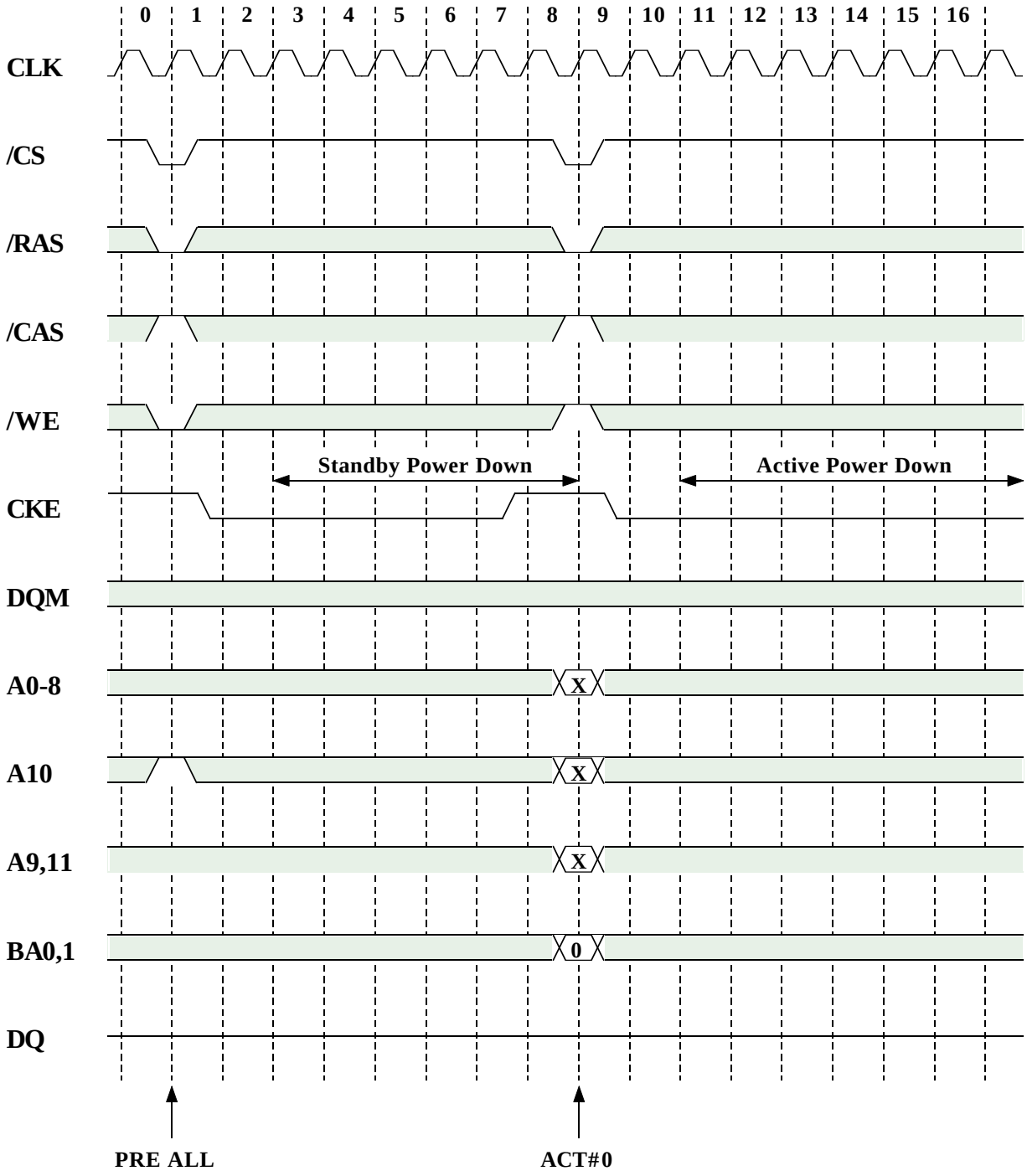
Italic parameter indicates minimum case

CLK Suspension @BL=4,CL=2



Italic parameter indicates minimum case

Power Down


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
CLK
/CS
/RAS
/CAS
/WE
Standby Power Down
Active Power Down
CKE
DQM
A0-8
X
A10
X
A9,11
X
BA0,1
0
DQ
PRE ALL
ACT#0

DQM Write Mask @BL=4