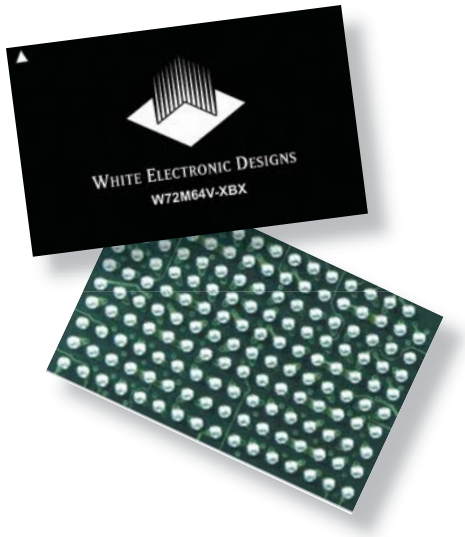
2M x 64 Flash Multi-Chip Package

Optimum Density and Performance in One Package



W72M64V-XBX Features

Designed to complement PowerPC™ high performance memory controllers (see page 2 for typical application block diagram)

Performance Features

- Simultaneous Read/Write operations
  - Data can be continuously read from one bank while executing erase/program functions in other bank
  - Zero latency between read and write operations
- Zero Power Operation
- 16MByte (128Mb) organized as 2Mx64
- Access Times of 100, 120, 150ns
- 1,000,000 Erase/Program Cycles per sector
- Sector Architecture
  - Bank 1: Eight 4KWord, fifteen 32KWord
    Bank 2: Forty-Eight 32K Word
  - Any combination of sectors can be concurrently erased. Also supports full chip erase.
- Boot Code Sector Architecture (Bottom)
- 3.3V for Read and Write Operations
- Commercial, industrial and military temperature ranges

Package

- 13x22mm, 159 Plastic Ball Grid Array (PBGA), 286mm^2

Benefits

- 70% space savings
- Reduced part count
- 17% I/O reduction
- Suitable for high-reliability applications
- Upgradeable to 8Mx64 (contact factory for future availability)

For more information, visit our website at **www.wedc.com** or call (602) 437-1520 and ask for applications support.

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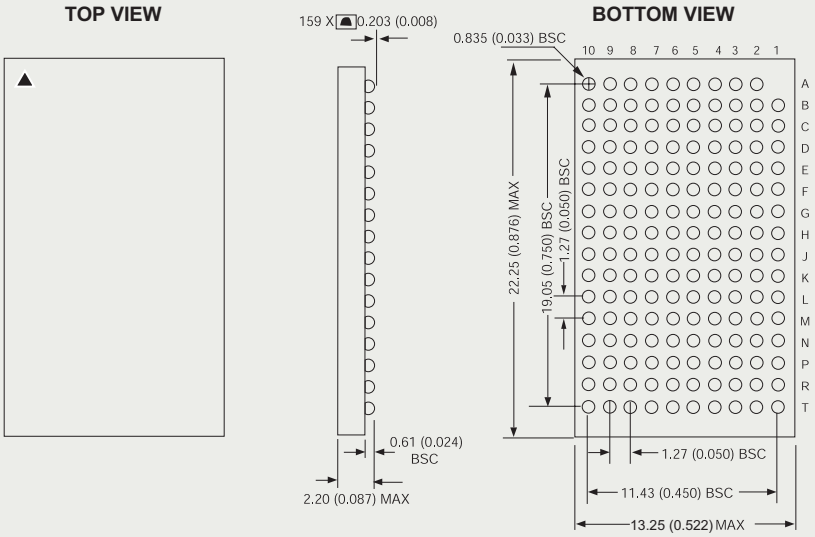
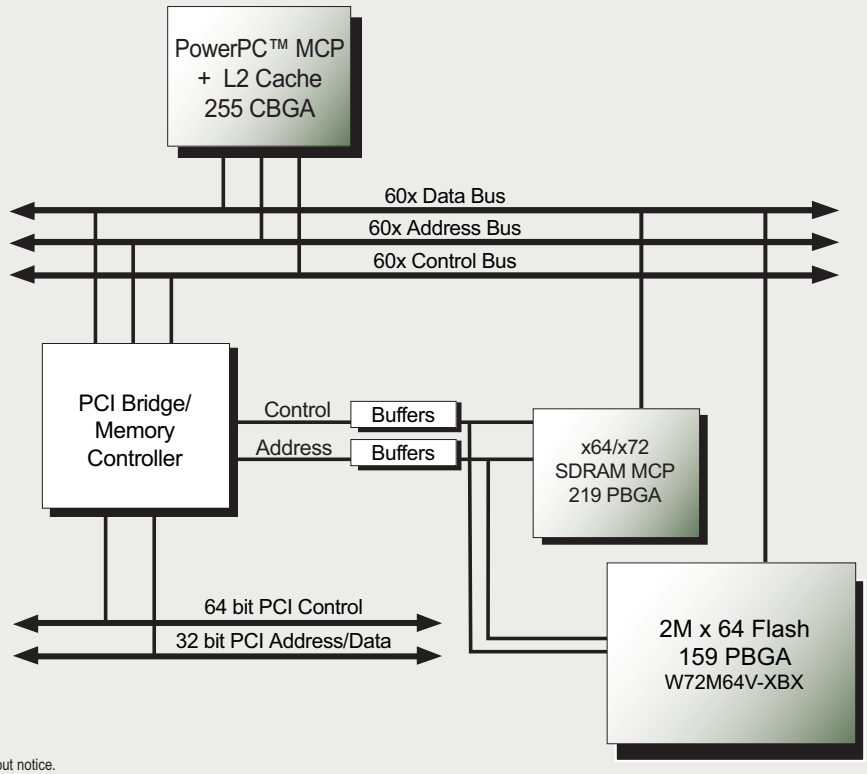
Package Dimensions



NOTE: Dimensions in millimeters (inches)

System Block Diagram



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For ordering or information on any of our products and services, call White Electronic Designs at:

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