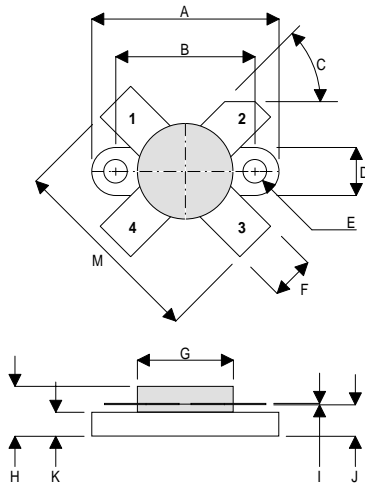


MECHANICAL DATA



DM

PIN 1 SOURCE PIN 2 DRAIN
 PIN 3 SOURCE PIN 4 GATE

DIM	mm	Tol.	Inches	Tol.
A	24.76	0.13	0.975	0.005
B	18.42	0.13	0.725	0.005
C	45°	5°	45°	5°
D	6.35	0.13	0.25	0.005
E	3.17 Dia.	0.13	0.125 Dia.	0.005
F	5.71	0.13	0.225	0.005
G	12.7 Dia.	0.13	0.500 Dia.	0.005
H	6.60	REF	0.260	REF
I	0.13	0.02	0.005	0.001
J	4.32	0.13	0.170	0.005
K	3.17	0.13	0.125	0.005
M	26.16	0.25	1.03	0.010

**GOLD METALLISED
 MULTI-PURPOSE SILICON
 DMOS RF FET
 60W – 28V – 175MHz
 SINGLE ENDED**

FEATURES

- SIMPLIFIED AMPLIFIER DESIGN
- SUITABLE FOR BROAD BAND APPLICATIONS
- LOW C_{rss}
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN – 16 dB MINIMUM

APPLICATIONS

- HF/VHF COMMUNICATIONS
 from 1 MHz to 175 MHz

ABSOLUTE MAXIMUM RATINGS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

P_D	Power Dissipation	117W
BV_{DSS}	Drain – Source Breakdown Voltage	70V
BV_{GSS}	Gate – Source Breakdown Voltage	$\pm 20V$
$I_{D(sat)}$	Drain Current	15A
T_{stg}	Storage Temperature	-65 to $150^{\circ}C$
T_j	Maximum Operating Junction Temperature	$200^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise stated)

Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS} Drain-Source Breakdown Voltage	$V_{GS} = 0$ $I_D = 100mA$	70			V
I_{DSS} Zero Gate Voltage Drain Current	$V_{DS} = 28V$ $V_{GS} = 0$			1	mA
I_{GSS} Gate Leakage Current	$V_{GS} = 20V$ $V_{DS} = 0$			1	μA
$V_{GS(th)}$ Gate Threshold Voltage *	$I_D = 10mA$ $V_{DS} = V_{GS}$	1		7	V
g_{fs} Forward Transconductance *	$V_{DS} = 10V$ $I_D = 3A$	2.4			S
G_{PS} Common Source Power Gain	$P_O = 60W$	16			dB
η Drain Efficiency	$V_{DS} = 28V$ $I_{DQ} = 0.3A$	50			%
VSWR Load Mismatch Tolerance	$f = 175MHz$	20:1			—
C_{iss} Input Capacitance	$V_{DS} = 0$ $V_{GS} = -5V$ $f = 1MHz$			180	pF
C_{oss} Output Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$ $f = 1MHz$			90	pF
C_{rss} Reverse Transfer Capacitance	$V_{DS} = 28V$ $V_{GS} = 0$ $f = 1MHz$			7.5	pF

* Pulse Test: Pulse Duration = 300 μs , Duty Cycle $\leq 2\%$

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area.

THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

THERMAL DATA

$R_{THj-case}$	Thermal Resistance Junction – Case	Max. 1.5°C / W
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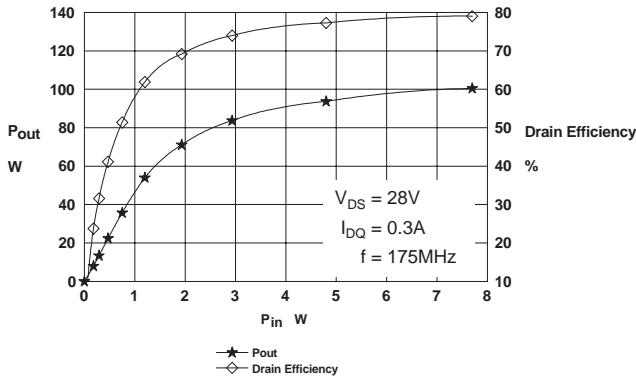


Figure 1 – Power Output and Efficiency vs. Power Input.

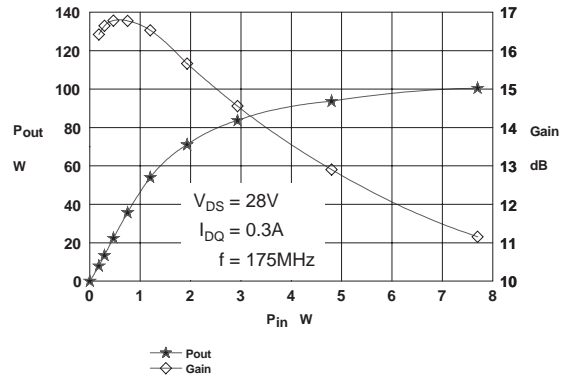


Figure 2 – Power Output & Gain vs. Power Input.

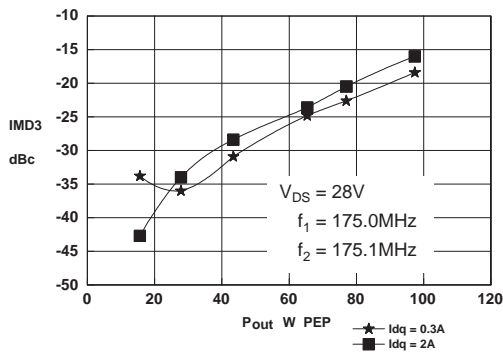


Figure 3 – IMD vs. Output Power.

D1003UK OPTIMUM SOURCE AND LOAD IMPEDANCE

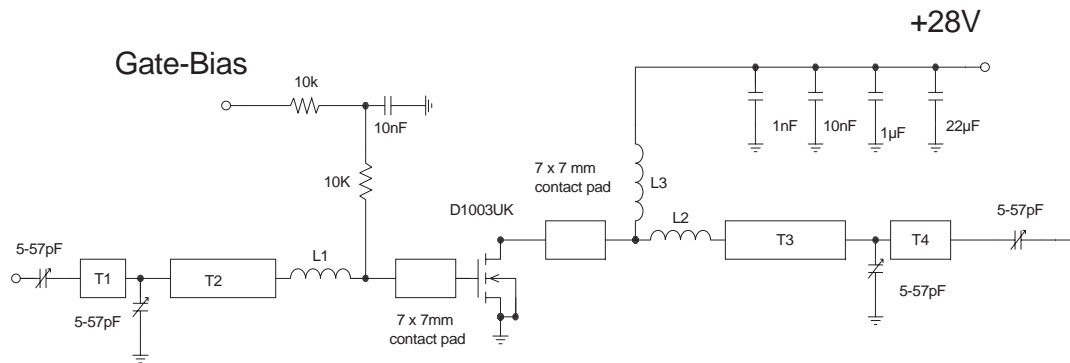
Frequency MHz	Z _S Ω	Z _L Ω
175MHz	2.0 – j4.3	3.7 – j4.5

Typical S Parameters

! V_{DS} = 28V, I_{DQ} = 0.3A

MHz S M A R 50

!Freq MHz	S11		S21		S12		S22	
	mag	ang	mag	ang	mag	ang	mag	ang
70	0.83	-156.8	6.9	59.9	0.018	-16.7	0.65	-137.0
100	0.87	-163.3	4.3	46.9	0.012	-15.5	0.75	-147.2
150	0.91	-171.0	2.3	31.5	0.007	37.1	0.84	-159.7
200	0.93	-177.6	1.4	22.6	0.013	81.0	0.90	-168.8
250	0.95	177.6	0.9	14.3	0.022	86.6	0.93	-175.0
300	0.97	173.6	0.7	10.5	0.032	86.9	0.95	179.5
350	0.96	168.6	0.5	4.0	0.039	80.0	0.96	175.3
400	0.98	165.0	0.4	3.9	0.048	80.0	0.98	172.0
450	0.98	161.9	0.3	2.9	0.053	77.5	0.98	169.8
500	0.97	159.3	0.3	2.1	0.064	74.8	0.97	166.5



D1003UK 175MHz TEST FIXTURE

Substrate 1.6mm PTFE/ glass, $\epsilon_r = 2.5$
 All microstrip lines $W = 4.4\text{mm}$

T1 8mm
 T2 22mm
 T3 18mm
 T4 4.5mm

L1 Hairpin loop 16swg 15.5mm dia.
 L2 Hairpin loop 16swg 10mm dia.
 L3 11 turns 18swg enamelled copper wire, 10mm i. d.