



## ESCC (e) 4001/023 Qualified High Precision (5 ppm, 0.01 %), Thin Film Chip Resistors



Vishay Sfernice Thin Film division holds ESCC QML qualification (ESCC technology flow qualification).

These High-Rel. components are ideal for low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, Vishay Sfernice's precision thin film wraparound resistors exceed requirements of MIL-PRF-55342G characteristics Y ( $\pm 10$  ppm/°C).

### FEATURES

HALOGEN  
FREE

- Load life stability at  $\pm 70$  °C for 2000 h: 0.15 % under Pn
- Low temperature coefficient down to  $\pm 5$  ppm/°C
- Very low noise ( $< -35$  dB) and voltage coefficient ( $< 0.01$  ppm/V)
- Resistance range: 10  $\Omega$  to 3 M $\Omega$  (depending on size)
- Laser trimmed tolerances to  $\pm 0.01$  %
- TCR in lot tracking  $\leq 5$  ppm/°C
- Termination: Thin film technology
- SnPb terminations over nickel barrier
- ESCC 4001 (generic specifications)
- ESCC 4001/023 (detailed specifications)
- ESCC qualified
- SMD wraparound chip resistor
- Operating temperature range: - 65 °C to + 155 °C
- From 0402 to 2010
- Material categorization: For definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)

### STANDARD ELECTRICAL SPECIFICATIONS

MODEL	SIZE	ESCC VARIANT NUMBER	RESISTANCE RANGE $\Omega$	RATED POWER AT + 70 °C (Pn) W <sup>(1)</sup>	LIMITING ELEMENT VOLTAGE (UL) V <sup>(1)</sup>	INSULATION VOLTAGE (U <sub>i</sub> ) V	TOLERANCE $\pm$ %	TEMPERATURE COEFFICIENT $\pm$ ppm/°C
PHR 0402 <sup>(2)</sup>	0402	13 and 14	10 to 150K	0.05	30	50	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 0603 (e)	0603	01 and 05	10 to 500K	0.1	35	100	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 0805 (e)	0805	02 and 06	10 to 750K	0.125	75	200	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 1206 (e)	1206	03 and 07	10 to 3.5M	0.25	100	300	0.01, 0.02, 0.05, 0.1	5, 10, 25
PHR 2010 (e)	2010	04 and 08	10 to 6M	0.50	150	300	0.01, 0.02, 0.05, 0.1	5, 10, 25

#### Notes

- <sup>(1)</sup> PHR 0402: Qualification ongoing.  
<sup>(2)</sup> Limiting voltages and power rating are already derated (for maximum ratings admissible, refer to P chip: [www.vishay.com/cod?253017](http://www.vishay.com/cod?253017)).

### CLIMATIC SPECIFICATIONS

Operating temperature range	- 65 °C; + 155 °C
Soldering temperature (T <sub>sol</sub> )	260 °C, immersion 10 s

### MECHANICAL SPECIFICATIONS

Substrate material	Alumina
Technology	Thin Film
Film	<b>Nickel Chromium</b> with mineral passivation
Protection	Epoxy and silicone
Terminations	<b>B type:</b> SnPb over nickel barrier for solder reflow <sup>(3)</sup> <b>G type:</b> Gold

#### Note

- <sup>(3)</sup> For B terminations use recommended reflow profile #1 as per Application Note "Guidelines for Vishay Sfernice Resistive and Inductive Components" (document number: 52029)

**DIMENSIONS** in millimeters

VARIANT NUMBER	STYLE	DIMENSIONS							
		A		B		C		D/E	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
01, 05	0603	1.368	1.672	0.723	0.977	0.373	0.627	0.25	0.51
02, 06	0805	1.758	2.062	1.143	1.397	0.373	0.627	0.25	0.51
03, 07	1206	2.908	3.212	1.473	1.727	0.373	0.627	0.27	0.53
04, 08	2010	4.898	5.232	2.413	2.667	0.373	0.627	0.35	0.61
13, 14	0402	0.848	1.152	0.473	0.727	0.373	0.627	0.15	0.35

**NOTION OF SINGLE LOT**

The homogeneity of lots is given by the front end lot numbers (primary process lot) and not by the date code. The date code is applied after completion of end of production testing. Parts coming from different lots might have same date code. A customer who needs lot homogeneity should mention on his order: SINGLE PRODUCTION LOT

**END OF PRODUCTION TESTING**

Mandatory testing performed at the end of the production process:

- 100 % overload: Voltage  $\sqrt{(6.25 P_n \times R_n)}$  or 2 UL whichever is less - duration 2 s
- 100 % burn in: 168 h at  $P_n$  at 70 °C

**OPTIONS****LOT VALIDATION TESTING**

For procurement of qualified components, lot validation testing is not required and shall only be performed if specifically stipulated in the purchase order.

For procurement of unqualified components, lot validation testing shall be performed as stipulated in the purchase order. The need for lot validation testing shall be determined by the orderer.

When lot validation testing is required, it shall consist of the performance of one or more of the tests or subgroup test sequences of chart F4 indicated in the ESA Generic Specification ESCC 4001. The testing to be performed and the sample size shall be as stipulated in the purchase order. When procurement of more than one component type is involved from a family, range or series, the selection of representative samples shall also be stipulated in the purchase order.

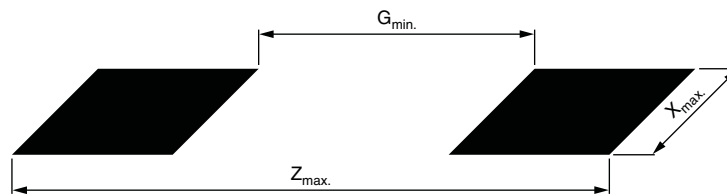
Lot validation testing will be composed of one LVT charges and LVT samples:

- Lot validation test charges has to be ordered separately on purchase order.
- Lot validation samples have to be ordered separately on purchase order.

**FINAL INSPECTION**

If requested by the orderer a final inspection can be performed on site.

Final inspection has to be stipulated separately on purchase order.

**LAND PATTERN** in millimeters

CHIP SIZE	Z <sub>max.</sub>	G <sub>min.</sub>	X <sub>max.</sub>
0402	1.55	0.15	0.73
0603	2.37	0.35	0.98
0705/0805	2.76	0.74	1.40
1206	3.91	1.85	1.73
2010	5.93	3.71	2.67

**Note**

- Suggested land pattern: According to IPC-7351A



QUALIFIED OHMIC RANGE (1)			
MODEL	ESCC VARIANT	OHMIC RANGE (Ω)	TOLERANCE (%)
PHR	01 to 08 and 13 to 14 (2)	10 to < 50	0.1
		50 to < 100	0.05 and 0.1
		100 to < 250	0.02, 0.05 and 0.1
		≥ 250	0.01, 0.02, 0.05 and 0.1

QUALIFIED OHMIC RANGE (1)				
MODEL	ESCC VARIANT	OHMIC RANGE (Ω)	TEMPERATURE COEFFICIENT (ppm/°C)	ESCC CODE
PHR	01 to 08 and 13 to 14 (2)	10 to < 20	E: 25 (- 55 °C; + 155 °C)	2
		20 to < 50	Y: 10 (- 55 °C; + 155 °C)	1
		20 to < 50	Z: 5 (+ 22 °C; + 70 °C)	0
		≥ 50	C: 5 (- 55 °C; + 155 °C)	9

QUALIFIED OHMIC RANGE: MAX. VALUE (1)				
PHR 0402 (2)	PHR 0603	PHR 0805	PHR 1206	PHR 2010
100 kΩ (67 kΩ for TCR C)	200 kΩ (160 kΩ for TCR C)	250 kΩ	1 MΩ	3 MΩ

**Notes**

- (1) For values, TCR, tolerance outside of qualified range: Please consult.
- (2) PHR 0402: Qualification ongoing.

**POPULAR OPTIONS**

**OPTION 0041**

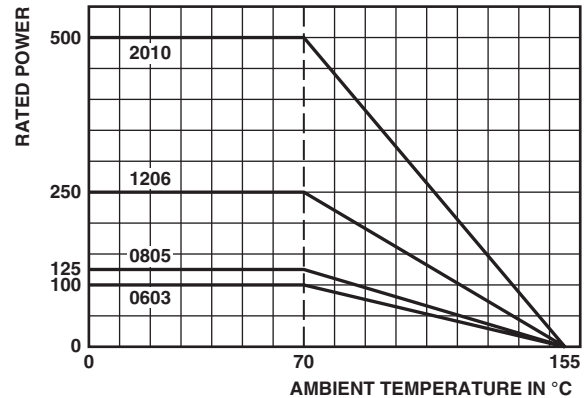
Production according to ESCC 4001/023 for: Cases, ohmic values, tolerance or TCR outside of qualified range. Please consult Vishay Sfernice for feasibility.

PACKAGING				
Two types of packaging are available: Waffle-pack and tape and reel.				
SIZE	NUMBER OF PIECES PER PACKAGE		TAPE WIDTH	
	WAFFLE PACK 2" x 2"	TAPE AND REEL (3)		
		MIN.	MAX.	
0402	100	50	5000	8 mm
0603			4000	
0805			2000	
1206				
2010				

**Note**

- (3) MoQ: 50 pieces

**POWER DERATING CURVE**



**EXTENDED FEATURES**

You may consult Vishay Sfernice for chip sizes, ohmic values and tolerances outside of the qualified range.



PERFORMANCE				
TEST	CONDITIONS	REQUIREMENTS		TYPICAL
		ESA/SCC 4001/023	MIL-PRF-55342G	
Short time overload	$U = \sqrt{(6.25 P_n \times R_n)}$ $U_{max.} < 2 UL - 2 s$	$\pm 0.05 \% + (0.05 \Omega \times 100/R_n)$	0.10 %	$\pm 0.01 \%$
Rapid temperature change	- 55 °C/+ 155 °C 5 cycles CEI 66-2-14 Test Na	$\pm 0.05 \% + (0.05 \Omega \times 100/R_n)$	0.1 % (for 100 cycles)	$\pm 0.01 \%$ $\pm 0.015 \%$ (for 500 cycles)
Soldering (thermal shock)	260 °C/10 s CEI 68-2-20 A Test T6 (met. 1A)	$\pm 0.05 \% + (0.05 \Omega \times 100/R_n)$	-	$\pm 0.005 \%$
Terminal strength: adhesion bend strength of end plated facing	CEI 115-1 Clause 4.32 CEI 115-1 Clause 4.33	$\pm 0.05 \% + (0.05 \Omega \times 100/R_n)$	-	$\pm 0.01 \%$
Climatic sequence	CEI 67-2-1/CEI 68-2-2 CEI 67-2-13/CEI 68-2-30	$\pm 0.10 \% + (0.05 \Omega \times 100/R_n)$	-	$\pm 0.02 \%$ Insulation resistance > 1 GΩ
Load life	2000 h Pn at + 70 °C 90'/30' cycle	$\pm 0.15 \% + (0.05 \Omega \times 100/R_n)$	0.5 %	$\pm 0.02 \%$ Insulation resistance > 1 GΩ
High temperature exposure	2000 h Pn at + 155 °C CEI 68-2-20A Test B	$\pm 0.15 \% + (0.05 \Omega \times 100/R_n)$	$\pm 0.10 \%$ (duration 1000 h)	$\pm 0.05 \%$ Insulation resistance > 1 GΩ

ESCC/PHR CODIFICATION CORRESPONDANCE TABLES			
VARIANT	MODEL	CASE SIZE	TERMINATION
13	PHR	0402	B (tin/lead)
01		0603	
02		0805	
03		1206	
04		2010	
14		0402	G (gold)
05		0603	
06		0805	
07		1206	
08		2010	

ESCC/PHR CODIFICATION CORRESPONDANCE TABLES		
TEMPERATURE COEFFICIENT	ESCC CODE	PHR CODE
5 ppm/°C (+ 22 °C; + 70 °C)	0	Z
10 ppm/°C (- 55 °C; + 155 °C)	1	Y
25 ppm/°C (- 55 °C; + 155 °C)	2	E
5 ppm/°C (- 55 °C; + 155 °C)	9	C

ESCC/PHR CODIFICATION CORRESPONDANCE TABLES		
TOLERANCE	ESCC CODE	PHR CODE
0.1 %	B	B
0.05 %	W	W
0.02 %	P	P
0.01 %	L	L



GLOBAL PART NUMBER INFORMATION																	
LIMITED TO 18 DIGITS: If more digits are necessary a codification of some digits might be necessary																	
P	H	R	0	6	0	3	Y	1	0	0	3	B	B	T	0	1	4
TYPE		TCR			OHMIC VALUE			TOLERANCE			TERMINATION		PACKAGING		OPTION		
PHR0402 PHR0603 PHR0805 PHR1206 PHR2010		Y = ± 10 ppm/°C E = ± 25 ppm/°C Z = 5 ppm/°C (+ 22 °C; + 70 °C) C = 5 ppm/°C (- 55 °C; + 155 °C)			The first three digits are significant figures and the last digit specifies the number of zero to follow. R designates decimal point. Example: 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ			L = ± 0.01 % P = ± 0.02 % W = ± 0.05 % B = ± 0.10 %			B: SnPb over nickel barrier G: Gold		For more information see Codification of Packaging table		Leave blank if no option		

Note

- Terminations B: Variants 01/03/05/07 and 13
- Terminations G: Variants 02/04/06/08 and 14

GLOBAL PART NUMBER INFORMATION															
ESCC Code															
4	0	0	1	0	2	3	0	1	1	0	0	3	B	1	T
ESCC SPEC		VARIANT			OHMIC VALUE			TOLERANCE			TCR			PACKAGING	
4001023		13 or 14 = 0402 01 or 05 = 0603 02 or 06 = 0805 03 or 07 = 1206 04 or 08 = 2010			The first three digits are significant figures and the last digit specifies the number of zero to follow. R designates decimal point. Example: 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ			L = ± 0.01 % P = ± 0.02 % W = ± 0.05 % B = ± 0.10 %			1 = ± 10 ppm/°C 0 = ± 5 ppm/°C (+ 22 °C; + 70 °C) 2 = ± 25 ppm/°C 9 = ± 5 ppm/°C (- 55 °C; + 155 °C)			T = For tape and reel (leave blank for waffle pack)	

CODIFICATION PACKAGING - Waffle Pack	
CODE 18	PACKAGING
W	25 min. (100 min. for size 0402), 1 mult
WA	100 min., 100 mult <sup>(1)</sup>

CODIFICATION PACKAGING - Plastic Tape <sup>(2)</sup>	
CODE 18	PACKAGING
T	50 min. (100 min. for size 0402), 1 mult
TA	100 min., 100 mult
TB	250 min., 250 mult
TC	500 min., 500 mult
TD	1000 min., 1000 mult
TE	2500 min., 2500 mult
TF	Full tape <sup>(3)</sup>

CODIFICATION PACKAGING - Paper Tape <sup>(2)</sup>	
CODE 18	PACKAGING
PT	100 min., 1 mult
PA	100 min., 100 mult
PB	250 min., 250 mult
PC	500 min., 500 mult
PD	1000 min., 1000 mult
PE	2500 min., 2500 mult
PF	Full tape <sup>(3)</sup>

Notes

- <sup>(1)</sup> Available only in size 1206.
- <sup>(2)</sup> Plastic tape in standard for all sizes except 0402. Paper tape in standard for size 0402 (option for other sizes. Availability to be checked with factory).
- <sup>(3)</sup> Qty. depending on size of chips.



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