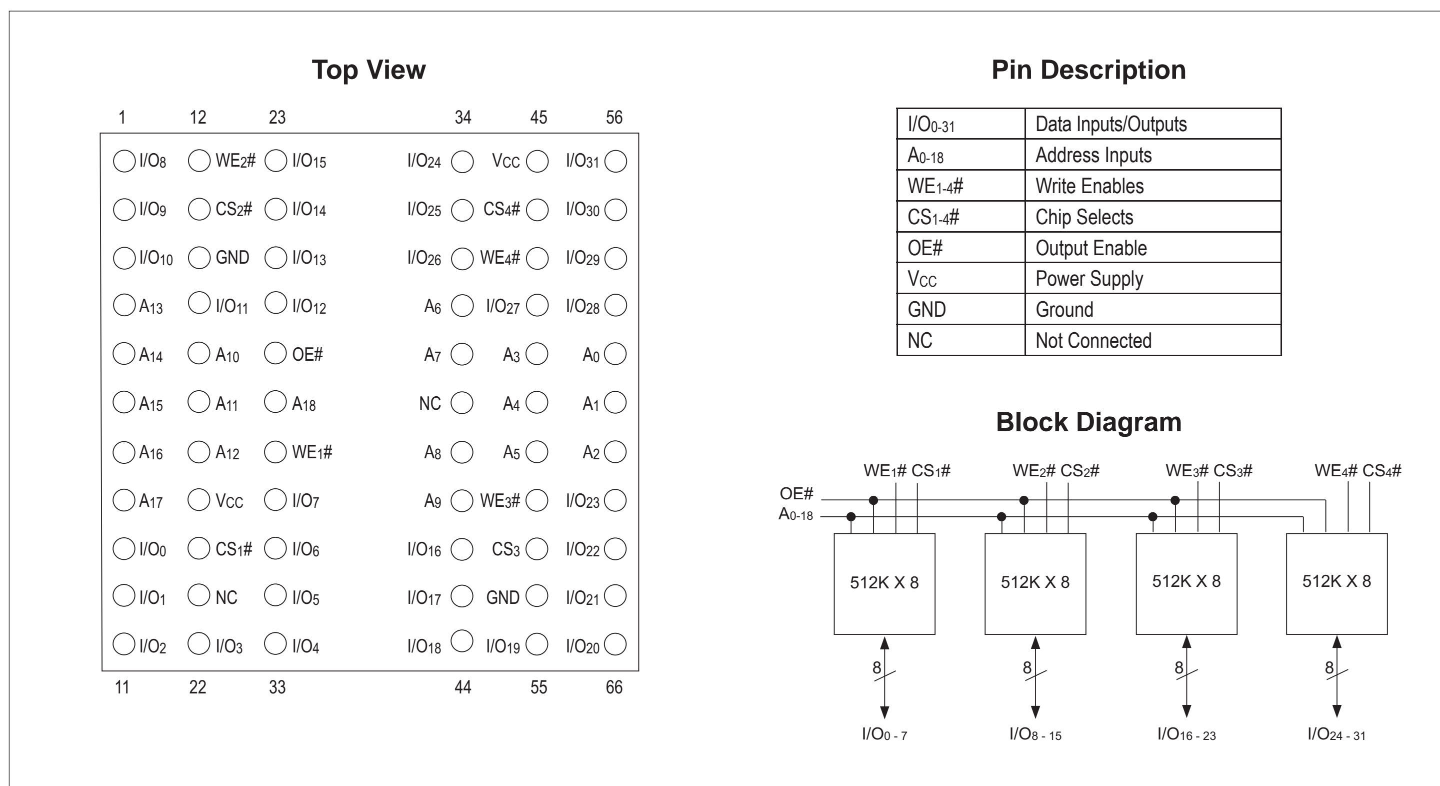
512Kx32 SRAM MODULE, SMD 5962-94611

FEATURES

- Access Times of 15, 17, 20, 25, 35, 45, 55ns
- Packaging
  - 66 pin, PGA Type, 1.075" square, Hermetic Ceramic HIP (Package 400).
  - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502)[1]
  - 68 lead, Hermetic CQFP (G2U), 22.4mm (0.880") square (Package 510) 3.56mm (0.140") height.
  - 68 lead, Hermetic CQFP (G2L), 22.4mm (0.880") square, 5.08mm (0.200") high (Package 528).
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
- WS512K32N-XH1X - 13 grams typical
  WS512K32-XG2UX - 8 grams typical
  WS512K32-XG4TX[1] - 20 grams typical
  WS512K32-XG2LX - 8 grams typical

* This product is subject to change without notice.
Note 1: Package Not Recommended For New Design

FIGURE 1 – PIN CONFIGURATION FOR WS512K32N-XH1X



Pin Description

Pin	Description
I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

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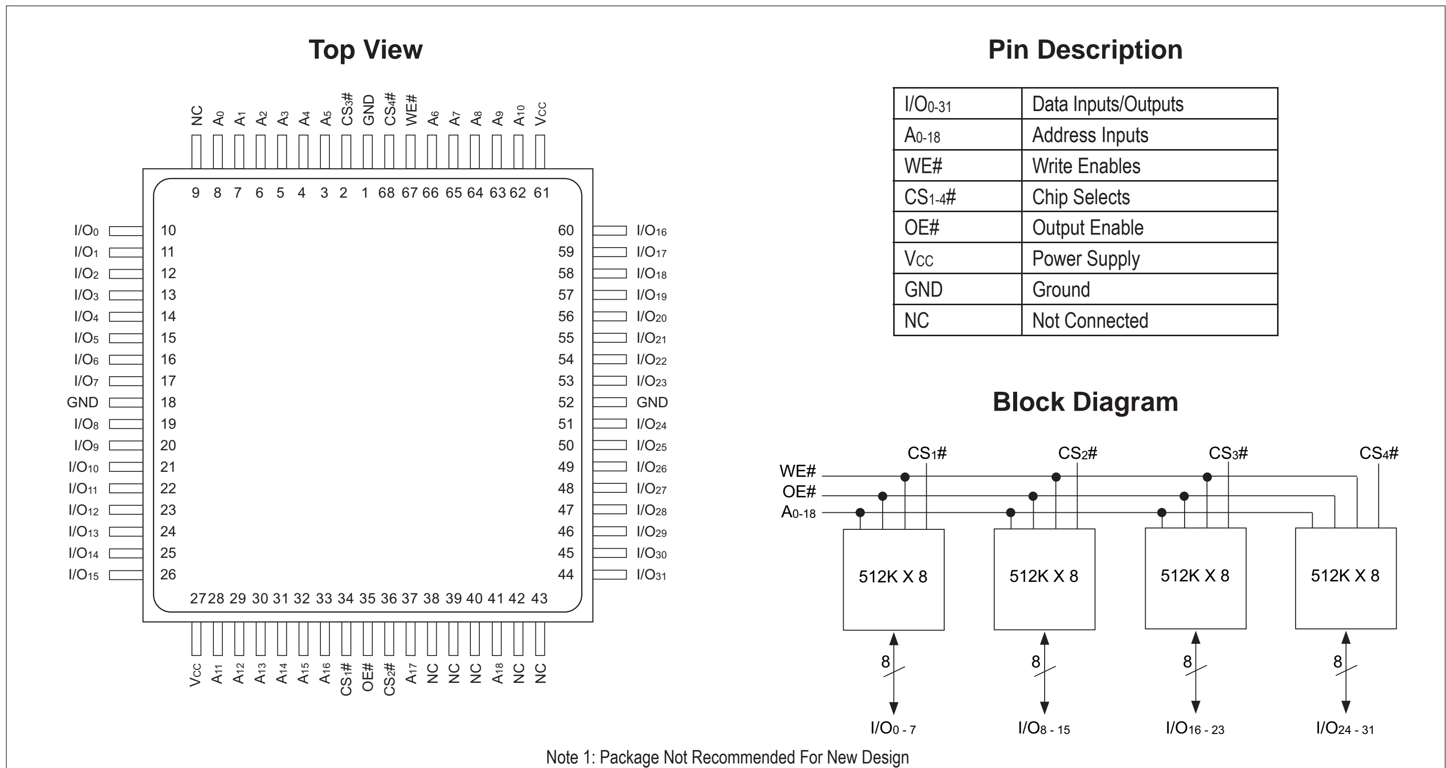
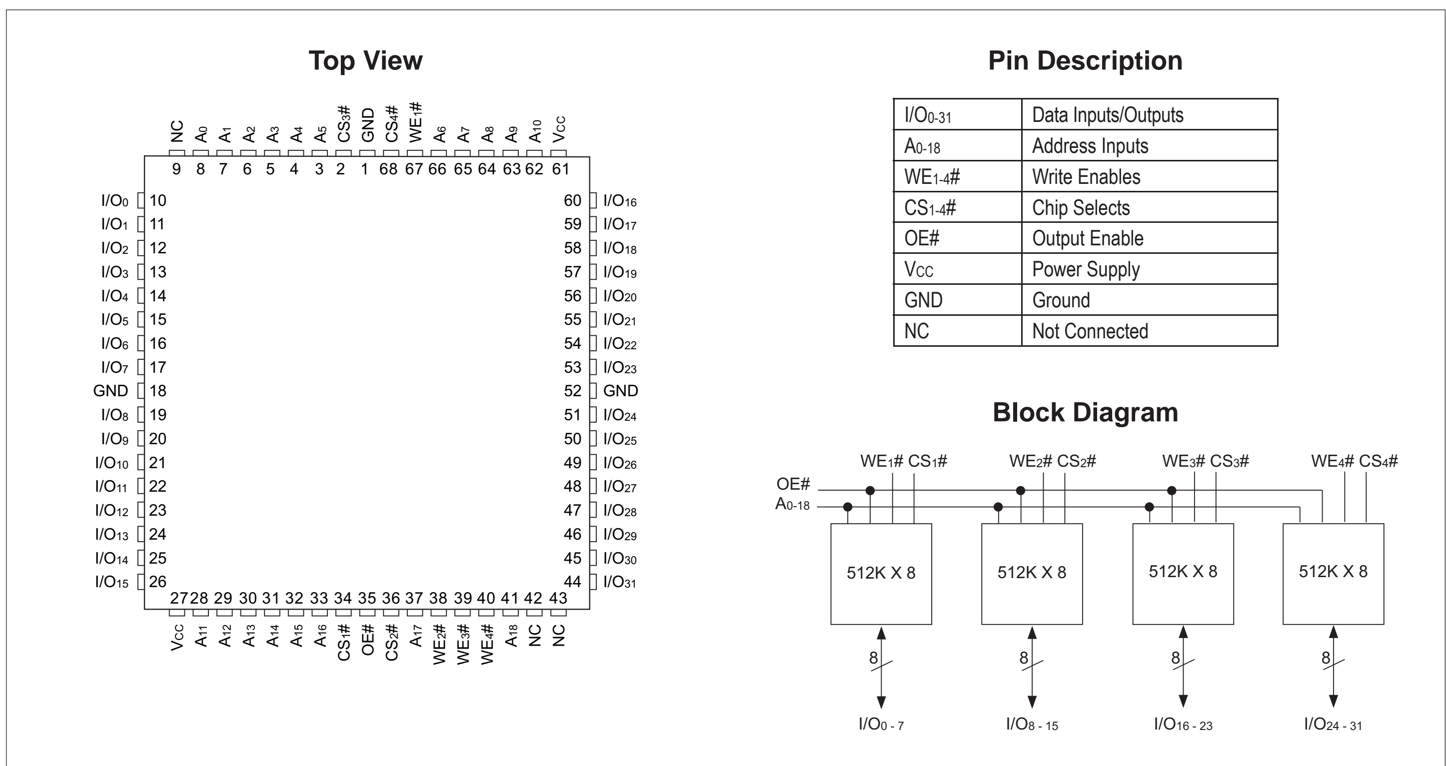
FIGURE 2 – PIN CONFIGURATION FOR WS512K32-XG4TX[1]



I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

Note 1: Package Not Recommended For New Design

FIGURE 3 – PIN CONFIGURATION FOR WS512K32-XG2UX AND WS512K32-XG2LX



I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
WE1-4#	Write Enables
CS1-4#	Chip Selects
OE#	Output Enable
VCC	Power Supply
GND	Ground
NC	Not Connected

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	V_{CC}+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

TRUTH TABLE

CS	OE	WE	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

CAPACITANCE

Ta = +25°C

Parameter	Symbol	Conditions	Max	Unit
OE# capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
WE_{1-4}# capacitance HIP (PGA)	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
CQFP G4T			50	
CQFP G2U/G2L			20	
CS_{1-4}# capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	CS# = V_{IH}, OE# = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	I_{CC} x 32	CS# = V_{IL}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		660	mA
Standby Current	I_{SB}	CS# = V_{IH}, OE# = V_{IH}, f = 5MHz, V_{CC} = 5.5		80	mA
Output Low Voltage	V_{OL}	I_{OL} = 6mA for 15 - 35ns, I_{OL} = 2.1mA for 45 - 55ns, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA for 15 - 35ns, I_{OH} = -1.0mA for 45 - 55ns, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(Ta = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Data Retention Supply Voltage	V_{DR}	CS ≥ V_{CC} − 0.2V	2.0	5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		28	mA
Low Power Data Retention Current (WS512K32L-XXX)	I_{CCDR2}	V_{CC} = 3V		16	mA

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AC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Read Cycle	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15		17		20		25		35		45		55		ns
Address Access Time	t_{AA}		15		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		8		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		12		12		12		15		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		12		12		12		15		20		20	ns

1. This parameter is guaranteed by design but not tested.

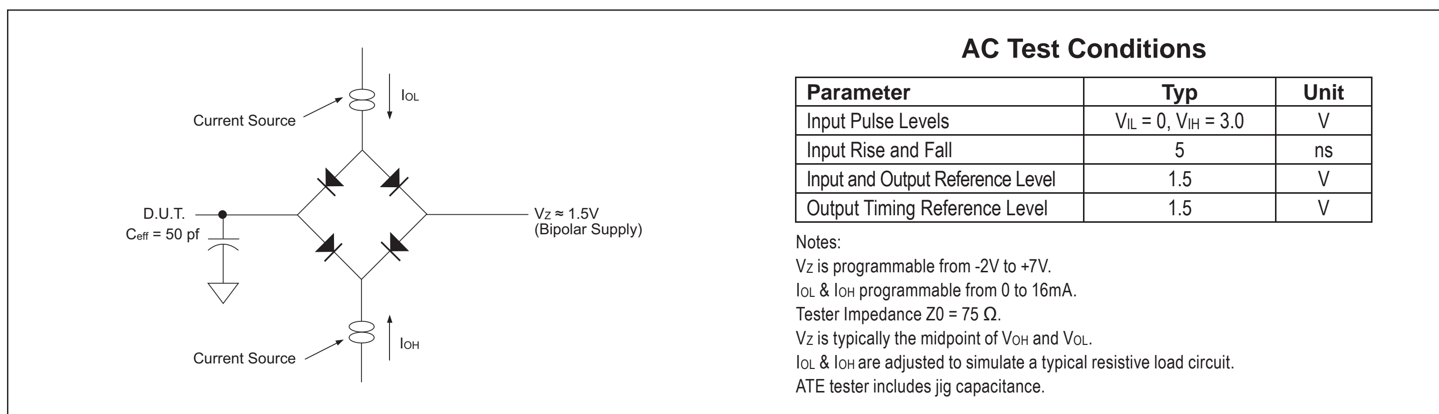
AC CHARACTERISTICS

V_{CC} = 5.0V, V_{SS} = 0V, -55°C ≤ T_A ≤ +125°C

Parameter Write Cycle	Symbol	-15		-17		-20		-25		-35		-45		-55		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15		17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	13		15		15		17		25		35		50		ns
Address Valid to End of Write	t_{AW}	13		15		15		17		25		35		50		ns
Data Valid to End of Write	t_{DW}	10		11		12		13		20		25		25		ns
Write Pulse Width	t_{WP}	13		15		15		17		25		35		40		ns
Address Setup Time	t_{AS}	2		2		2		2		2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		0		0		5		5		ns
Output Active from End of Write	t_{OW}[1]	2		2		3		4		4		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		8		9		11		13		15		20		20	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.
2. The Address Setup Time of minimum 2ns is for the G2U, G1U and H1 packages. t_{AS} minimum for the G4T package is 0ns.

FIGURE. 4 – AC TEST CIRCUIT



AC Test Conditions

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

Notes:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

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FIGURE 5 – TIMING WAVEFORM - READ CYCLE

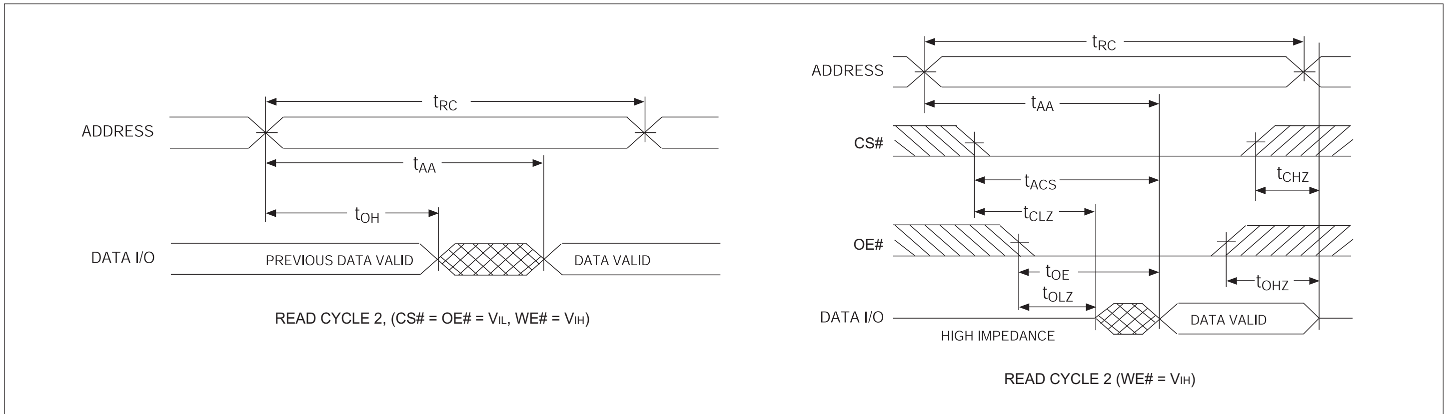


FIGURE 6 – WRITE CYCLE - WE# CONTROLLED

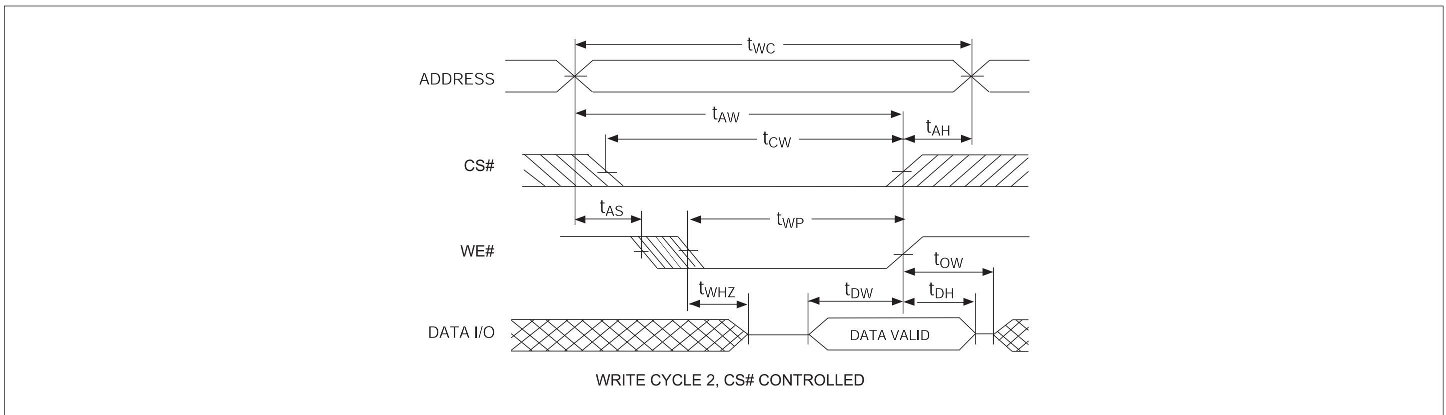
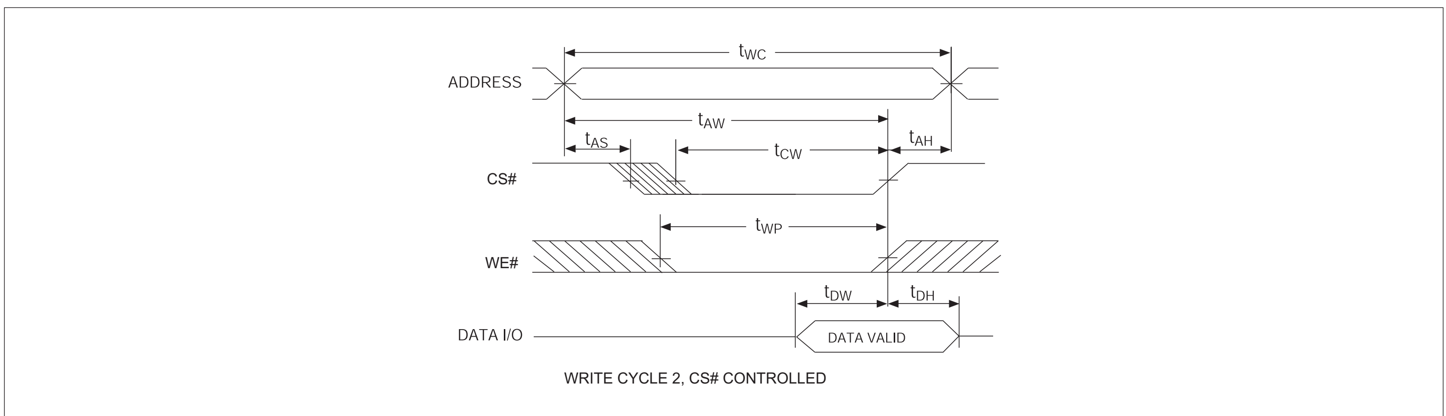
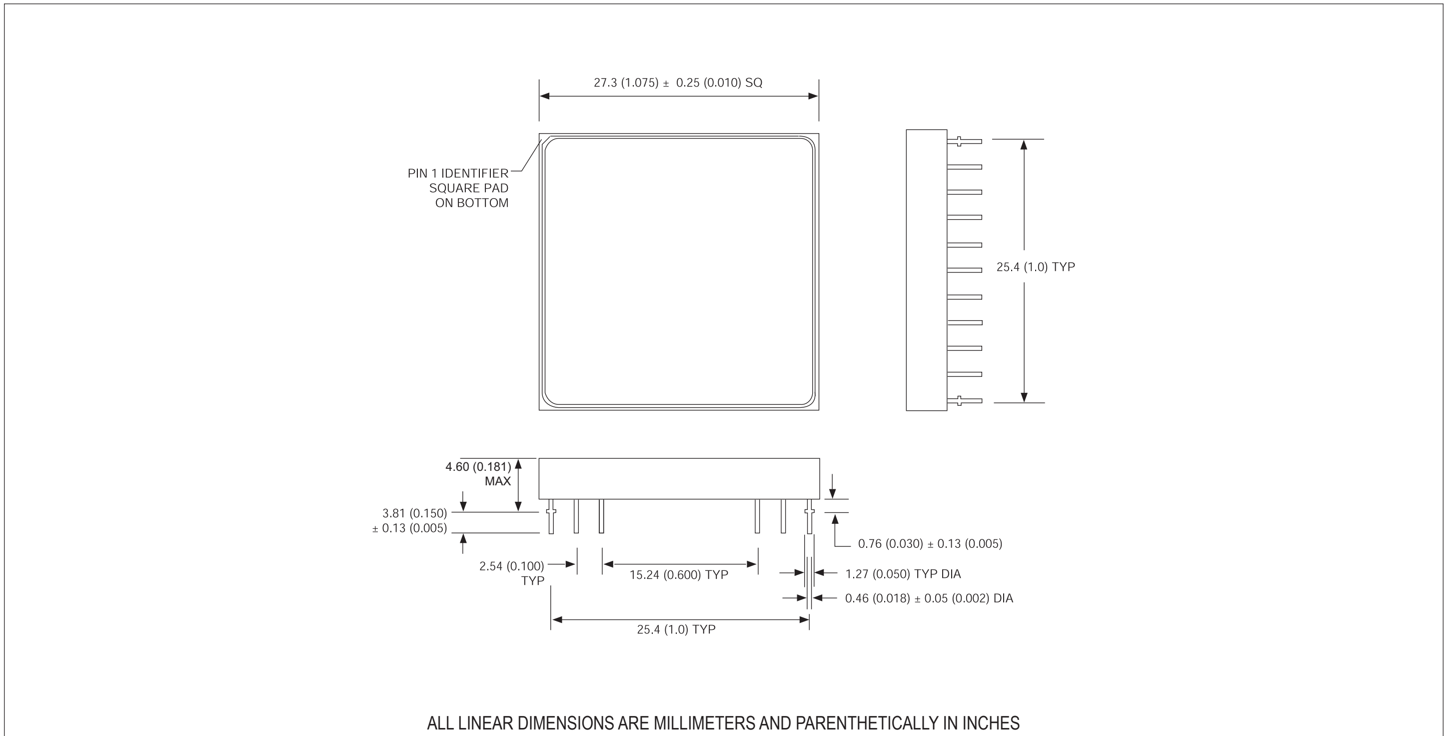


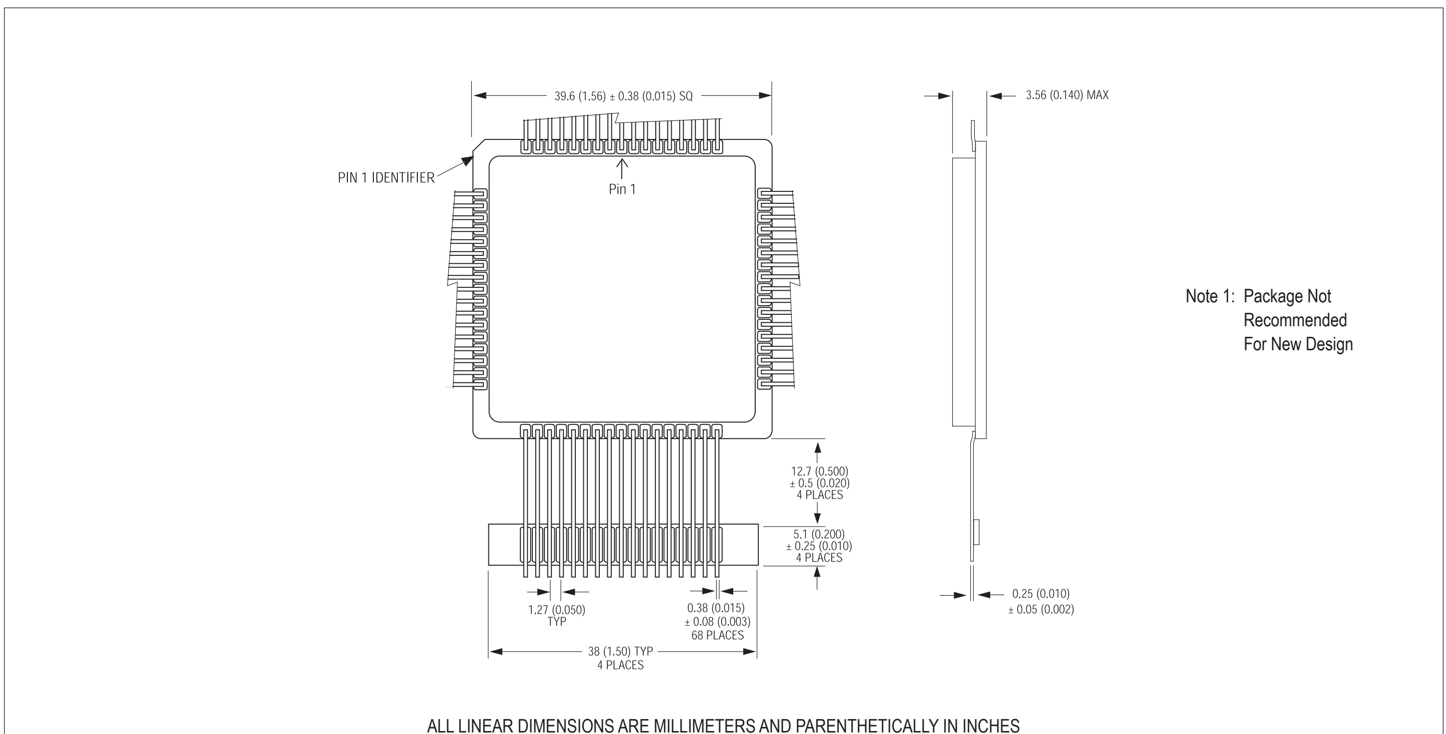
FIGURE 7 – WRITE CYCLE - CS# CONTROLLED



PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)[1]



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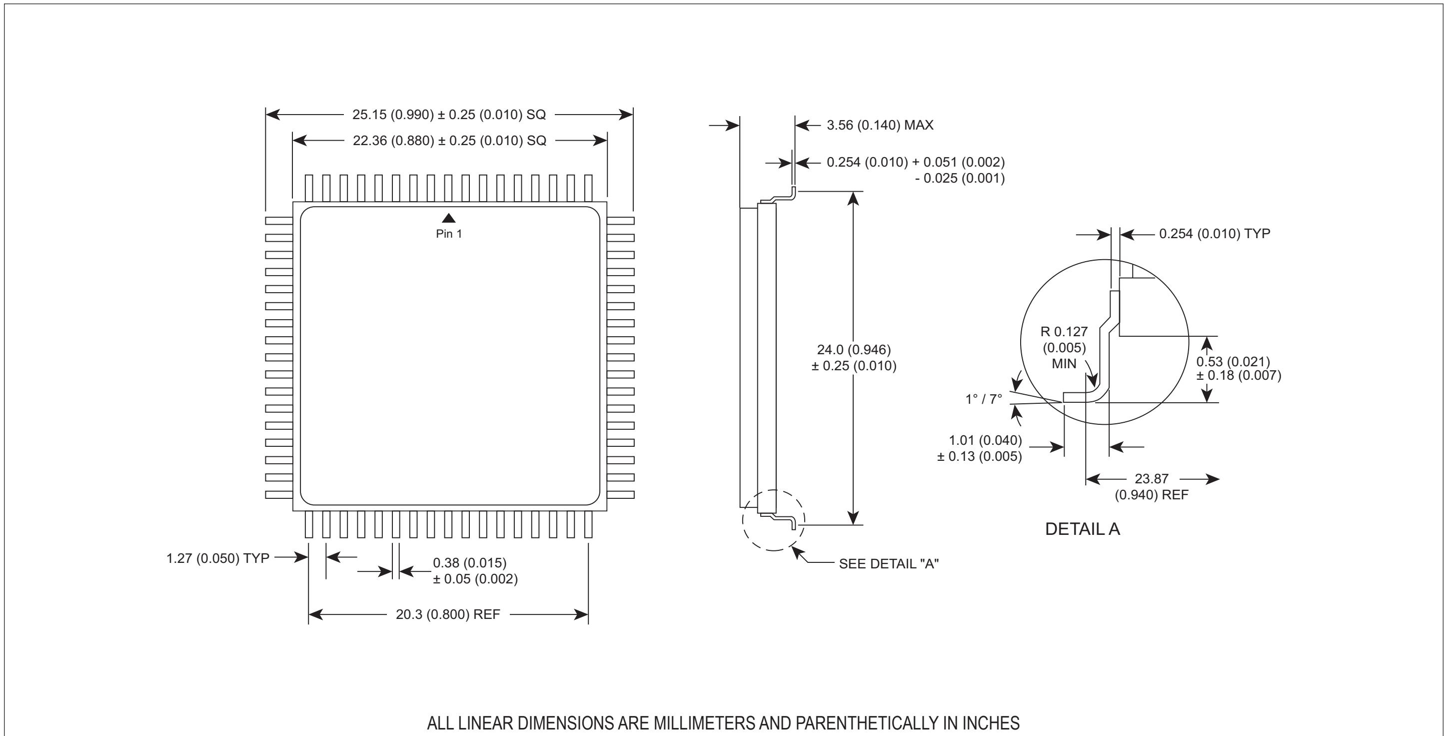
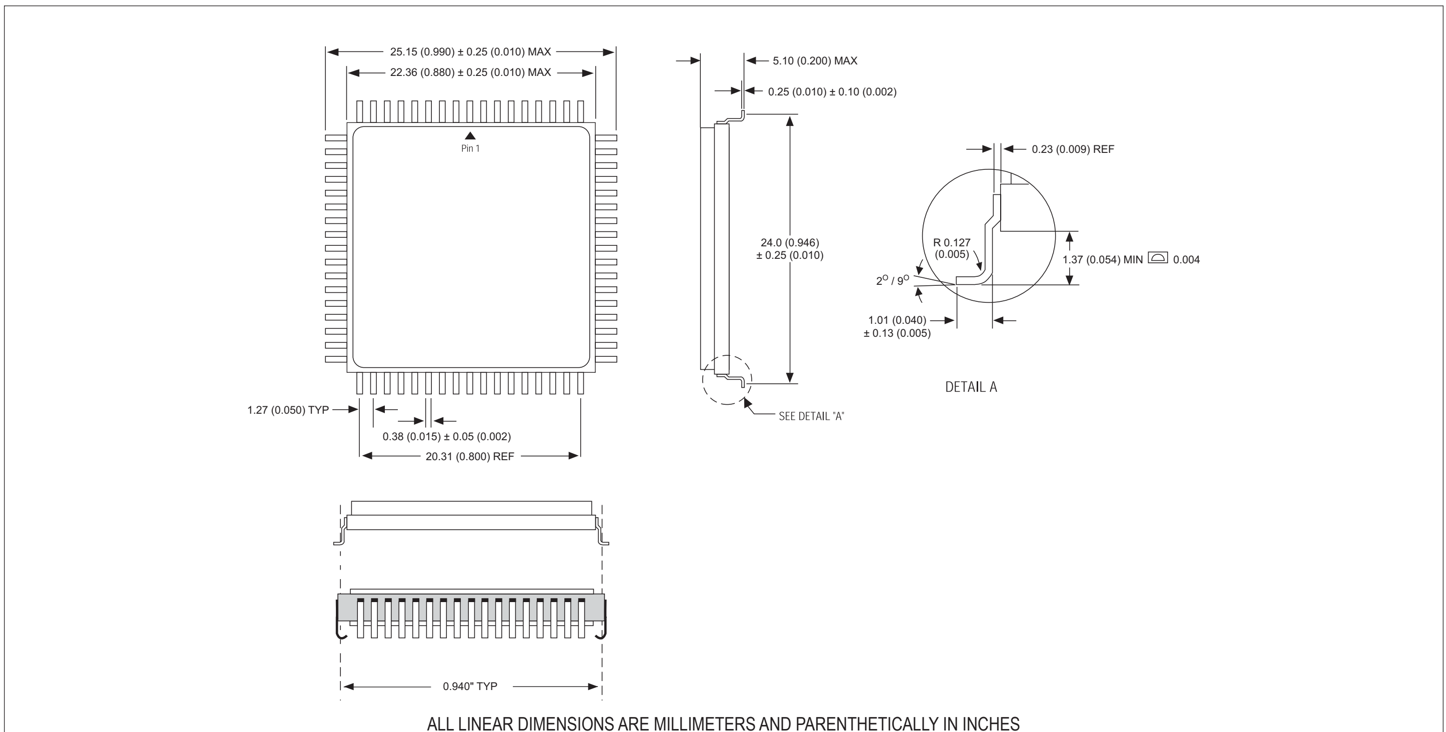
PACKAGE 510: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2U)



PACKAGE 528: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2L)



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ORDERING INFORMATION

W S 512K 32 X - XXX X X X

MICROSEMI CORPORATION — W

SRAM — S

ORGANIZATION, 512Kx32 — 512K 32
User configurable as 1Mx16 or 2Mx8

IMPROVEMENT MARK: — X
- Blank = Standard Power
- N = No Connect at pin 21 and 39 in HIP for Upgrades
- L = Low Power Data Retention

ACCESS TIME (ns) — XXX

PACKAGE TYPE: — X
- H1 = Ceramic Hex-In-line Package, HIP (Package 400)
- G2U = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 510)
- G2L = 22.4mm Ceramic Quad Flat Pack, CQFP (Package 528)
- G4T* = 40mm Low Profile CQFP (Package 502)

DEVICE GRADE: — X

Q	=	Military Grade**	
M	=	Military Screened	-55°C to +125°C
I	=	Industrial	-40°C to 85°C
C	=	Commercial	0°C to +70°C

LEAD FINISH: — X
- Blank = Gold plated leads
- A = Solder dip leads

* Package Not Recommended For New Design
** This product is processed the same as the 5962-XXXXXHXX product but all test and mechanical requirements are per the Microsemi data sheet.

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DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-94611 05HTX
512K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-94611 06HTX
512K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-94611 07HTX
512K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-94611 08HTX
512K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-94611 09HTX
512K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-94611 10HTX
512K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-94611 19HTX
512K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 05HYX
512K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 06HYX
512K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 07HYX
512K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 08HYX
512K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 09HYX
512K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)[1]	5962-94611 10HYX
512K x 32 SRAM Module	55ns	68 lead CQFP (G2U)	5962-94611 05HMX
512K x 32 SRAM Module	45ns	68 lead CQFP (G2U)	5962-94611 06HMX
512K x 32 SRAM Module	35ns	68 lead CQFP (G2U)	5962-94611 07HMX
512K x 32 SRAM Module	25ns	68 lead CQFP (G2U)	5962-94611 08HMX
512K x 32 SRAM Module	20ns	68 lead CQFP (G2U)	5962-94611 09HMX
512K x 32 SRAM Module	17ns	68 lead CQFP (G2U)	5962-94611 10HMX
512K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-94611 19HMX
512K x 32 SRAM Module	55ns	68 lead CQFP (G2L)	5962-94611 05HAX
512K x 32 SRAM Module	45ns	68 lead CQFP (G2L)	5962-94611 06HAX
512K x 32 SRAM Module	35ns	68 lead CQFP (G2L)	5962-94611 07HAX
512K x 32 SRAM Module	25ns	68 lead CQFP (G2L)	5962-94611 08HAX
512K x 32 SRAM Module	20ns	68 lead CQFP (G2L)	5962-94611 09HAX
512K x 32 SRAM Module	17ns	68 lead CQFP (G2L)	5962-94611 10HAX
512K x 32 SRAM Module	15ns	66 pin HIP (H1)	5962-94611 19HAX

Note 1: Package Not Recommended For New Design

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Document Title

512K x 32 SRAM Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial	October 1996	Preliminary
Rev 1	Change (Pg. 1, 3) 1.1 Change Operation Supply Current from 520mA To 540mA 1.2 Change Data Retention Current from 12mA to 28mA.	September 2002	Advanced
	Change (Pg. 1, 2, 8, 10, 11) 1.1 Delete G2 Package	November 1997	Preliminary
	Change (Pg. 1, 9) 1.1 Add SMD Case Outline M for G2T	February 1998	Preliminary
	Change (Pg. 1, 3, 8) 1.1 Remove Low Capacitance package option	April 1998	Preliminary
	Change (Pg. 1, 6, 8) 1.1 Add H1 package	December 1998	Preliminary
	Change (Pg. 1, 4, 6, 9, 10) 1.1 Remove H2 package 1.2 Change logo to WEDC logo	March 1999	Preliminary
Rev 2	Change (Pg. 1, 3, 4, 8) 2.1 Change status from Preliminary to Final 2.2 Make package descriptions consistent 2.3 Add 15ns as available in Commercial and Industrial Temperatures only.	May 1999	Final
Rev 4	Change (Pg. 1, 3) 4.1 Change Standby Current (Isb) from 60mA to 80mA Maximum	June 1999	Final
Rev 5	Change (Pg. 1, 2, 3, 4, 7, 8) 5.1 Add G1U package	November 1999	Final
Rev 6	Change (Pg. 1, 8) 6.1 Change G1U lead foot length from 0.64mm to 0.84mm Ref	February 2000	Final
Rev 7	Change (Pg. 1, 3, 9) 7.1 Change Operating Supply Current from 540mA to 660mA Maximum 7.2 Add Low Power Data Retention Current of 16mA to Data Retention Characteristics table 7.3 Add Low Power Data Retention (L) option to Ordering Information	October 2000	Final
Rev 8	Change (Pg. 1, 2, 6, 7, 9, 10) 8.1 Change G2T and G4T package status to Not Recommended For New Design	October 2001	Final
Rev 9	Change (Pg. 1, 2, 3, 8, 9, 10) 9.1 Add G1T package 9.2 Remove 'Hi-Reliability Product' Title	November 2001	Final
Rev 10	Change (Pg. 1, 2, 3, 4, 7, 8, 9, 10, 11) 10.1 Remove G2T package 10.2 Add G2U package 10.3 Remove 'Package to be Developed' note for G4T	August 2002	Final
Rev 11	Change (Pg. 1,2,4,8,10,11,13) 11.1 Change G1U package status to Not Recommended For New Designs	February 2002	Final
Rev 12	Change (Pg. 1,2,3,7,8,10,11,13) 12.1 Add G2L package	May 2003	Final
Rev 13	Change (Pg. 1,2,3,7,8,10,11,13) 13.1 Remove all reference to G1U package 13.2 Remove all reference to G1T package	December 2003	Final

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Document Title

512K x 32 SRAM Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 14	Change (Pg. 1,3,11) 14.1 Change I_{OL} to 6mA for 15-35 ns	May 2004	Final
Rev 15	Change (Pg. 1,4,11) 15.1 Add 15ns for Military Temperature	November 2004	Final
Rev 16	Change (Pg. 1, 6, 11) 16.1 Correct thickness to 0.181"per PCN#140A00143	March 2006	Final
Rev 17	Change (Pg. 1, 2, 11) 17.1 Correct pinout of G4T 17.2 Correct G2L foot length	May 2006	Final
Rev 18	Change (Pg. 6) 18.1 Change drawing on HIP to generic square drawing	November 2010	Final
Rev 19	Change (Pg. 8) 19.1 Swap positions with 'Access Time' and 'Improvement Mark' in the 'Ordering Information' chart	September 2011	Final
Rev 20	Change (Pg. 8) 20.1 Changed Device Grade "Q" description from "MIL-STD-883 Compliant" to "MIL-PRF-38534 Class H Compliant."	May 2014	Final
Rev 21	Change (Pg. 8) 21.1 Changed Device Grade "Q" description from "MIL-PRF-38534 Class H Compliant." to "Military Grade."	August 2014	Final
Rev 22	Change (Pg. 7) (ECN 9936) 22.1 Update package 510 dimensions	April 2016	Final

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