TMC2250
Matrix Multiplier
12 x 12 Bits, 40 MHz

Description

The TMC2250 is a flexible high-performance nine-multiplier array VLSI circuit which can execute a cascadeable 9-tap FIR filter, a cascadeable 4 x 2 or 3 x 3-pixel image convolution, or a 3 x 3 color space conversion. All configurations offer throughput at up to the maximum guaranteed 40 MHz clock rate with 12-bit data and 10-bit coefficients. All inputs and outputs are registered on the rising edges of the clock.

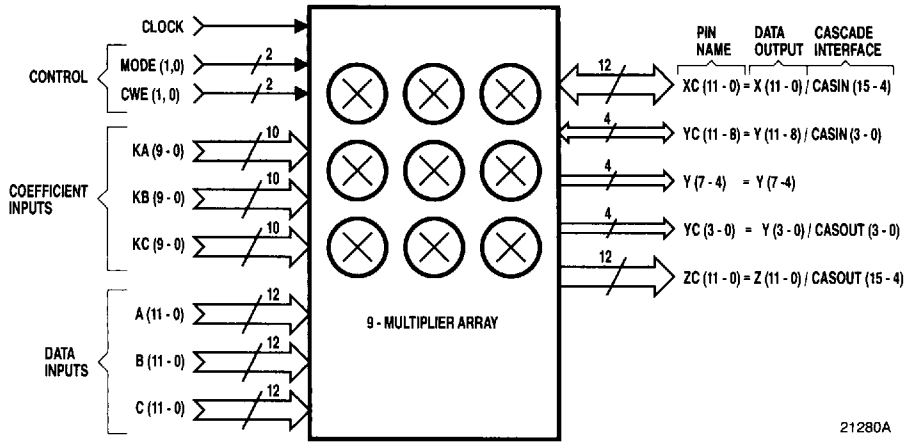
The 3 x 3 matrix multiply or color conversion configuration can perform video standard conversion (YIQ or YUV to RGB, etc.) or three-dimensional perspective translation at real-time video rates.

The 9-tap FIR filter configuration, useful in Video, Telecommunications, and Signal Processing, features a 16-bit cascade input to allow construction of longer filters.

The cascadeable 3 x 3 and 4 x 2-pixel image convolver functions allow the user to perform numerous image processing functions, including static filters and edge detectors. The 16-bit cascade input port facilitates two-chip 40 MHz cubic convolution (4 x 4-pixel kernel).

The TMC2250 is fabricated in a one-micron CMOS process and operates at clock speeds of up to 40 MHz over the full commercial (0°C to 70°C) temperature and supply voltage ranges. It is available in a 121-pin plastic pin grid array (PPGA) package. All input and output signals are TTL compatible.

Logic Symbol



Features

- Four User-Selectable Filtering And Transformation Functions:
  - Triple Dot Product (3 x 3) Matrix Multiply
  - Cascadeable 9-Tap Systolic FIR Filter
  - Cascadeable 3 x 3-Pixel Image Convolver
  - Cascadeable 4 x 2-Pixel Image Convolver
- 40MHz (25ns) Pipelined Throughput
- 12-Bit Input And Output Data, 10-Bit Coefficients
- 16-Bit Cascade Input And Output Ports In All Filter Modes
- Onboard Coefficient Storage, With Three-Cycle Updating Of All Nine Coefficients

Applications

- Image Filtering And Manipulation
- Video Effects Generation
- Video Standards Conversion And Encoding/Decoding
- Three-Dimensional Image Manipulation
- Medical Image Processing
- Edge Detection For Object Recognition
- FIR Filtering For Communications Systems

Functional Description

General Information

The TMC2250 is a nine-multiplier array with the internal bus structure and summing adders needed to implement a 3 x 3 matrix multiplier (triple dot product) or cascadeable 9-tap FIR filter, 3 x 3-pixel convolver, or 4 x 2-pixel convolver, all in one monolithic circuit. With a 30MHz guaranteed maximum clock rate, this device offers video and imaging system designers a single-chip solution to numerous common image and signal-processing problems.

The three data input ports (A, B, C) accept 12-bit two's complement integer data, which is also the format for the output ports (X, Y, Z) in the matrix multiply mode (Mode 00). In the filter configurations (Modes 01, 10, and 11), the cascade ports assume 12-bit integer, 4-bit fractional two's complement data on both input and output. The coefficient input ports (KA, KB, KC) are always 10-bit two's complement fractional. ***Table 1*** details the bit weighting of the input and output data in all configurations.

Operating Modes

The TMC2250 can implement four different digital filter architectures. Upon selection of the desired function by the user ($MODE_{1-0}$), the device reconfigures its internal data paths and input and output buses appropriately. The output ports (XC, YC, and ZC) are configured in all filter modes as 16-bit Cascade In and Cascade Out ports so that multiple devices can be connected to build larger filters. These modes are described individually below. The I/O pin-function configurations for all four modes are shown in ***Table 1***.

Definitions

The calculations performed by the TMC2250 in each mode are also shown below, utilizing the following notation:

A(1), B(5), C(2), CASIN(3)	Indicates the data word presented to that input port during the specified clock rising edge (x). Applies to all input ports A_{11-0}, B_{11-0}, C_{11-0}, and $CASIN_{15-0}$.
KA1(1), KB3(4)	Indicates coefficient data stored in the specified one of the nine onboard coefficient registers KA1 through KC3, as shown in the block diagram for that mode, input during or before the specified clock rising edge (x).
X(1), Y(4), Z(6), CASOUT(6)	Indicates data available at that output port t_{DO} after the specified clock rising edge (x). Applies to all output ports X_{11-0}, Y_{11-0}, Z_{11-0}, and $CASOUT_{15-0}$.

Table 1. Data Port Formatting by Mode

Mode	Inputs						Inputs/Outputs		Outputs		
	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	XC_{11-0}	YC_{11-8}	Y_{7-4}	YC_{3-0}	ZC_{11-0}
00	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	X_{11-0}	Y_{11-8}	Y_{7-4}	Y_{3-0}	Z_{11-0}
01	A_{11-0}	A_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
10	A_{11-0}	B_{11-0}	C_{11-0}	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$
11	A_{11-0}	B_{11-0}	NC	KA_{9-0}	KB_{9-0}	KC_{9-0}	$CASIN_{15-4}$	$CASIN_{3-0}$	NC	$CASOUT_{3-0}$	$CASOUT_{15-4}$

Numeric Format

Table 2 shows the binary weightings of the input and output ports of the TMC2250. Although the internal sums of products could grow to 23 bits, in the matrix multiply mode (Mode 00) the outputs X, Y, and Z are truncated to yield 12-bit integer words. Thus the output format is identical to the input data format. In the filter configurations (Modes 01, 10, and 11) the cascade output is always half-LSB rounded to 16 bits, specifically 12 integer bits and 4 fractional guard bits, with no overflow "headroom." The user is of course free to half-LSB round the output word to any size less than 16 bits by forcing a 1 into the bit position of the cascade input immediately below the desired LSB. In all modes, bit weighting is easily adjusted if desired by applying the same scaling correction factor to both input and output data words. If the coefficients are rescaled, the relative weightings of the CASIN and CASOUT ports will differ accordingly.

Data Overflow

As shown in *Table 2*, the TMC2250's matched input and output data formats accommodate 0 dB (unity) gain. Therefore, the user must be aware of input conditions that could lead to numeric overflow. Maximum input data and coefficient word sizes must be taken into account with the specific algorithm performed to ensure that no overflow occurs.

Signal Definitions

Power

V_{DD}, GND — The TMC2250 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The TMC2250 operates from a single system clock input. All timing specifications are referenced to the rising edge of clock.

Table 2. Bit Weightings For Input and Output Data Words

Bit Weights	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	.	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}
Inputs																						
All Modes Data A, B, C	$-I_{11}$	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	.									
Coefficients KA, KB, KC												$-K_9$	.	K_8	K_7	K_6	K_5	K_4	K_3	K_2	K_1	K_0
Modes 01, 10, 11 CASIN	$-CI_{15}$	CI_{14}	CI_{13}	CI_{12}	CI_{11}	CI_{10}	CI_9	CI_8	CI_7	CI_6	CI_5	CI_4	.	CI_3	CI_2	CI_1	CI_0					
Internal Sum	X_{20}	X_{19}	X_{18}	X_{17}	X_{16}	X_{15}	X_{14}	X_{13}	X_{12}	X_{11}	X_{10}	X_9	.	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0
Outputs																						
Mode 00 X, Y, Z	$-O_{11}$	O_{10}	O_9	O_8	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	.									
Modes 01, 10, 11 CASOUT	$-CO_{15}$	CO_{14}	CO_{13}	CO_{12}	CO_{11}	CO_{10}	CO_9	CO_8	CO_7	CO_6	CO_5	CO_4	.	CO_3	CO_2	CO_1	CO_0					

Note: 1. A minus sign indicates a two's complement sign bit.

3 x 3 Matrix Multiplier (Mode 00)

This mode utilizes all six input and output ports in the basic configuration to realize a "triple dot product," in which each output is the sum of all three input words in that column multiplied by the appropriate stored coefficients. The three corresponding sums of products are available at the outputs five clock cycles after the input data are latched, and three new data words half-LSB rounded to 12 bits are then available every clock cycle.

$$X(5) = A(1)KA1(1) + B(1)KB1(1) + C(1)KC1(1)$$
$$Y(5) = A(1)KA2(1) + B(1)KB2(1) + C(1)KC2(1)$$
$$Z(5) = A(1)KA3(1) + B(1)KB3(1) + C(1)KC3(1)$$

Figure 1. 3 x 3 Matrix Multiplier Impulse Response (Mode 00)

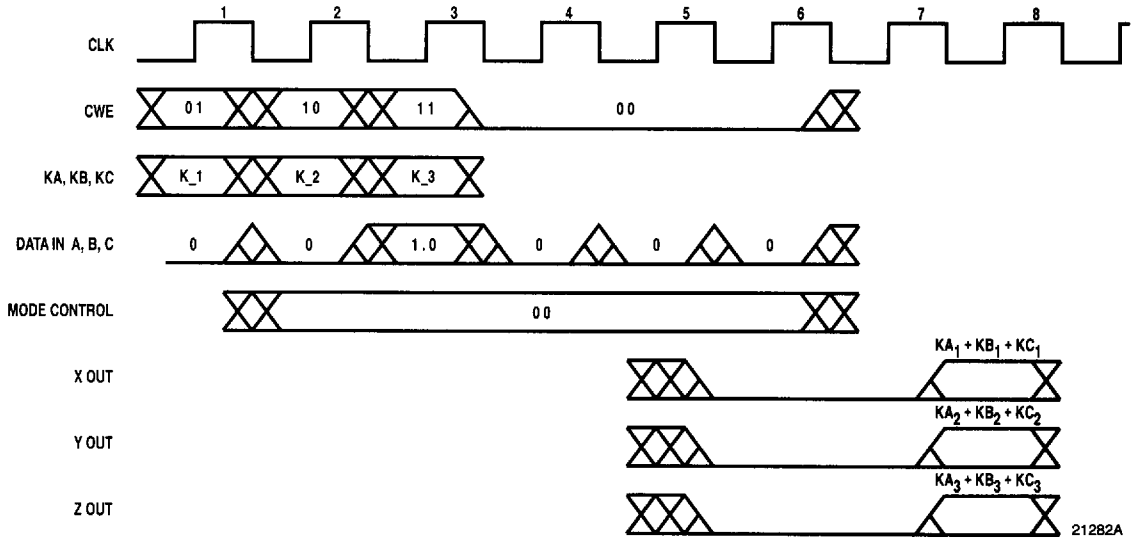
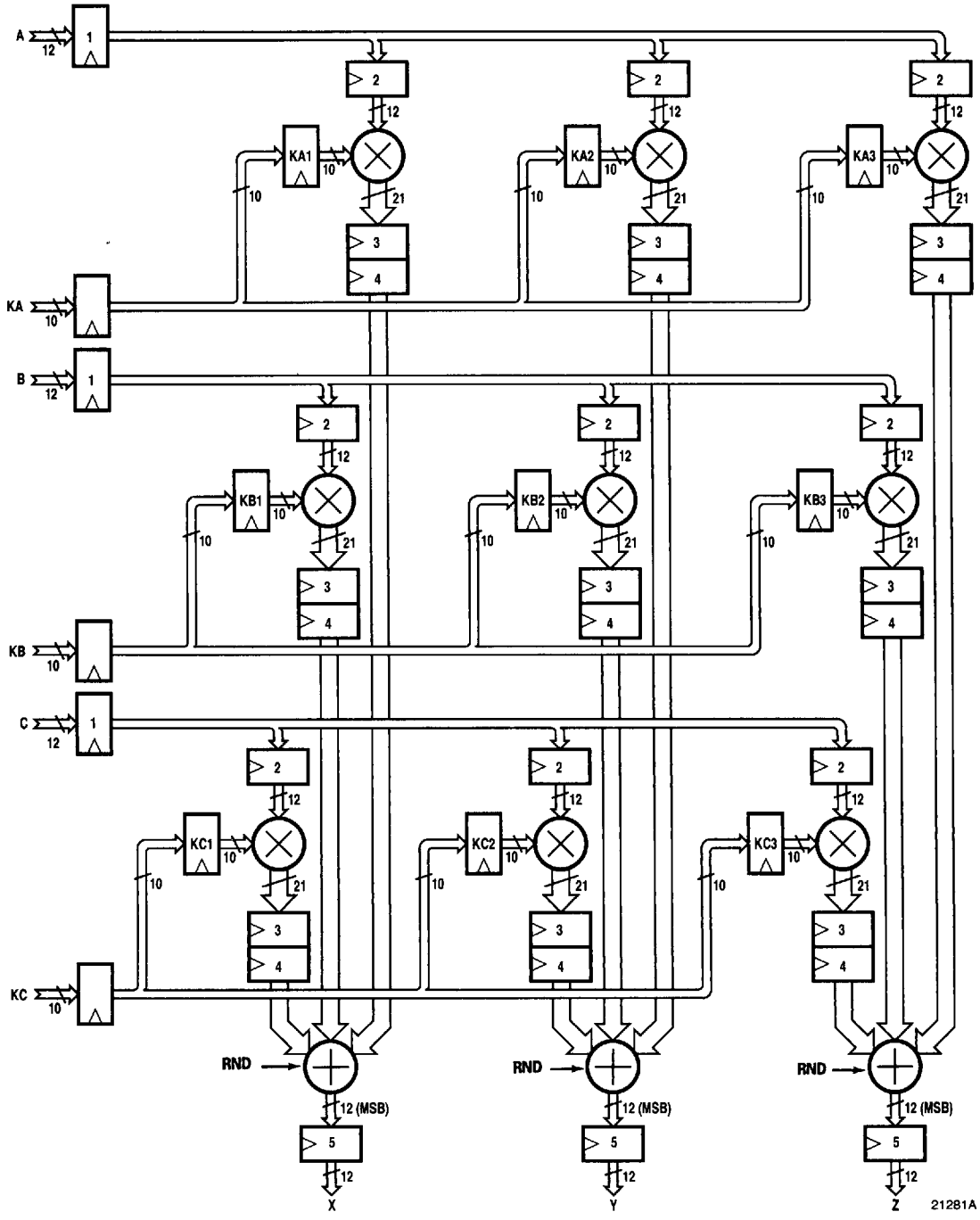


Figure 2. 3 x 3 Matrix Multiplier Configuration (Mode 00)



9-Tap FIR Filter (Mode 01)

The architecture for this configuration is shown in ***Figure 4.*** The user loads the desired coefficient set, presents input data to ports A and B simultaneously (most applications will wire the A and B inputs together), and receives the resulting 9-sample response, half-LSB rounded to 16 bits, 5 to 13 clock cycles later. A new output data word is available every clock cycle. The figure shows that the input data are automatically right-shifted one location through the row of multiplier input registers on every clock in anticipation of a new input data word.

$$\begin{aligned}CASOUT(13) = {} & A(9)KA3(9) + A(8)KA2(8) + A(7)KA1(7) \\ & + B(6)KB3(9) + B(5)KB2(8) + B(4)KB1(7) \\ & + B(3)KC3(9) + B(2)KC2(8) + B(1)KC1(7) \\ & + CASIN(10)\end{aligned}$$

Latency: Impulse in to center of 9-tap response = 9 registers. Cascade In to Cascade Out = 4 registers.

Figure 3. 9-Tap FIR Filter Impulse Response (Mode 01)

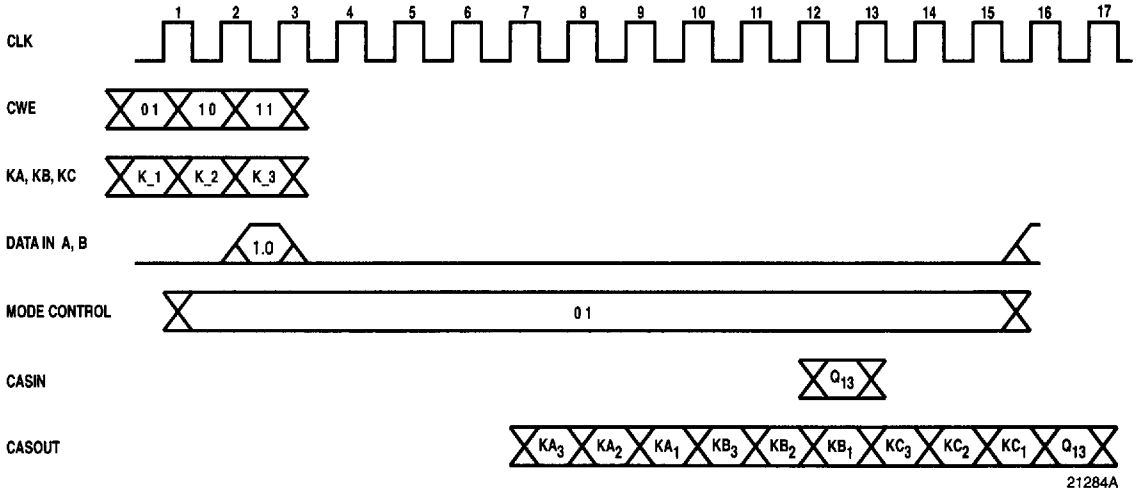
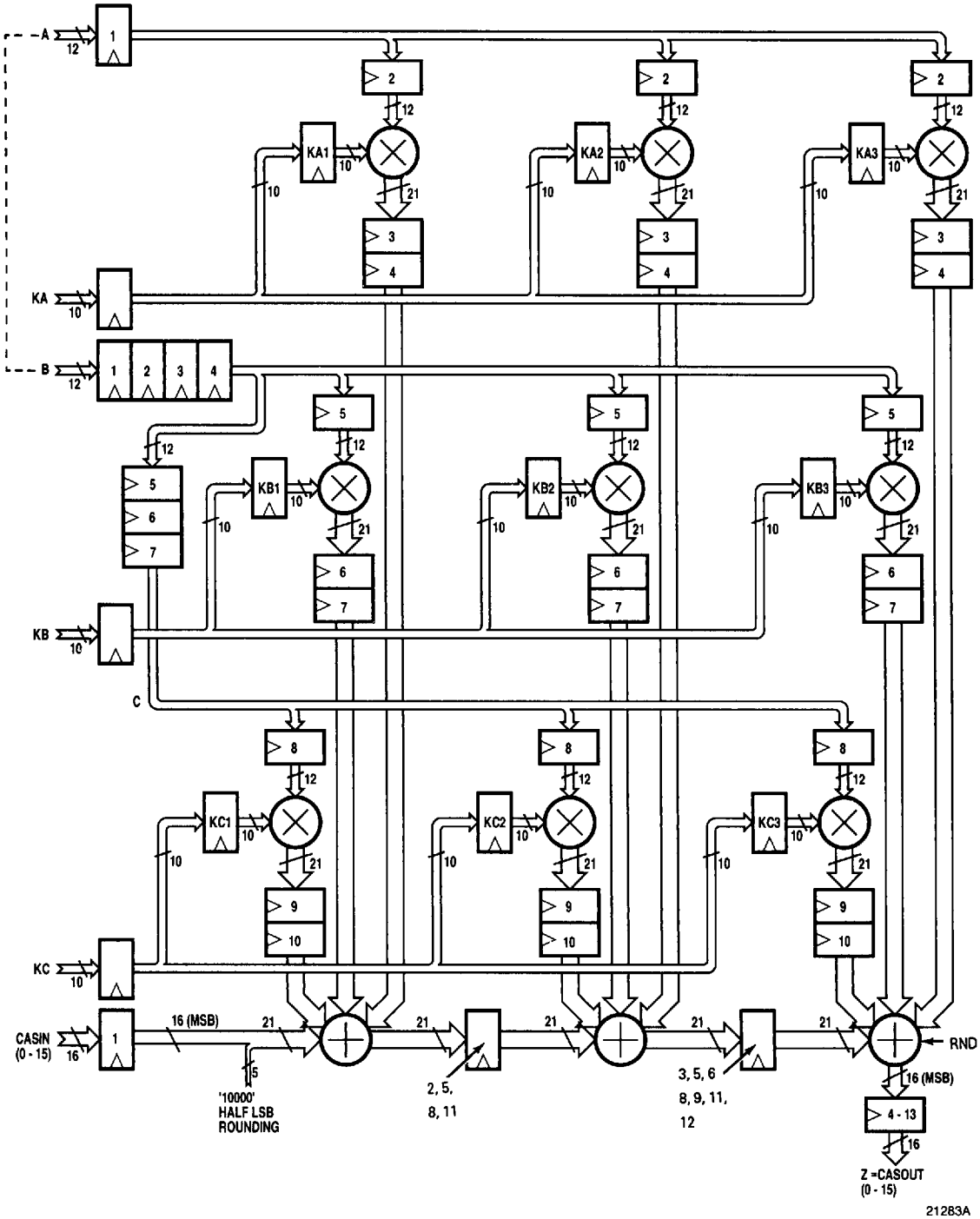


Figure 4. 9-Tap FIR Filter Configuration (Mode 01)



3 x 3-Pixel Convolver (Mode 10)

This filter configuration accepts a 3-pixel-square neighborhood, side-loaded three pixels at a time through input ports A, B, and C, and multiplies the 9 most recent pixel values by the coefficient set currently stored in the registers. These products are summed with the data presented to the cascade input, and a new 3-cycle impulse response, rounded to 16 bits, is available at the output port 5-7 clocks later, with a new output available on every clock cycle. The input pixel data are automatically shifted one location to the right through the three rows of multiplier input registers on every clock in anticipation of three new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned}CASOUT(7) = {} & A(3)KA3(3) + A(2)KA2(2) + A(1)KA1(1) \\ & + B(3)KB3(3) + B(2)KB2(2) + B(1)KB1(1) \\ & + C(3)KC3(3) + C(2)KC2(2) + C(1)KC1(1) \\ & + CASIN(4)\end{aligned}$$

Latency: Impulse in to center of 3-tap response = 6 registers. Cascade In to Cascade Out = 4 registers.

Figure 5. 3 x 3-Pixel Convolver Impulse Response (Mode 10)

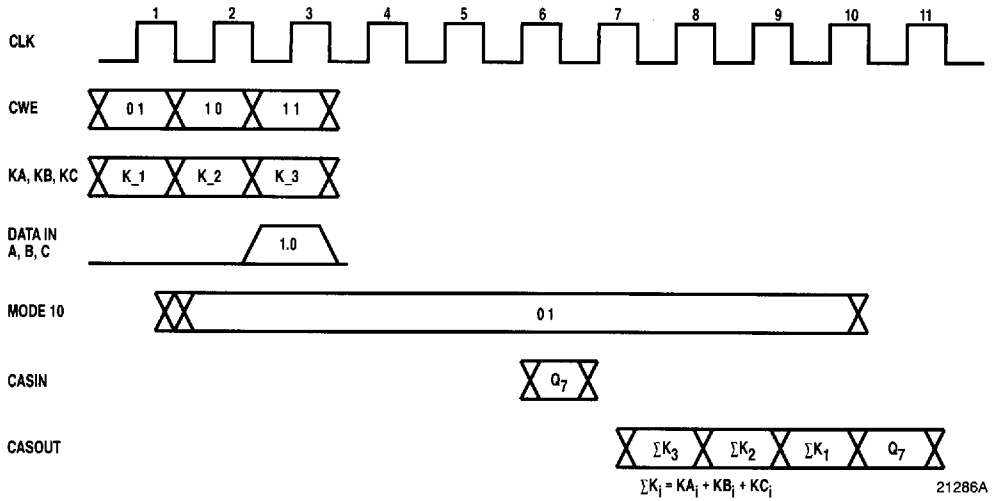
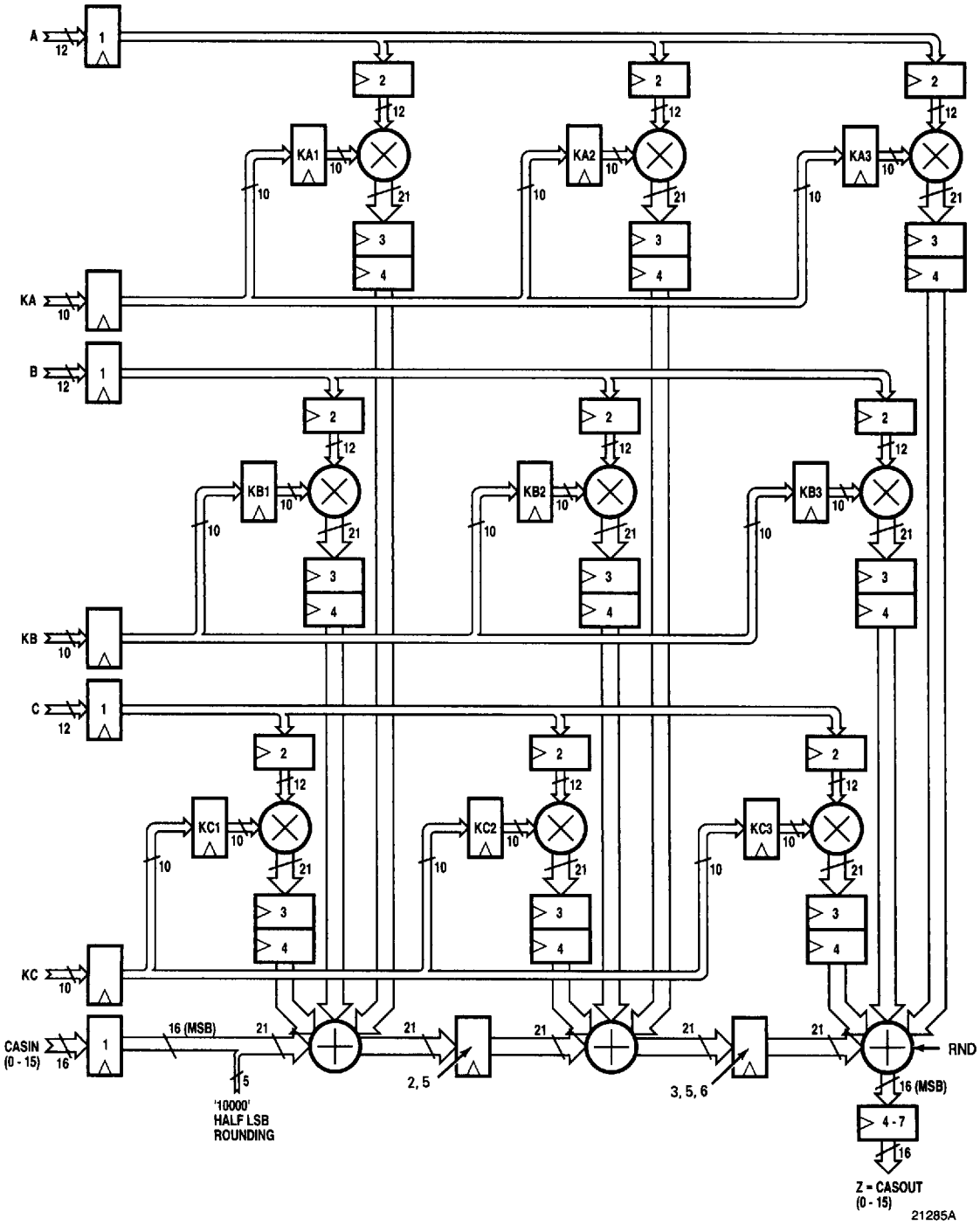


Figure 6. 3 x 3-Pixel Convolver Configuration (Mode 10)



4 x 2-Pixel Cascadeable Convolver (Mode 11)

Similar to Mode 10, the 4 x 2-pixel convolver allows the user to perform full-speed cubic convolution with only two TMC2250 devices and the TMC2111 Pipeline Delay Register to synchronize the cascade ports (see the *Applications Discussion* section). Pixel data are side-loaded into ports A and B, multiplied by the onboard coefficients, summed with the cascade input, and half-LSB rounded to 16 bits. The four-cycle impulse response emerges at the cascade output port 5 to 8 clock cycles later. A new output word is available on every clock cycle. Note that Multiplier KC2 is not used in this mode and that its stored coefficient is ignored. As shown below, the column of input pixel data is automatically shifted one location to the right through the two rows of multiplier input registers on every clock in anticipation of two new input data words, effectively sliding the convolutional window over one column in an image plane.

$$\begin{aligned}CASOUT(8) = {} & A(4)KA3(4) + A(3)KA2(3) + A(2)KA1(2) \\ & + A(1)KB3(4) + B(4)KB3(4) + B(3)KB2(3) \\ & + B(2)KB1(2) + B(1)KC1(2) + CASIN(5)\end{aligned}$$

Figure 7. 4 x 2-Pixel Convolver Impulse Response (Mode 11)

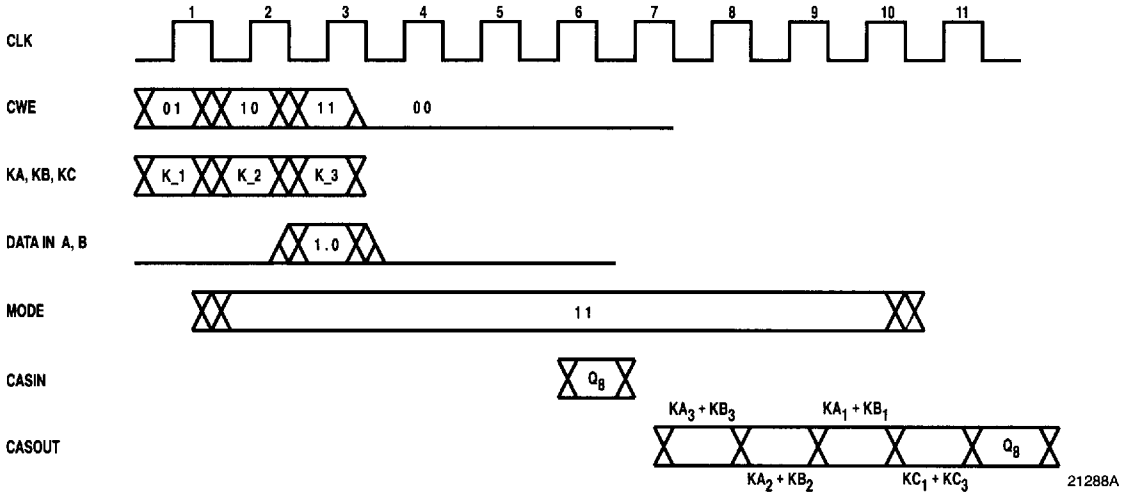
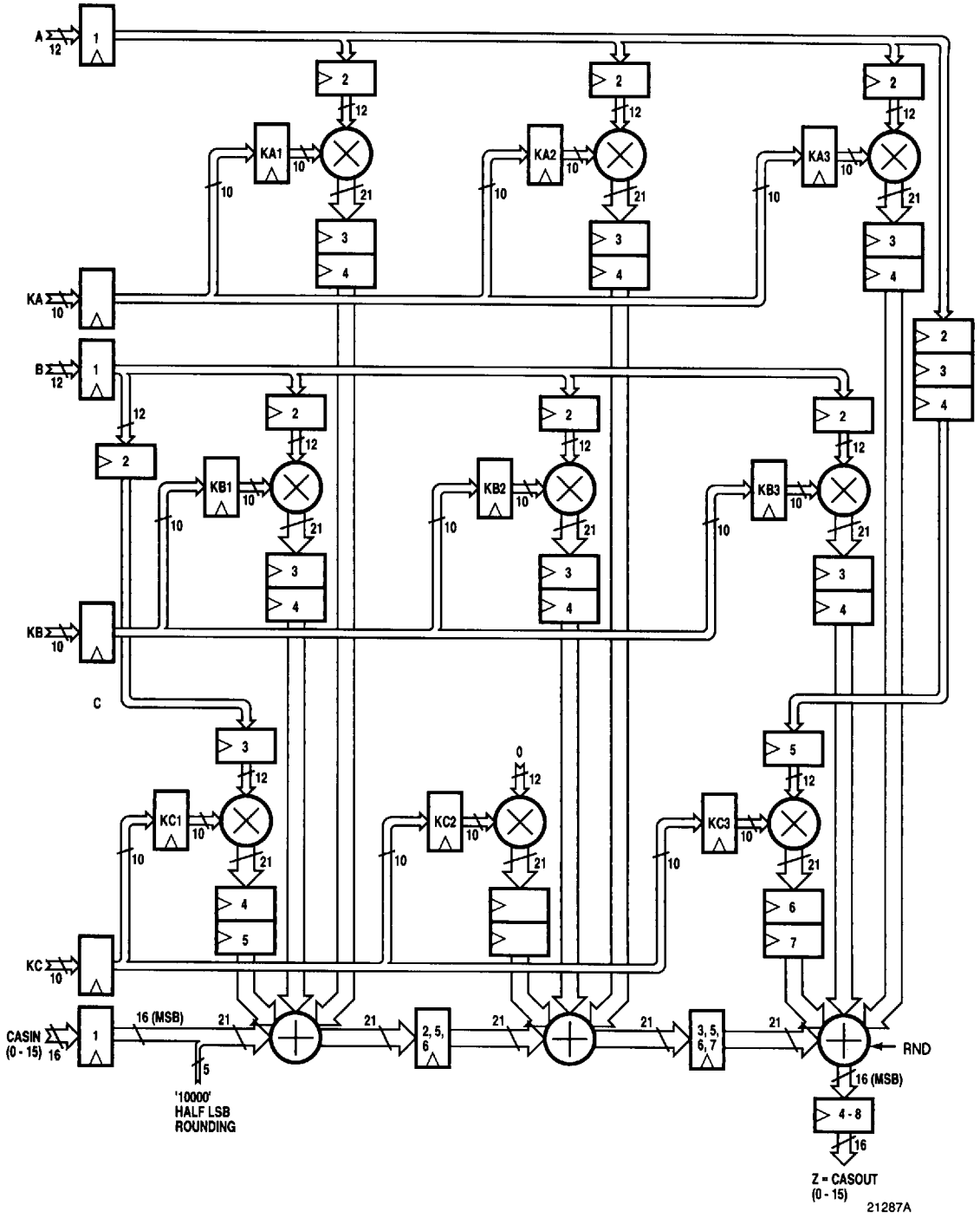


Figure 8. 4 x 2-Pixel Convolver Configuration (Mode 11)



Signal Definitions (cont.)

Controls

$MODE_{1,0}$ The TMC2250 will switch to the configuration selected by the user (as shown in *Table 3*) on the next clock. This registered control is usually static; however, should the user wish to switch between modes, the internal pipeline latencies of the device must be taken into account. Valid data will not be available at the outputs in the new configuration until enough clocks in the new mode have passed to flush the internal registers.

Table 3. Configuration Mode Word

$MODE_{1,0}$	Configuration Mode
00	3 x 3 Matrix Multiply
01	9-Tap One-Dimensional FIR
10	3 x 3-Pixel Convolver
11	4 x 2-Pixel Convolver

$CWE_{1,0}$ Data presented to the coefficient input ports (KA, KB, and KC) will update three of the internal coefficient storage registers, as indicated by the simultaneous Coefficient Write Enable select, on the next clock. See *Table 4* and the *Functional Block Diagram*.

Table 4. Coefficient Write Enable Word

$CWE_{1,0}$	Coefficient Set Selected
00	Hold all registers
01	Update KA1, KB1, KC1
10	Update KA2, KB2, KC2
11	Update KA3, KB3, KC3

Table 5. Coefficient Input Ports

Input Port	Registers Available
KA	KA1, KA2, KA3
KB	KB1, KB2, KB3
KC	KC1, KC2, KC3

Inputs And Outputs

A_{11-0}, B_{11-0}, C_{11-0} Data presented to the 10-bit registered data input ports A, B, and C are latched into the multiplier input registers for the currently selected configuration (*Table 3*). In all modes except Mode 00, new data are internally right-shifted to the next filter tap on each rising edge of CLK.

KA_{9-0}, KB_{9-0}, KC_{9-0} Data presented to the 10-bit registered coefficient input ports KA, KB, and KC are latched three at a time into the internal coefficient storage register set indicated by the Coefficient Write Enable $CWE_{1,0}$ on the next clock, as shown in *Table 4*.

$CASIN_{15-0}$ In all modes except Mode 00, the x port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Input port $CASIN_{15-0}$. Data presented to this input will be added to the weighted sums of the data words which were presented to the input ports (A, B, and C).

X_{11-0}, Y_{11-0}, Z_{11-0} In the matrix multiply mode, data are available at the 12-bit registered output ports X, Y, and Z t_{DO} after every clock. These ports are reconfigured in the filtering modes as 16-bit Cascade Input and Output ports.

NOTE: The output ports X, Y, Z and CASOUT, and the input port CASIN are internally reconfigured by the device as required for each mode of the device. The multiple-function pins have names which are combinations of these titles, as appropriate.

$CASOUT_{15-0}$ In all modes except Mode 00, the Z port and four bits of the Y output port are reconfigured as the 16-bit registered Cascade Output port $CASOUT_{15-0}$.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V_{DD}	Supply Voltage	F3, H3, L7, C8, C4
	GND	Ground	E3, G3, J3, L4, L6, H11, C7, C5
Clock	CLK	System Clock	D11
Controls	$MODE_{1,0}$	Mode Control	B5, A4
	$CWE_{1,0}$	Coefficient Write Enable	J12, J13
Input/Output	A_{11-0}	Data Input A	E11, D13, E12, E13, F11, F12, F13, G13, G11, G12, H13, H12
	B_{11-0}	Data Input B	B10, A11, B11, C10, A12, B12, C11, A13, C12, B13, C13, D12
	C_{11-0}	Data Input C	A5, C6, B6, A6, A7, B7, A8, B8, A9, B9, A10, C9
	KA_{9-0}	Coefficient Input A1, A2, A3	K13, J11, K12, L13, L12, K11, M13, M12, L11, N13
	KB_{9-0}	Coefficient Input B1, B2, B3	M11, L10, N12, N11, M10, L9, N10, M9, N9, L8
	KC_{9-0}	Coefficient Input C1, C2, C3	M8, N8, N7, M7, N6, M6, N5, M5, N4, L5
	XC_{11-0}	$CASIN_{15-4}$/Output X	B4, A3, A2, B3, A1, C3, B2, B1, D3, C2, C1, D2
	YC_{11-8}	$CASIN_{3-0}$/Output Y_{11-0}	D1, E2, E1, F2
	Y_{7-4}	Output Y_{7-4} Only	F1, G2, G1, H1
	YC_{3-0}	$CASOUT_{3-0}$/Output Y_{3-0}	K1, J2, J1, H2
	ZC_{11-0}	$CASOUT_{15-4}$/Output Z_{11-0}	M4, N3, M3, N2, M2, L3, N1, L2, K3, M1, L1, K2

Figure 9. Input/Output Timing Diagram

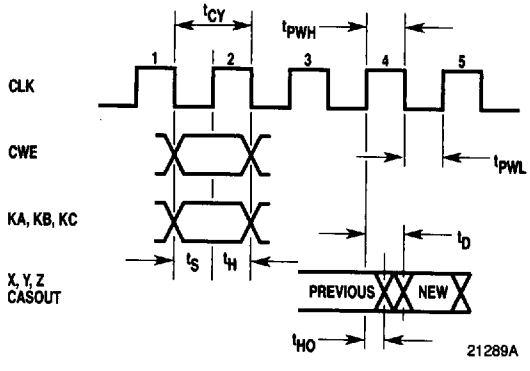


Figure 10. Equivalent Input Circuit

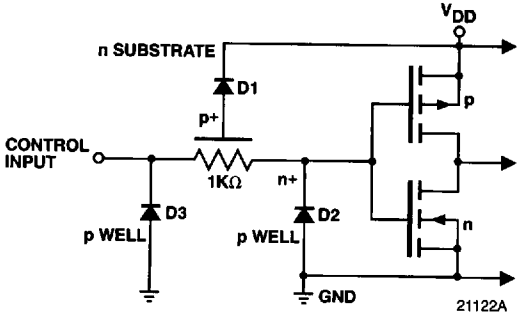
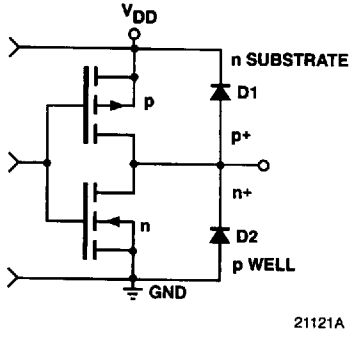


Figure 11. Equivalent Output Circuit



Absolute maximum ratings (beyond which the device may be damaged) [1]

Supply Voltage ..... −0.5 to +7.0V

Input Voltage ..... −0.5 to (V_{DD}+5.0)V

Output

Applied voltage ..... −0.5 to (V_{DD}+5.0)V [2]

Forced current ..... −6.0 to 6.0mA [3,4]

Short-circuit duration (single output in HIGH state to ground) ..... 1 Second

Temperature

Operating, case ..... −60 to +130°C

junction ..... 175°C

Lead, soldering (10 seconds) ..... 300°C

Storage ..... −65 to 150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating conditions

RAYTHEON/ SEMICONDUCTOR

Parameter		Temperature Range: Standard Min	Standard Nom	Standard Max	Extended Min	Extended Nom	Extended Max	Units
V_{DD}	Supply Voltage	4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW			0.8			0.8	V
	CLK Only			0.8			0.6	V
V_{IH}	Input Voltage, Logic HIGH	2.0			2.0			V
I_{OL}	Output Current, Logic LOW			4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH			−2.0			−2.0	mA
t_{CY}	Cycle Time							
	TMC2250	33			33			ns
	TMC2250-1	27.7			27.7			ns
	TMC2250-2	25						ns
t_{PWL}	Clock Pulse Width, LOW							
	TMC2250	15			15			ns
	TMC2250-1	12			12			ns
	TMC2250-2	10						ns
t_{PWH}	Clock Pulse Width, HIGH	10			10			ns
t_S	Input Setup Time							
	TMC2250	8			8			ns
	TMC2250-1	7			7			ns
	TMC2250-2	6						ns
t_H	Input Hold Time							
	TMC2250	3			3			ns
	TMC2250-1	3			3			ns
	TMC2250-2	2						ns
T_A	Ambient Temperature, Still Air	0		70				°C
T_C	Case Temperature				−55		125	°C

Electrical characteristics within specified operating conditions[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		12		12	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz		160		160	mA
I_{IL}	Input Current, Logic LOW [2]	V_{DD} = Max, V_{IN} = 0V		−10		−10	μA
I_{IH}	Input Current, Logic HIGH [2]	V_{DD} = Max, V_{IN} = V_{DD}		10		10	μA
I_{OIL}	Input Current, Logic LOW [3]	V_{DD} = Max, V_{IN} = 0V		−40		−40	μA
I_{OIH}	Input Current, Logic HIGH [3]	V_{DD} = Max, V_{IN} = V_{DD}		40		40	μA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = 4mA		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = −2mA	2.4		2.4		V
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to to ground, one second duration max.	−20	−80	−20	−80	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Notes:
1. Actual test conditions may vary from those shown, but guarantee operation as specified.
2. Except pins XC_{11-0}, YC_{11-8}.
3. Pins XC_{11-0}, YC_{11-8} only.

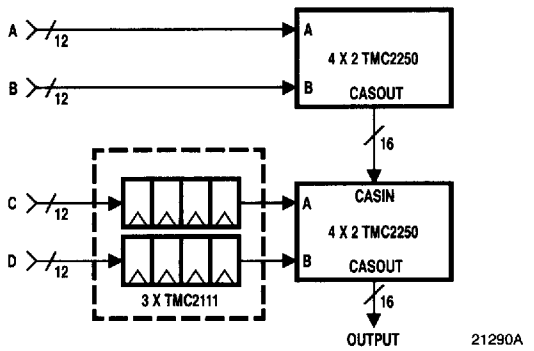
Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF					
	TMC2250			18		20	ns
	TMC2250-1			17		18	ns
	TMC2250-2			16			ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF					
	TMC2250		3		3		ns
	TMC2250-1		3		3		ns
	TMC2250-2		3		3		ns

Performing Large-Kernel Pixel Interpolation

The Cascade Input and Output Ports of the TMC2250 allow the user to stack multiple devices to perform larger interpolation kernels with no decrease in pixel throughput. *Figure 12* illustrates a basic application utilizing Mode 11 to realize a 4 x 4-pixel kernel, also called Cubic Convolution. This example utilizes the TMC2011 Variable-Length Shift Register to compensate for the internal latency of each TMC2250. Alternatively, some applications may utilize RAM, FIFOs, or other methods to store multiple-line pixel data. In these cases the user may compensate for latency by simply offsetting the access sequencing of the storage devices.

Figure 12. Performing Cubic Convolution with Two TMC2250s



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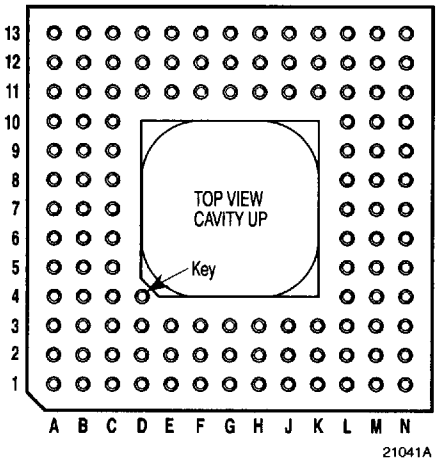
Pin Assignments — 121 Pin Plastic (H5) or Ceramic (G1) Pin Grid Array

Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
A1	XC_7	B3	XC_8	C5	GND	E1	YC_9	G11	A_3	K1	YC_3	L10	KB_8	M12	KA_2
A2	XC_9	B4	XC_{11}	C6	C_{10}	E2	YC_{10}	G12	A_2	K2	ZC_0	L11	KA_1	M13	KA_3
A3	XC_{10}	B5	$MODE_1$	C7	GND	E3	GND	G13	A_4	K3	ZC_3	L12	KA_5	N1	ZC_5
A4	$MODE_0$	B6	C_9	C8	V_{DD}	E11	A_{11}	H1	Y_4	K11	KA_4	L13	KA_6	N2	ZC_8
A5	C_{11}	B7	C_6	C9	C_0	E12	A_9	H2	YC_0	K12	KA_7	M1	ZC_2	N3	ZC_{10}
A6	C_8	B8	C_4	C10	B_8	E13	A_8	H3	V_{DD}	K13	KA_9	M2	ZC_7	N4	KC_1
A7	C_7	B9	C_2	C11	B_5	F1	Y_7	H11	GND	L1	ZC_1	M3	ZC_9	N5	KC_3
A8	C_5	B10	B_{11}	C12	B_3	F2	YC_8	H12	A_0	L2	ZC_4	M4	ZC_{11}	N6	KC_5
A9	C_3	B11	B_9	C13	B_1	F3	V_{DD}	H13	A_1	L3	ZC_6	M5	KC_2	N7	KC_7
A10	C_1	B12	B_6	D1	YC_{11}	F11	A_7	J1	YC_1	L4	GND	M6	KC_4	N8	KC_8
A11	B_{10}	B13	B_2	D2	XC_0	F12	A_6	J2	YC_2	L5	KC_0	M7	KC_6	N9	KB_1
A12	B_7	C1	XC_1	D3	XC_3	F13	A_5	J3	GND	L6	GND	M8	KC_9	N10	KB_3
A13	B_4	C2	XC_2	D11	CLK	G1	Y_5	J11	KA_8	L7	V_{DD}	M9	KB_2	N11	KB_6
B1	XC_4	C3	XC_6	D12	B_0	G2	Y_6	J12	CWE_1	L8	KB_0	M10	KB_5	N12	KB_7
B2	XC_5	C4	V_{DD}	D13	A_{10}	G3	GND	J13	CWE_0	L9	KB_4	M11	KB_9	N13	KA_0

D4 Index Pin (Unconnected)



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Ordering Information

Product Number	Speed (MHz)	Temperature Range	Screening	Package	Package Marking
TMC2250H5C	30	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C
TMC2250H5C 1	36	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C 1
TMC2250H5C 2	40	STD – T_A = 0°C to 70°C	Commercial	121 Pin Plastic Pin Grid Array	2250H5C 2
TMC2250G1V	30	MIL – T_C = –55°C to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V
TMC2250G1V1	36	MIL – T_C = –55°C to 125°C	MIL-STD-883	121 Pin Ceramic Pin Grid Array	2250G1V1