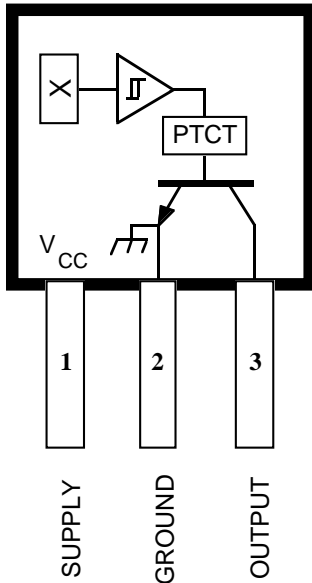


3150

PROGRAMMABLE, CHOPPER-STABILIZED, HALL-EFFECT SWITCH



Dwg. PH-003-2

PRELIMINARY INFORMATION
(subject to change without notice)
April 12, 1998

ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

Supply Voltage, V_{CC}	26.5 V
Reverse Supply Voltage, V_{RCC}	-30 V
Overvoltage Supply Current, I_{CC}	100 mA
Magnetic Flux Density, B	Unlimited
Output Current, I_{OUT}	Internally Limited
Output OFF Voltage, V_{OUT}	26.5 V
Reverse Output Current, I_{ROUT}	-50 mA
Operating Temperature Range, T_A	-40°C to +115°C
Storage Temperature, T_S	+170°C

The A3150JLT and A3150JUA programmable switches provide tooth/valley recognition in large gear-tooth sensing applications. Each sensor consists of a single element, chopper-stabilized Hall-effect IC that can be programmed to the desired magnetic switch point, optimizing sensor airgap and timing accuracy performance after final packaging. The small package can be easily assembled and used in conjunction with a wide variety of gear/target shapes and sizes. The two devices differ only in package style.

The sensing technology used for this sensor is Hall-effect based. The sensor incorporates a single-element Hall IC that switches in response to magnetic signals created by a ferrous target. The programmability of the circuit eliminates magnet and system offsets such as those caused by tilt yet provides zero-speed detection capabilities without the associated running jitter inherent in classical digital solutions.

A proprietary dynamic offset cancelation technique, with an internal high-frequency clock, reduces the residual offset voltage, which is normally caused by device overmolding, temperature dependencies, and thermal stress. This technique produces devices that have an extremely stable quiescent output voltage, are immune to mechanical stress, and have precise recoverability after temperature cycling. Many problems normally associated with low-level analog signals are minimized by having the Hall element and amplifier in a single chip. Output precision is obtained by internal gain adjustments during the manufacturing process and operate-point programming in the user's application.

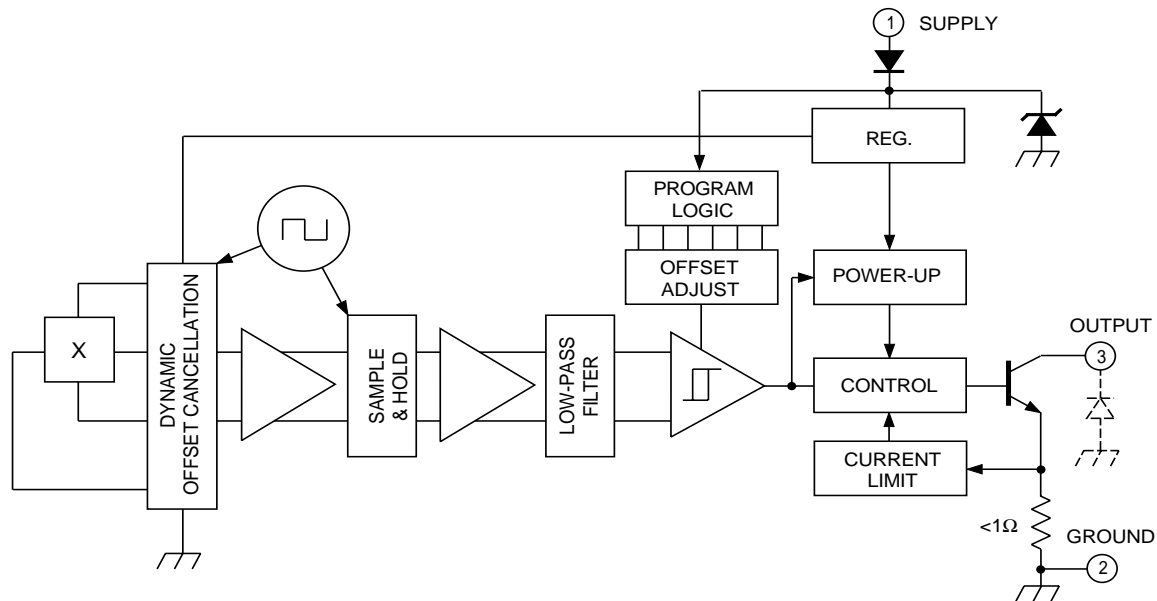
This sensor system is ideal for use in gathering speed, position, and timing information using gear-tooth-based configurations. The A3150JLT/JUA are particularly suited to those applications that require accurate duty cycle control or accurate edge detection. The lower vibration sensitivity also makes these devices extremely useful for transmission speed sensing.

Continued next page

Always order by complete part number: the prefix 'A' + the basic four-digit part number + a suffix to indicate operating temperature range + a suffix to indicate package style, e.g., **A3150JLT** .

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FUNCTIONAL BLOCK DIAGRAM



Dwg. FH-020-3

Two package styles provide a magnetically optimized package for most applications. Suffix '-LT' is a miniature SOT-89/TO-243AA transistor package for surface-mount applications; while suffix '-UA' is a three-lead ultra-mini-SIP for through-hole mounting.

FEATURES AND BENEFITS

- Chopper Stabilized for Extremely Low Switch-Point Drift and Immunity to Mechanical Stress
- Externally Programmed Switch Point
- On-Chip Supply-Transient Protection
- Output Short-Circuit Protection
- Single-Chip Sensing IC for High Reliability
- Small Mechanical Size
- <math><50\ \mu\text{s}</math> Power-On Time
- Wide Operating Voltage Range
- Defined Power-On State



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ELECTRICAL CHARACTERISTICS over operating voltage and temperature range (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage	V_{CC}	Operating, $T_J < 165^\circ\text{C}$	4.25	–	26	V
Power-On State	POS	After programming, $V_{CC} = 0 \rightarrow 5\text{ V}$	HIGH	HIGH	HIGH	–
Low Output Voltage	$V_{\text{OUT(SAT)}}$	$I_{\text{OUT}} = 20\text{ mA}$	–	175	400	mV
Output Current Limit	I_{OUTM}	$V_{\text{OUT}} = 12\text{ V}$	65	80	95	mA
Output Leakage Current	I_{OFF}	$V_{\text{OUT}} = 24\text{ V}$	–	0.2	10	μA
Supply Current	I_{CC}	Before programming, output OFF	–	4.0	7.0	mA
		Before programming, output ON	–	5.0	8.0	mA
Reverse Supply Current	I_{RCC}	$V_{RCC} = -30\text{ V}$	–	–	-5.0	mA
Power-On Delay	t_{on}	$V_{CC} > 5\text{ V}$	–	20	50	μs
Output Rise Time	t_r	$R_L = 820\ \Omega$, $C_L = 20\text{ pF}$	–	200	–	ns
Output Fall Time	t_f	$R_L = 820\ \Omega$, $C_L = 20\text{ pF}$	–	100	–	ns
Clock Frequency	f_C		–	340	–	kHz
Zener Voltage	V_Z	$I_{ZT} = 100\ \mu\text{A}$, $T_A = 25^\circ\text{C}$	27	32	–	V
Zener Impedance	z_Z	$I_{ZT} = 10\text{ mA}$, $T_A = 25^\circ\text{C}$	–	50	100	Ω

NOTE: Typical data is at $V_{CC} = 5\text{ V}$ and $T_A = +25^\circ\text{C}$ and is for design information only.

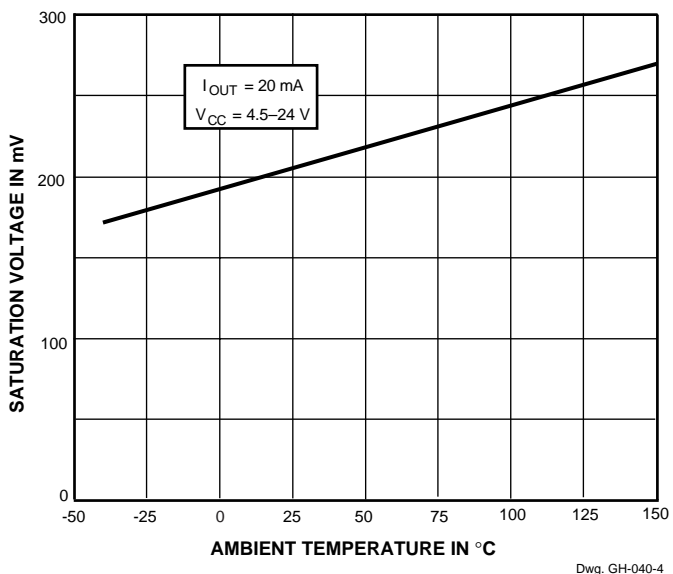
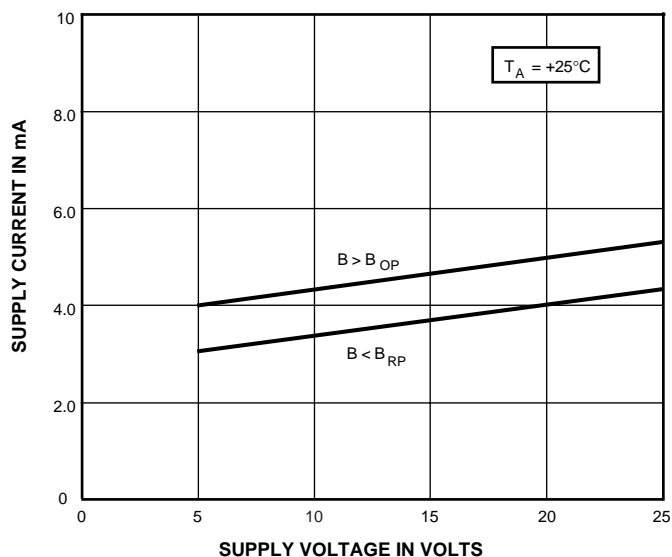
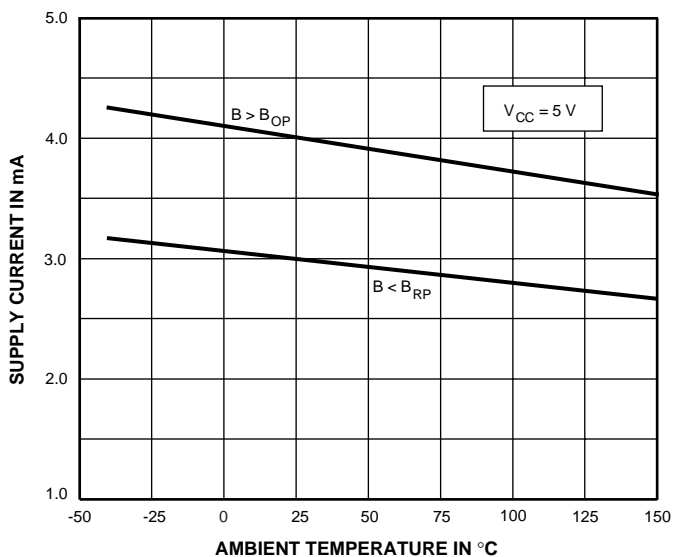
MAGNETIC CHARACTERISTICS over operating supply voltage and temperature ranges.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Point	B_{OP}	Programmable offset range	500	670	850	G
		Initial (before programming)	0	20	40	G
		Resolution	8.0	11	14	G
	ΔB_{OP}	$V_{CC} = 14\text{ V}$, after programming, $B_{\text{OP}} \approx 500\text{ G}$	-35	8.0	+35	G
Hysteresis	B_{hys}		5.0	20	35	G

NOTE: Typical data is at $V_{CC} = 5\text{ V}$ and $T_A = +25^\circ\text{C}$ and is for design information only.

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TYPICAL ELECTRICAL CHARACTERISTICS



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FUNCTIONAL DESCRIPTION

Chopper-Stabilized Technique. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique will also slightly degrade the device output repeatability.

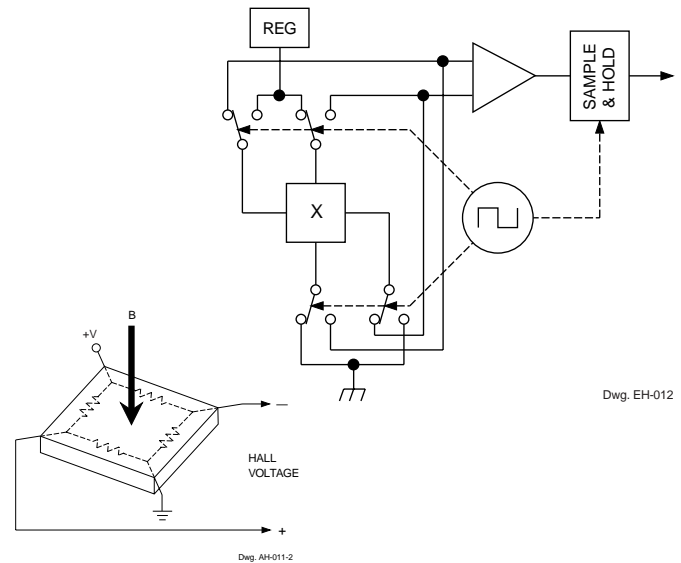
The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. The chopper-stabilizing technique cancels the mismatching of the resistors by changing the direction of the current flowing through the Hall plate and Hall voltage measurement taps, while maintaining the Hall-voltage signal that is induced by the external magnetic flux. The signal is, then, captured by a sample-and-hold circuit.

Operation. The output of these devices switches low (turns ON) when a magnetic field (south pole) perpendicular to the Hall sensor exceeds the operate point threshold (B_{OP}). After turn-ON, the output is capable of sinking 25 mA and the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced below the release point (B_{RP}), the device output goes high (turns OFF). The difference in the magnetic operate and release points is the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

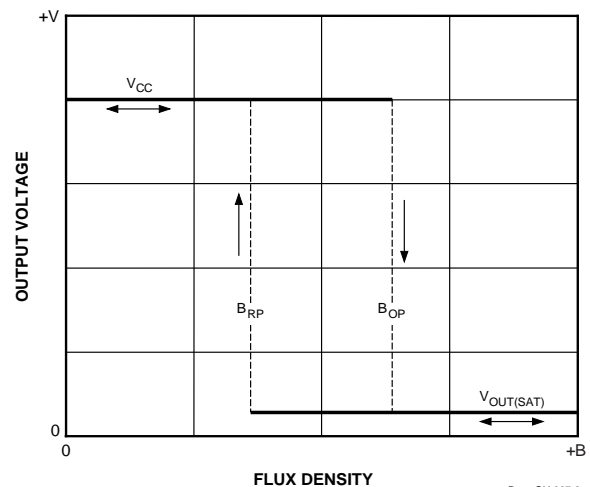
Applications. It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall sensor) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique.

The simplest form of magnet that will operate these devices is a bar magnet with the south-seeking pole towards the branded surface of the device. Many other methods of operation are possible. Extensive applications information on magnets and Hall-effect sensors is also available in the *Allegro Electronic Data Book AMS-702* or *Application Note 27701*, or

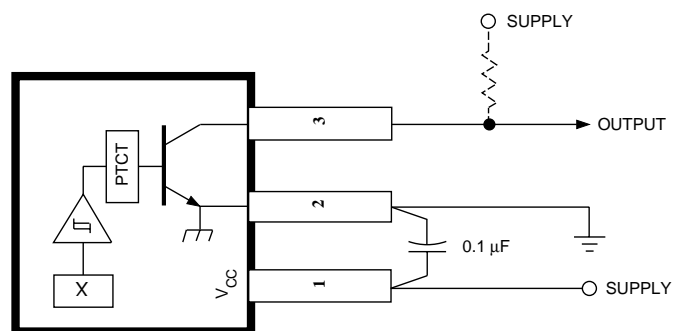
www.allegromicro.com



Dwg. EH-012



Dwg. GH-007-2



Dwg. EH-013

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PROGRAMMING PROTOCOL

The A3150JLT and A3150JUA operate points are programmed by serially addressing the device through the supply terminal (pin1). After the correct operate point is determined, the device programming bits are selected and then a “lock” set to prevent any further (accidental) programming.

Program Enable. To program the device, a sequence of pulses is used to activate/enable the addressing mode as shown in figure 1. This sequence of a V_{PP} pulse, at least seven V_{PH} pulses, and a V_{PP} pulse with no supply interruptions, is designed to prevent the device from being programmed accidentally (for example, as a result of noise on the supply line).

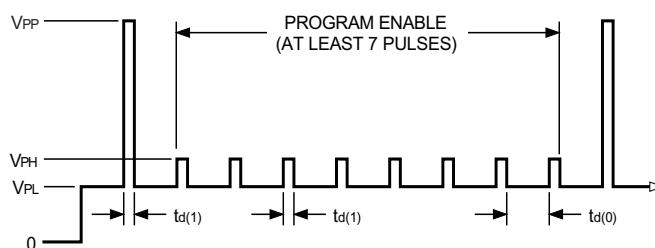


Figure 1 — Program enable

Dwg. WH-013

PROGRAMMING PROTOCOL over operating temperature range.

Characteristic	Symbol	Description	Limits			
			Min.	Typ.	Max.	Units
Programming Voltage	V_{PL}	Minimum voltage during programming	4.5	5.0	5.5	V
	V_{PH}		9.0	10	11	V
	V_{PP}		20	23	25	V
Programming Current	I_{PP}	Max. supply current during programming	–	250	–	mA
Pulse Width	$t_{d(0)}$	OFF time between bits	20	–	–	μ s
	$t_{d(1)}$	Enable, address, program, or lock bit ON time	20	–	–	μ s
	t_{dP}	Program pulse ON time	100	300	–	μ s
Pulse Rise Time	t_r	V_{PL} to V_{PH} or V_{PP}	11	–	–	μ s
Pulse Fall Time	t_f	V_{PH} or V_{PP} to V_{PL}	5.0	–	–	μ s

NOTE: Typical data is at $T_A = +25^\circ\text{C}$ and is for design information only.

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Address Determination. The operate point is adjustable in 64 increments. With the appropriate target or gear* in position, the 64 switch points are sequentially selected (figure 2) until the required operate point is reached. Note that the difference between the operate point and the release point (hysteresis) is a constant for all addresses.

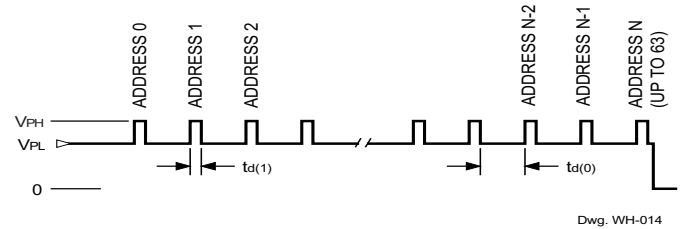


Figure 2 — Address determination

Set-Point Programming. After the desired set-point address is determined (0 through 63), each bit of the equivalent binary address is programmed individually. For example, as illustrated in figure 3, to program address code 5 (binary 000101), bits 1 and 3 need to be programmed. Each bit is programmed during the wide V_{PP} pulse and is not reversible.

Lock Programming. After the desired set point is programmed, the program lock is then activated (figure 4) to prevent further programming of the device.

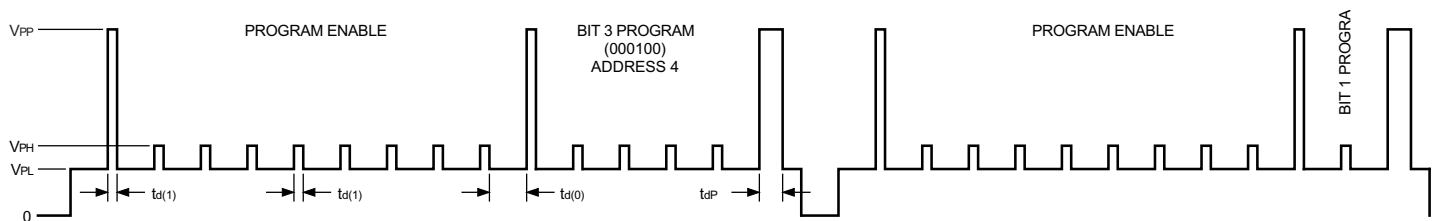


Figure 3 — Set-point programming

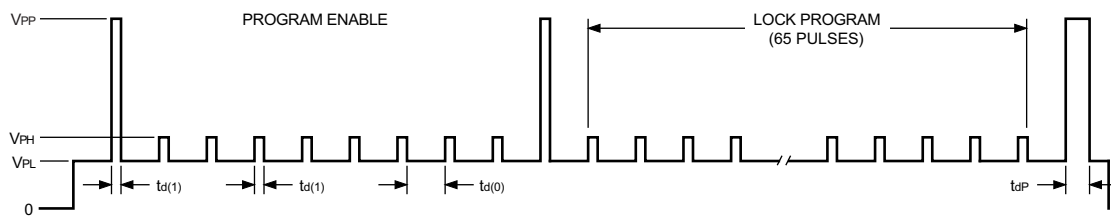


Figure 4 — Lock programming

* In application, the terms “gear” and “target” are often interchanged. However, “gear” is preferred when motion is transferred.

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CRITERIA FOR DEVICE QUALIFICATION

All Allegro sensors are subjected to stringent qualification requirements prior to being released to production. To become qualified, except for the destructive ESD tests, no failures are permitted.

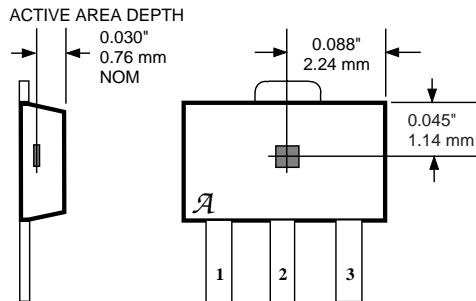
Qualification Test	Test Method and Test Conditions	Test Length	Samples	Comments
Biased Humidity (HAST)	$T_A = 130^{\circ}\text{C}$, RH = 85%	50 hrs	77	$V_{CC} = V_{OUT} = 5\text{ V}$
High-Temperature Operating Life (HTOL)	JESD22-A108, $T_A = 150^{\circ}\text{C}$, $T_J = 165^{\circ}\text{C}$	408 hrs	77	$V_{CC} = 24\text{ V}$, $V_{OUT} = 20\text{ V}$
Accelerated HTOL	JESD22-A108, $T_A = 175^{\circ}\text{C}$, $T_J = 190^{\circ}\text{C}$	504 hrs	77	$V_{CC} = 24\text{ V}$, $V_{OUT} = 20\text{ V}$
Autoclave, Unbiased	JESD22-A102, Condition C, $T_A = 121^{\circ}\text{C}$, 15 psig	96 hrs	77	
High-Temperature (Bake) Storage Life	MIL-STD-883, Method 1008, $T_A = 170^{\circ}\text{C}$	1000 hrs	77	
Temperature Cycle	MIL-STD-883, Method 1010, -65°C to $+150^{\circ}\text{C}$	500 cycles	77	
Latch-Up	—	Pre/Post Reading	6	
Electro-Thermally Induced Gate Leakage	—	Pre/Post Reading	6	
ESD, Human Body Model	CDF-AEC-Q100-002	Pre/Post Reading	x per test	Test to failure, All leads > TBD
Electrical Distributions	Per Specification	—	30	



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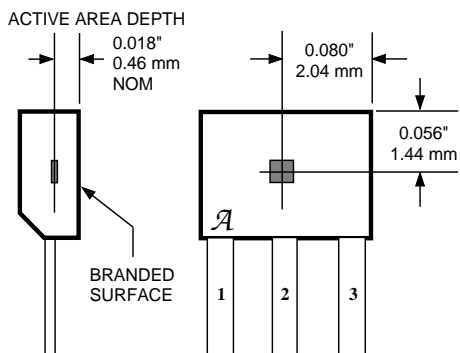
SENSOR LOCATIONS
(± 0.005 " [0.13 mm] die placement)

Package Designator "LT"



Dwg. MH-008-8

Package Designators "UA" and "UA-TL"



Dwg. MH-011-9A

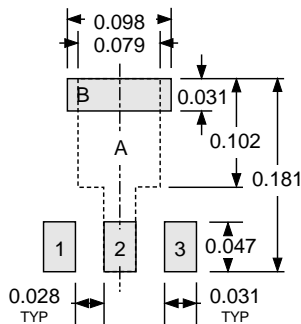
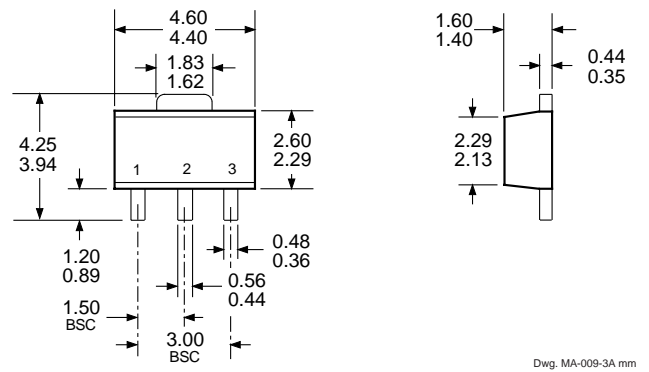
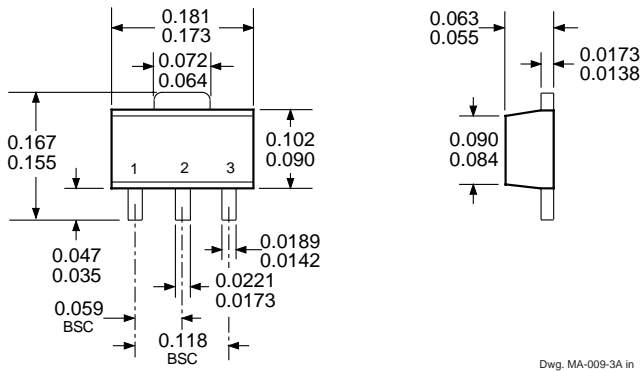
Although sensor location is accurate to three sigma for a particular design, product improvements may result in small changes to sensor location.

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PACKAGE DESIGNATOR 'LT' (SOT-89/TO-243AA)

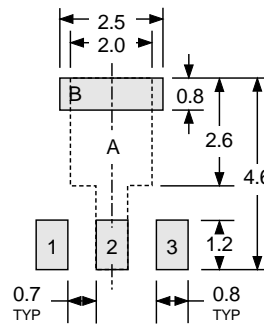
Dimensions in Inches
(for reference only)

Dimensions in Millimeters
(controlling dimensions)



pads 1, 2, 3, and A — Standard SOT-89 Layout
pads 1, 2, 3, and B — Low-Stress Version
pads 1, 2, and 3 only — Lowest Stress, But Not Self Aligning

Dwg. MA-012-3 in



Pads 1, 2, 3, and A — Standard SOT-89 Layout
Pads 1, 2, 3, and B — Low-Stress Version
Pads 1, 2, and 3 only — Lowest Stress, But Not Self Aligning

Dwg. MA-012-3 mm

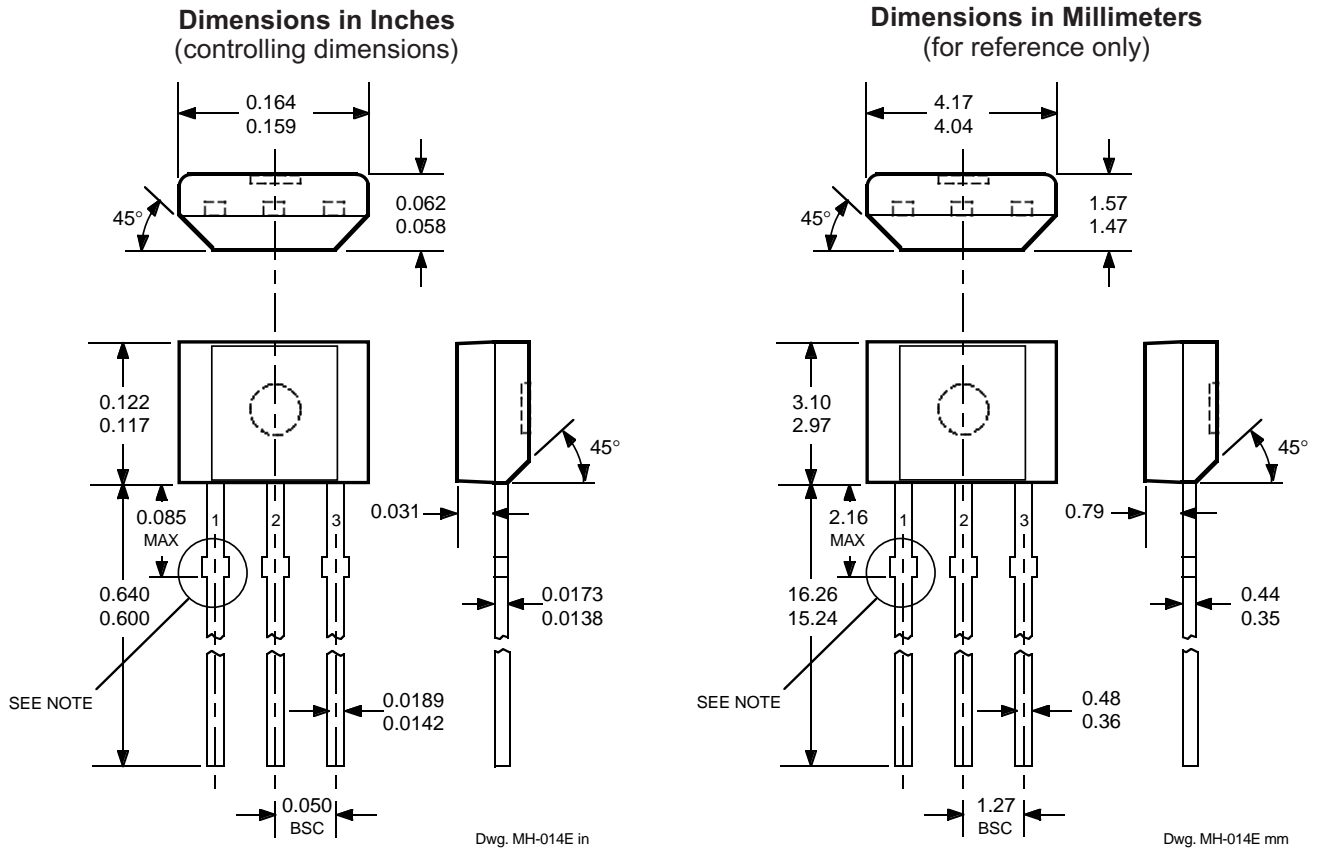
NOTE: Exact body and lead configuration at vendor's option within limits shown.



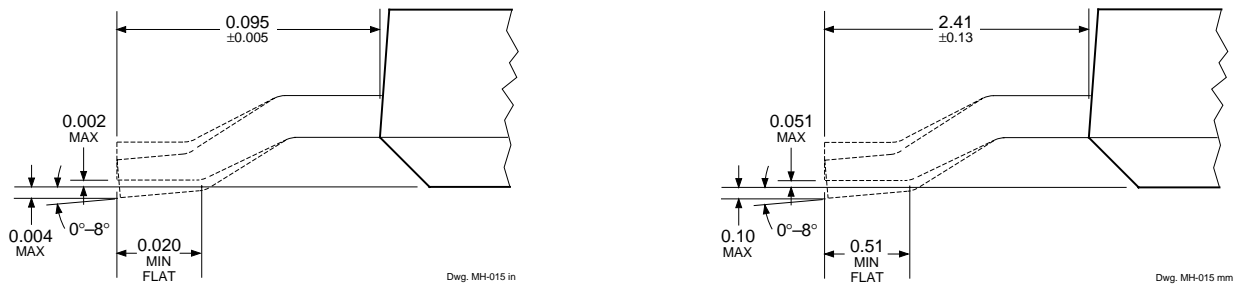
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000

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PACKAGE DESIGNATOR 'UA'



Surface-Mount Lead Form (Suffix '-TL')



- NOTES: 1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.

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The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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