

# DATA SHEET

## **74LVC2G06**

**Inverters with open-drain outputs**

Product specification  
Supersedes data of 2003 Aug 25

2004 Sep 10

## Inverters with open-drain outputs

## 74LVC2G06

## FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- –24 mA output drive ( $V_{CC} = 3.0$  V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- Multiple package options
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

## DESCRIPTION

The 74LVC2G06 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant for slower input rise and fall time.

This device is fully specified for partial power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G06 provides two inverting buffers.

The output of this device is an open drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PLZ}/t_{PZL}$	propagation delay input nA to output nY	$V_{CC} = 1.8$ V; $C_L = 30$ pF; $R_L = 1$ k $\Omega$	3.2	ns
		$V_{CC} = 2.5$ V; $C_L = 30$ pF; $R_L = 500$ $\Omega$	2.0	ns
		$V_{CC} = 2.7$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.6	ns
		$V_{CC} = 3.3$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	2.3	ns
		$V_{CC} = 5.0$ V; $C_L = 50$ pF; $R_L = 500$ $\Omega$	1.6	ns
$C_I$	input capacitance		2.5	pF
$C_{PD}$	power dissipation capacitance per gate	$V_{CC} = 3.3$ V; notes 1 and 2	5.9	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = total load switching outputs;

$\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

2. The condition is  $V_I = \text{GND}$  to  $V_{CC}$ .

# Inverters with open-drain outputs

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## FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	nY
L	Z
H	L

### Note

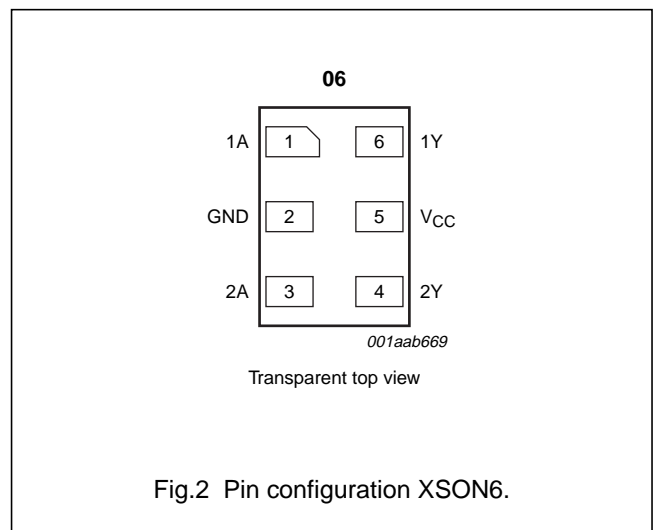
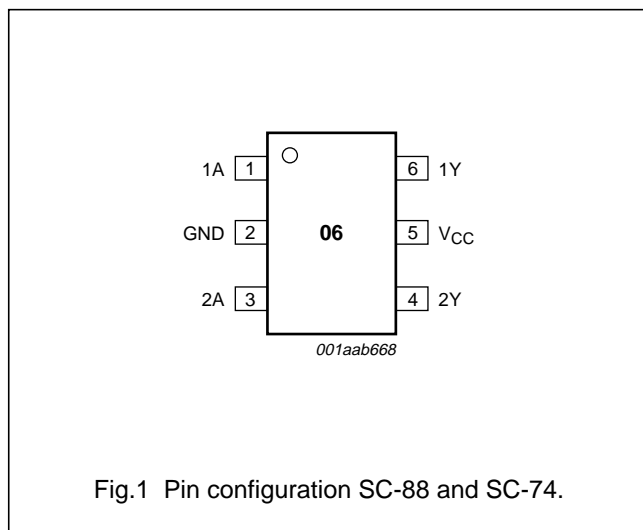
- 1. H = HIGH voltage level;
- L = LOW voltage level;
- Z = high-impedance OFF-state.

## ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2G06GW	-40 °C to +125 °C	6	SC-88	plastic	SOT363	V6
74LVC2G06GV	-40 °C to +125 °C	6	SC-74	plastic	SOT457	V06
74LVC2G06GM	-40 °C to +125 °C	6	XSON6	plastic	SOT886	V6

## PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	GND	ground (0 V)
3	2A	data input
4	2Y	data output
5	V <sub>CC</sub>	supply voltage
6	1Y	data output



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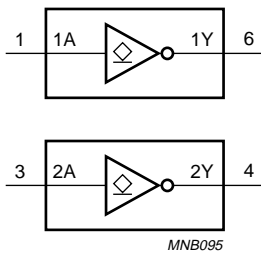


Fig.3 Logic symbol.

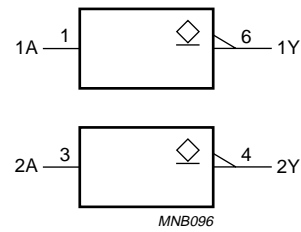


Fig.4 IEEE/IEC logic symbol.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		1.65	5.5	V
$V_I$	input voltage		0	5.5	V
$V_O$	output voltage	active mode	0	$V_{CC}$	V
		$V_{CC} = 0$ V; Power-down mode	0	5.5	V
$T_{amb}$	operating ambient temperature		-40	+125	°C
$t_r, t_f$	input rise and fall times	$V_{CC} = 1.65$ V to 2.7 V	0	20	ns/V
		$V_{CC} = 2.7$ V to 5.5 V	0	10	ns/V

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**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input diode current	$V_I < 0$ V	-	-50	mA
$V_I$	input voltage	note 1	-0.5	+6.5	V
$I_{OK}$	output diode current	$V_O < 0$ V	-	-50	mA
$V_O$	output voltage	active mode; notes 1 and 2	-0.5	6.5	V
		Power-down mode; notes 1 and 2	-0.5	+6.5	V
$I_O$	output source or sink current	$V_O = 0$ V to 6.5 V	-	50	mA
$I_{CC}, I_{GND}$	$V_{CC}$ or GND current		-	$\pm 100$	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	power dissipation	$T_{amb} = -40$ °C to +125 °C	-	300	mW

**Notes**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When  $V_{CC} = 0$  V (Power-down mode), the output voltage can be 5.5 V in normal operation.

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**DC CHARACTERISTICS**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C; note 1</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.45	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.3	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.4	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.55	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.55	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	1.65 to 5.5	–	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	±0.1	±10	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	±0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	0.1	10	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A	2.3 to 5.5	–	5	500	μA

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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		1.65 to 1.95	0.65 × V <sub>CC</sub>	–	–	V
			2.3 to 2.7	1.7	–	–	V
			2.7 to 3.6	2.0	–	–	V
			4.5 to 5.5	0.7 × V <sub>CC</sub>	–	–	V
V <sub>IL</sub>	LOW-level input voltage		1.65 to 1.95	–	–	0.35 × V <sub>CC</sub>	V
			2.3 to 2.7	–	–	0.7	V
			2.7 to 3.6	–	–	0.8	V
			4.5 to 5.5	–	–	0.3 × V <sub>CC</sub>	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	1.65 to 5.5	–	–	0.1	V
		I <sub>O</sub> = 4 mA	1.65	–	–	0.70	V
		I <sub>O</sub> = 8 mA	2.3	–	–	0.45	V
		I <sub>O</sub> = 12 mA	2.7	–	–	0.60	V
		I <sub>O</sub> = 24 mA	3.0	–	–	0.80	V
		I <sub>O</sub> = 32 mA	4.5	–	–	0.80	V
I <sub>LI</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	1.65 to 5.5	–	–	±20	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	–	–	±10	μA
I <sub>off</sub>	power OFF leakage current	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	–	–	±20	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	5.5	–	–	40	μA
ΔI <sub>CC</sub>	additional quiescent supply current per pin	V <sub>I</sub> = V <sub>CC</sub> – 0.6 V; I <sub>O</sub> = 0 A	2.3 to 5.5	–	–	5000	μA

**Note**

1. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

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AC CHARACTERISTICS

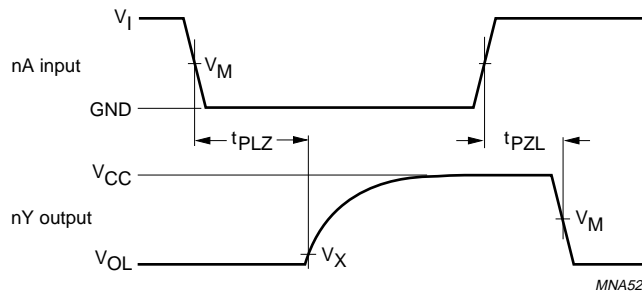
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C; note 1</b>							
t <sub>PLZ</sub> /t <sub>PZL</sub>	propagation delay input nA to output nY	see Figs 5 and 6	1.65 to 1.95	1.0	3.2	6.5	ns
			2.3 to 2.7	0.5	2.0	3.9	ns
			2.7	1.0	2.6	4.2	ns
			3.0 to 3.6	0.5	2.3	3.4	ns
			4.5 to 5.5	0.5	1.6	2.9	ns
<b>T<sub>amb</sub> = -40 °C to +125 °C</b>							
t <sub>PLZ</sub> /t <sub>PZL</sub>	propagation delay input nA to output nY	see Figs 5 and 6	1.65 to 1.95	1.0	-	8.2	ns
			2.3 to 2.7	0.5	-	4.9	ns
			2.7	1.0	-	5.3	ns
			3.0 to 3.6	0.5	-	4.3	ns
			4.5 to 5.5	0.5	-	3.7	ns

Note

1. All typical values are measured at T<sub>amb</sub> = 25 °C and at V<sub>CC</sub> = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	V <sub>X</sub>	INPUT	
			V <sub>I</sub>	t <sub>r</sub> = t <sub>f</sub>
1.65 V to 1.95 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>CC</sub>	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>CC</sub>	≤ 2.0 ns
2.7 V	1.5 V	V <sub>OL</sub> + 0.3 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	V <sub>OL</sub> + 0.3 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.3 V	V <sub>CC</sub>	≤ 2.5 ns

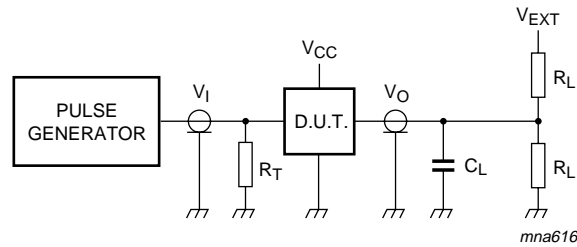
V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 The input (nA) to output (nY) propagation delays.



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$V_{CC}$	$V_I$	$C_L$	$R_L$	$V_{EXT}$
				$t_{pZL}/t_{pLZ}$
1.65 V to 1.95 V	$V_{CC}$	30 pF	1 k $\Omega$	$2 \times V_{CC}$
2.3 V to 2.7 V	$V_{CC}$	30 pF	500 $\Omega$	$2 \times V_{CC}$
2.7 V	2.7 V	50 pF	500 $\Omega$	6 V
3.0 V to 3.6 V	2.7 V	50 pF	500 $\Omega$	6 V
4.5 V to 5.5 V	$V_{CC}$	50 pF	500 $\Omega$	$2 \times V_{CC}$

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig.6 Load circuitry for switching times.

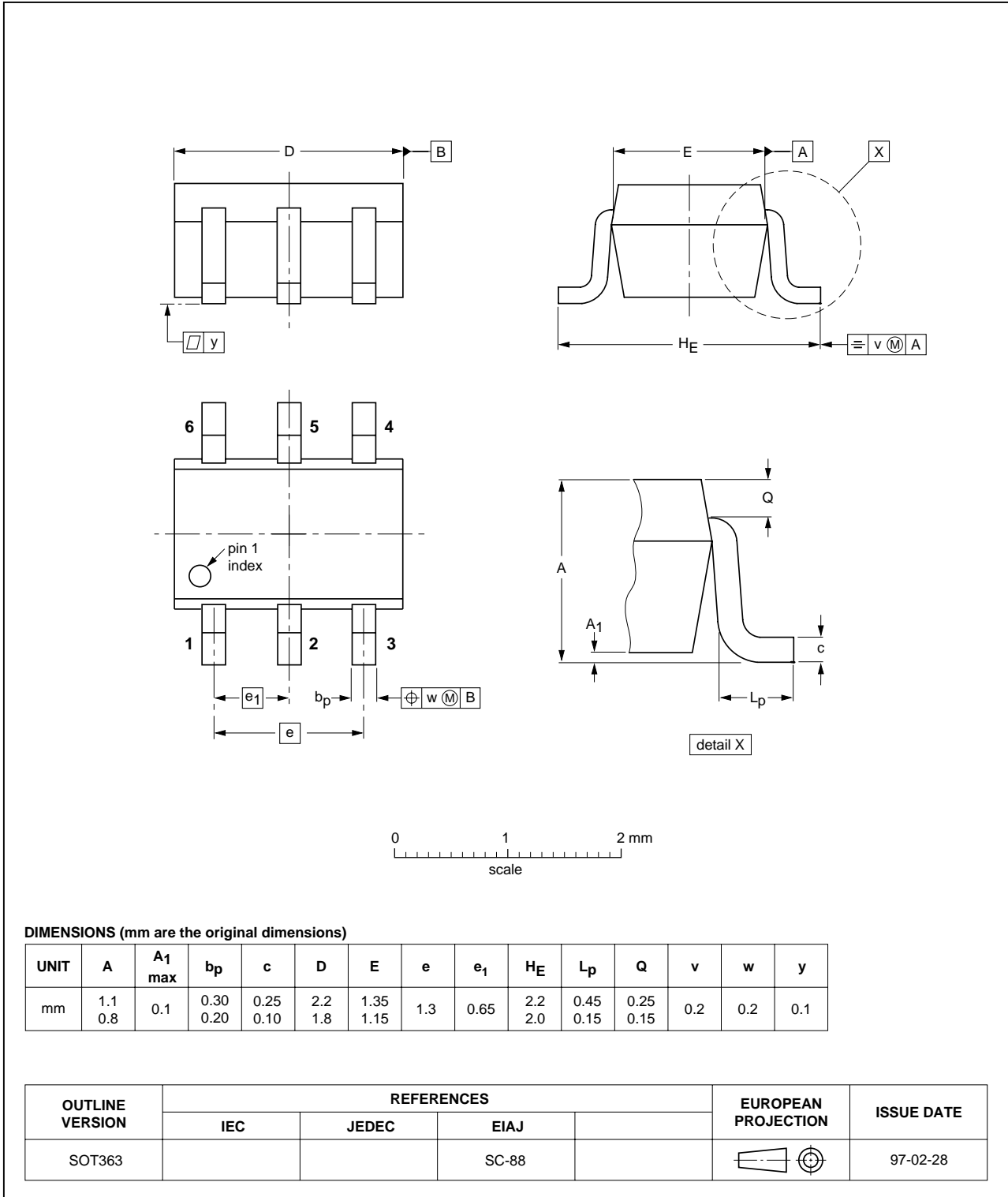
Inverters with open-drain outputs

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PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT363

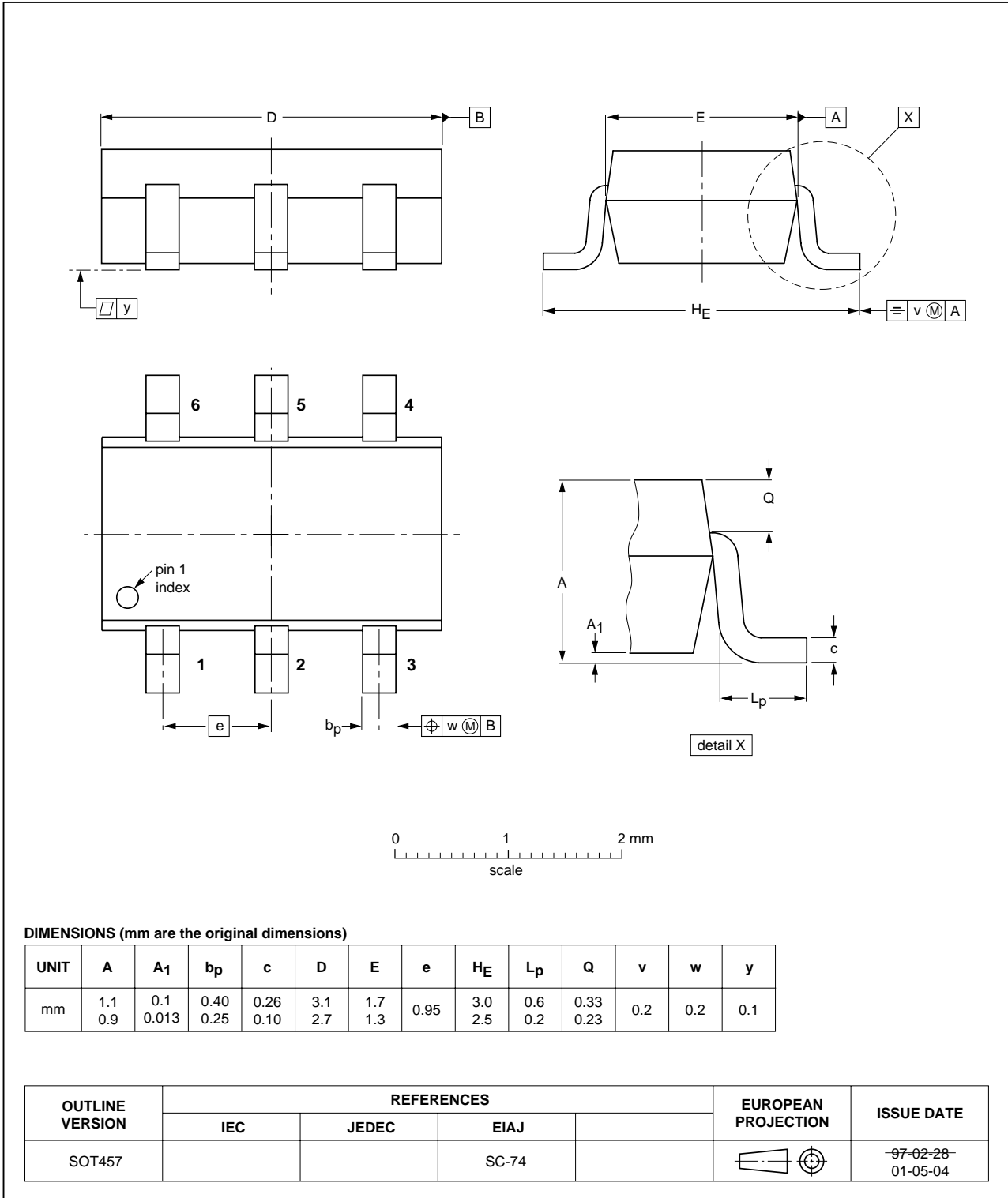


Inverters with open-drain outputs

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Plastic surface mounted package; 6 leads

SOT457

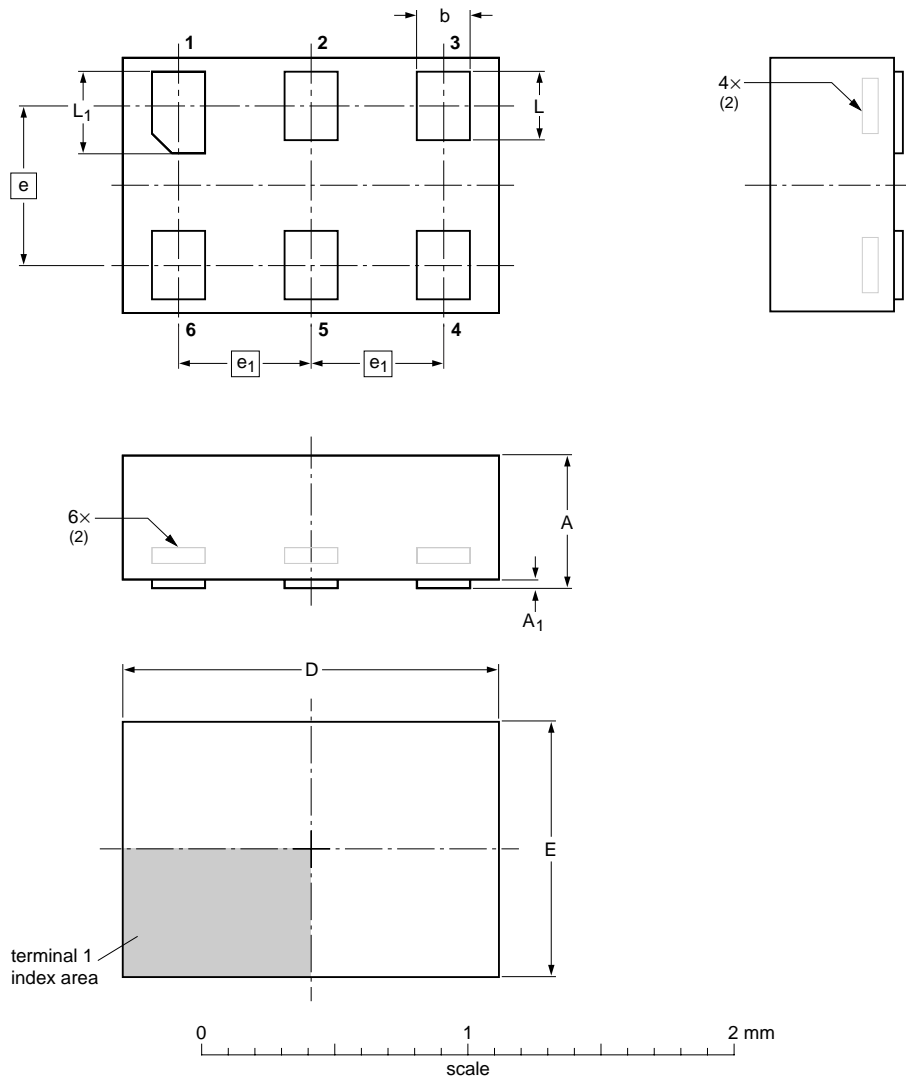


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XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



**DIMENSIONS (mm are the original dimensions)**

UNIT	A <sup>(1)</sup> max	A <sub>1</sub> max	b	D	E	e	e <sub>1</sub>	L	L <sub>1</sub>
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT886		MO-252			04-07-15 04-07-22

## Inverters with open-drain outputs

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## DATA SHEET STATUS

LEVEL	DATA SHEET STATUS <sup>(1)</sup>	PRODUCT STATUS <sup>(2)(3)</sup>	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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