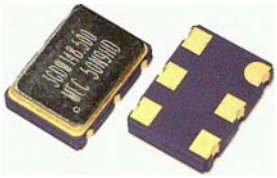
GD	LVDS Differential	F group 0.5 ps	W group 4.0 ps	Thru-Hole	SMD	3.3V	Min. 750KHz	Max. 800MHz

Applications

- GDF and GDW uses a high-Q fundamental crystal and a low jitter multiplier circuit.
- GDF offers < 1 ps phase jitter at only a fraction of the cost of a high frequency fundamental crystal VCXO. GDW series has moderate jitter at a low cost.



RoHS Compliance

General specifications of GDF and GDW only , at Ta=+25°C , CL=15pF

Model			" **GDF** " series			" **GDW** " series	
Technology			High Q fundamental crystal + low jitter multiplier circuit			High Q fundamental crystal + multiplier circuit	
Output Logic			LVDS				
Available Frequency Range			38.0 MHz ~ 640.0 MHz			750 KHz ~ 800.0 MHz	
Supply Voltage V_{DD}			+3.3 V_{DD} ± 5%			+3.3 V_{DD} ± 5%	
Supply Voltage Code			***" 3 "***			***" 3 "***	
Output Logic " High " , " 1 "			1.4 V typical ; 1.6 V max.				
Output Logic " Low " , " 0 "			0.9 V min. ; 1.1 V typical.				
Differential Output Voltage, V_{OD}			247 mV min.; 355 mV typical ; 454 mV max. Output 1 - output 2				
Differential Output Error, V_{OD}			-50 mV min ; 50 mV max.				
Output Offset Voltage, Vos			1.125 V min. ; 1.200 V typical ; 1.375 V max.				
Offset Magnitude Error (△Vos)			0 mV min. ; 3 mV typical ; 25 m V max.				
Integrated Phase Jitter (12 KHz to 20 MHz)			0.4 ps typical; 0.5 ps max. [for 156.250 MHz]			2.6 ps typical; 4 ps max. [for 155.520 MHz]	
Period Jitter (RMS ; Decoupling capacitor between V_{DD} and ground)			3.0 ps typical; 5 ps max. [for 156.250 MHz]			4.3 ps typical. [for 155.520 MHz]	
Period Jitter(peak-to-peak ;Decoupling capacitor between V_{DD} and ground)			20 ps typical; 30 ps max. [for 156.250 MHz]			27 ps typical. [for 155.520 MHz]	
Current Consumption (15 pF load)			38 MHz ~ 100 MHz - - - - - - - - - 65 mA max 100.01 MHz ~ 320 MHz - - - - - - - 80 mA max. 320.01 MHz ~ 640 MHz - - - - - - 90 mA max.			< 24 MHz - - - - - - - - - - - - - - - - 25 mA max 24.01 MHz ~ 96 MHz - - - - - - - - 65 mA max 96.01 MHz ~ 800 MHz - - - - - - - 100 mA max..	
Rise Time / Fall Time			0.7 ns typical , 1.0 ns max. (20%↔80% of the LVDS wave form)			1.5 ns max. (20%↔80% of the LVDS wave form)	
Frequency Stability [1] Codes		Frequency Stability over Operating Temperature Range	± 25 ppm	± 50 ppm	± 100 ppm	If non-standard , please enter the desired stability after the " C " or " I " . For example : " C20 " : ± 20 ppm over -10°C to +70°C " I20 " : ± 20 ppm over -40°C to +85°C	
		Commercial "C" (*-10°C ~ +70°C*)	*A*	*B*	*C*		
		Industrial " I " (*-40°C to +85°C*)	*D*	*E*	*F*		
Load			50 Ω from each output				
Start-up Time			5 m sec. typical; 10 m sec. max.				
Duty Cycle			50% ± 5% (measured at 1.25V)				
Drive Capability			100 ohms between LVDS output and complimentary LVDS output.				
Aging at Ta = +25°C			± 3 ppm max. first year ; ± 2 ppm max. per year thereafter				
Pad 1 Voltage Control Characteristics	Control Voltage Center , Range		+ 1.65 V , Vcon =+0.3V to +3.0V				
	Frequency Deviation Range		±80 ppm (min.) . Use " N " (minimum) , " M " (maxiimum) , " T " (typical,±20%) for the desired range . Example : " 100N " represents ±100ppm (min.) .				
	Linearity		6% typical ; 10% max.				
	Slope Polarity		Positive : Positive voltage for positive frequency shift				
	Modulation Bandwidth		25 KHz min. (-3dB , 0V ≤ Vcontrol ≤ 3.3V)				
	Input Impedance		60 KΩ min.			2 MΩ min.	
Tri - State Function. on pad No. 2	No Connection		Differential LVDS and compliantary LVDS outputs .				
	Disable		Both outputs are disabled (high impedance) when pad No.2 is taken below 0.45*Vcc referenced to ground (threshold) Oscillator is always On . Only buffer stage is disabled . Disable current : 50 uA max. (at 0.0V) , Disable time : 10 ns (max.)				
	Enable		At disabled mode , both outputs are enabled when Tri-state pad is taken above 0.45*Vcc referenced to ground (threshold) ; Enable time : 10ns + one period of the output frequency (max.)				
Phase Noise : Tested with Vcontrol pin connected to ground (typical)		Offset	Frequency: 156.250 MHz			Frequency: 155.520 MHz	
		10 Hz	-62 dBc / Hz			-60 dBc / Hz	
		100 Hz	-92 dBc / Hz			-90 dBc / Hz	
		1 KHz	-120 dBc / Hz			-115 dBc / Hz	
		10 KHz	-132 dBc / Hz			-125 dBc / Hz	
		100 KHz	-128 dBc / Hz			-119 dBc / Hz	
		1 MHz	-140 dBc / Hz			-120 dBc / Hz	
		10 MHz	-150 dBc / Hz			-140 dBc / Hz	

[1] Inclusive of 25ºC tolerance, operating temperature range, ±10% input voltage variation, load change, aging shock and vibration

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GP_ [LVPECL Differential output]

GD_ [LVDS Differential output]

Part Number Format and Example

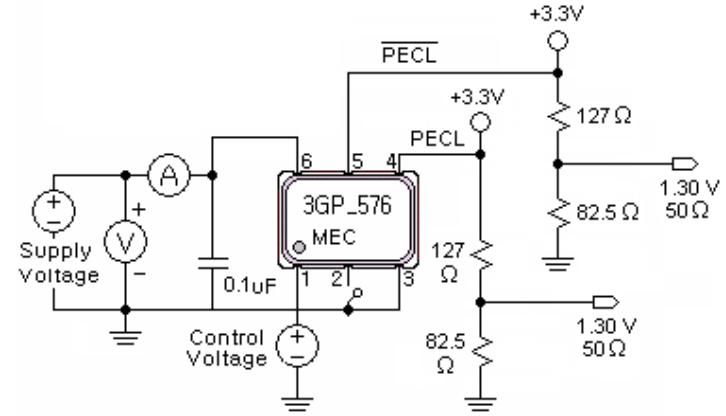
	[1]	[2]	[3]	[4]		[5]	[6]		[7]
	Supply Voltage	Holder Type Output Wave	G	Frequency Stability	–	Pulling Range	Range Code	–	Center Frequency
Examples	(1)	5	GPF14	G	B	–	100	N	–	35.328
	(2)	3	GV576		D	–	80	T	–	27.000

Ex (1) : 3GPF14GB - 100N - 155.520 [+3.3V , G_ 14 type (F characteristics , PECL output) , RoHS , ±50ppm(-10°C to 70°C) , pulling : ±100 ppm (min.) , 155.520 MHz]

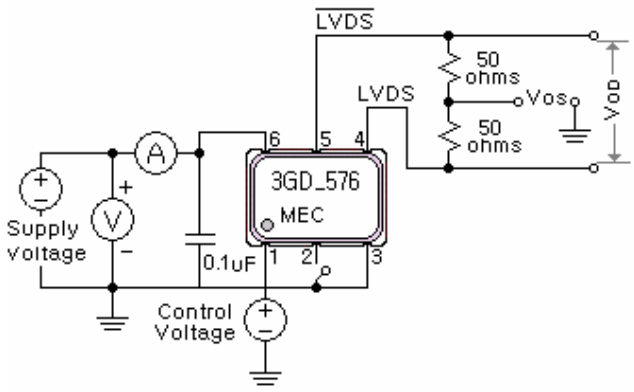
Ex (1) : 3GWD576D - 80T - 125.000 [+3.3V , G_576 type (W characteristics , LVDS output) , ±25ppm (-40°C to 85°C) , pulling : ±80 ppm (typical) , 125.000 MHz]

[1]	Supply voltage , " 3 " for +3.3V		
[2]	Holder type and output wave [" P " for PECL differential , " D " for LVDS differential]		
[3]	Please add " G " after the " type code " for RoHS compliant equivalent (Does not apply to G_576 series) .		
[4]	-10°C ~ 70 °C	" A " ± 25ppm ; " B " ± 50ppm ; " C " ± 100ppm ;	
		If non-standard please enter the desired stability after " C " , for example " C15 " : represents ±15ppm over -10 to +70°C	
	-40°C ~ 85 °C	" D " ± 25ppm ; " E " ± 50ppm ; " F " ± 100ppm ;	
		If non-standard please enter the desired stability after " I " , for example " I20 " : represents ±20ppm over -40 to +85°C	
[5]	Freqency Pulling Range	3.3V	From ±30ppm ~ ±150ppm , control Voltage range : 0.3V ~ 3.0 ; control voltage center : ± 1.65 V
		5.0V	From ±70ppm ~ ±200ppm , control Voltage range : 0.5V ~ 4.5V ; control voltage center : ± 2.5 V
[6]	Pulling Range Code	" M " stands for maximum ; " N " stands for minimum ; " T " stands for typical (tolerance is ± 20%)	
[7]	Center Frequency in MHz		

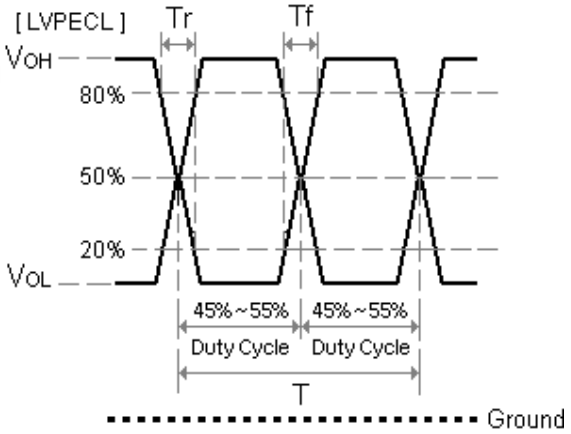
PECL Square Wave Test Circuit



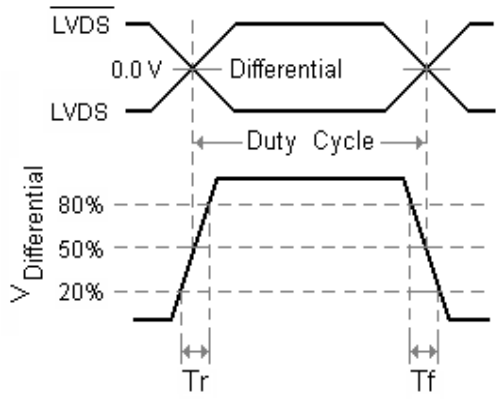
LVDS Square Wave Test Circuit



PECL Square Wave Output Wave Form



LVDS Square Wave Output Wave Form



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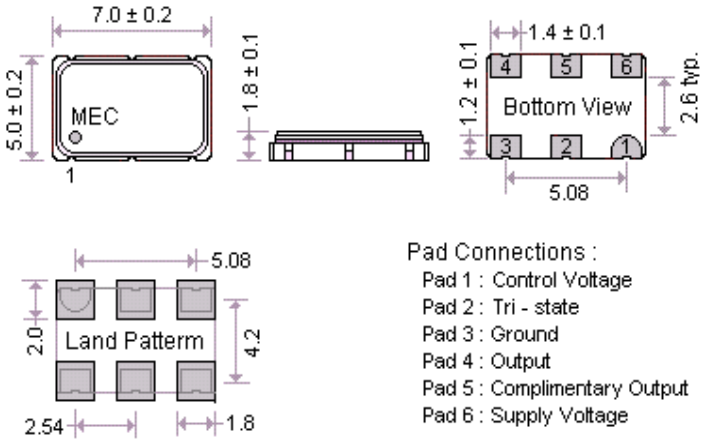
GP_ [LVPECL Differential output]

GD_ [LVDS Differential output]

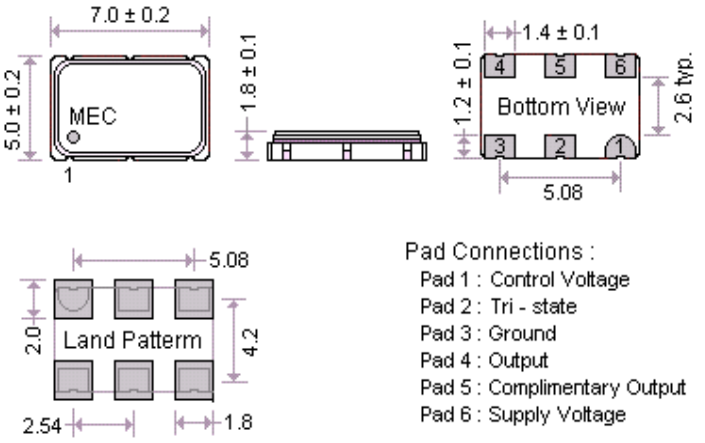
Outline Dimensions (Unit : mm) , Suggested pad Layout for SMDs [Please refer to page 5 for product series selections.]

[GPF576 , GPW576] - - - PECL Differential Output



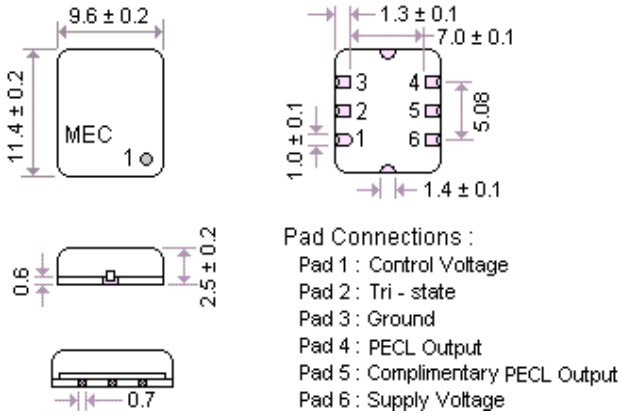
Pad Connections :
- Pad 1 : Control Voltage
- Pad 2 : Tri - state
- Pad 3 : Ground
- Pad 4 : Output
- Pad 5 : Complimentary Output
- Pad 6 : Supply Voltage

[GDF576 , GDW576] - - - LVDS Differential Output



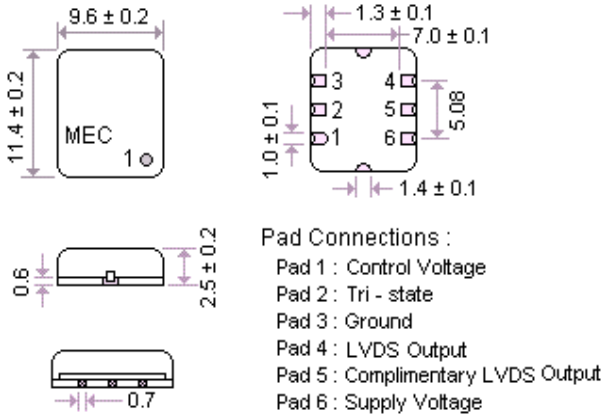
Pad Connections :
- Pad 1 : Control Voltage
- Pad 2 : Tri - state
- Pad 3 : Ground
- Pad 4 : Output
- Pad 5 : Complimentary Output
- Pad 6 : Supply Voltage

[GPF62 , GPW62] - - - PECL Differential Output



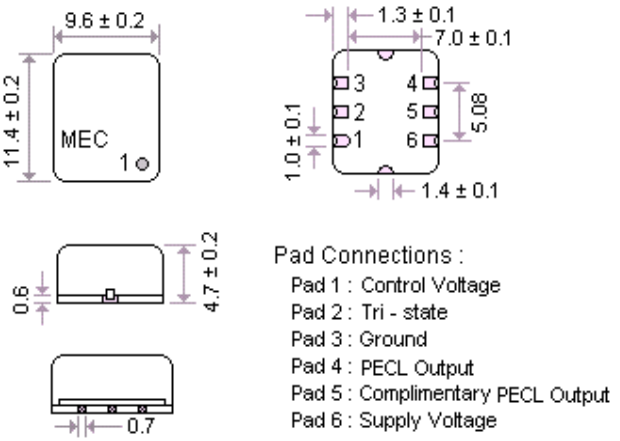
Pad Connections :
- Pad 1 : Control Voltage
- Pad 2 : Tri - state
- Pad 3 : Ground
- Pad 4 : PECL Output
- Pad 5 : Complimentary PECL Output
- Pad 6 : Supply Voltage

[GDF62 , GDW62] - - - LVDS Differential Output



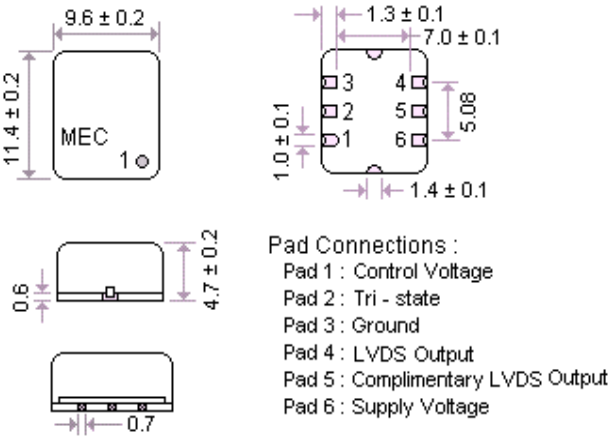
Pad Connections :
- Pad 1 : Control Voltage
- Pad 2 : Tri - state
- Pad 3 : Ground
- Pad 4 : LVDS Output
- Pad 5 : Complimentary LVDS Output
- Pad 6 : Supply Voltage

[GPF64 , GPW64] - - - PECL Differential Output



Pad Connections :
- Pad 1 : Control Voltage
- Pad 2 : Tri - state
- Pad 3 : Ground
- Pad 4 : PECL Output
- Pad 5 : Complimentary PECL Output
- Pad 6 : Supply Voltage

[GDF64 , GDW64] - - - LVDS Differential Output



Pad Connections :
- Pad 1 : Control Voltage
- Pad 2 : Tri - state
- Pad 3 : Ground
- Pad 4 : LVDS Output
- Pad 5 : Complimentary LVDS Output
- Pad 6 : Supply Voltage