mosaic

Mosaic Semiconductor Inc.

512 K X 8 SRAM

MS8512FKX-10/12/15

Issue 2.1 : March 1990

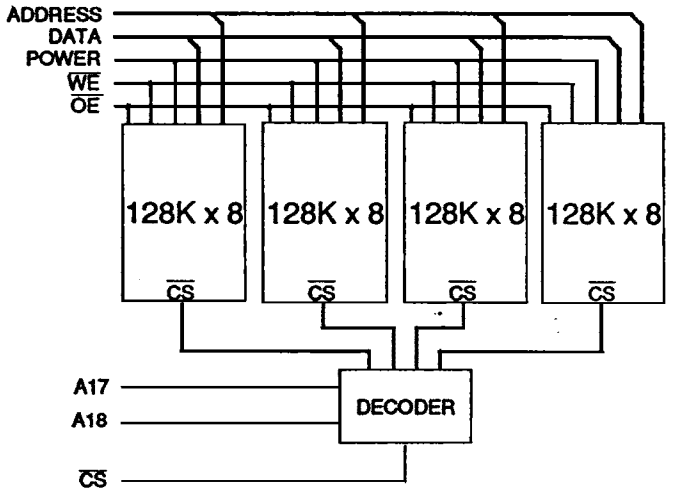
PRELIMINARY

524,288 x 8 CMOS High Speed Static RAM

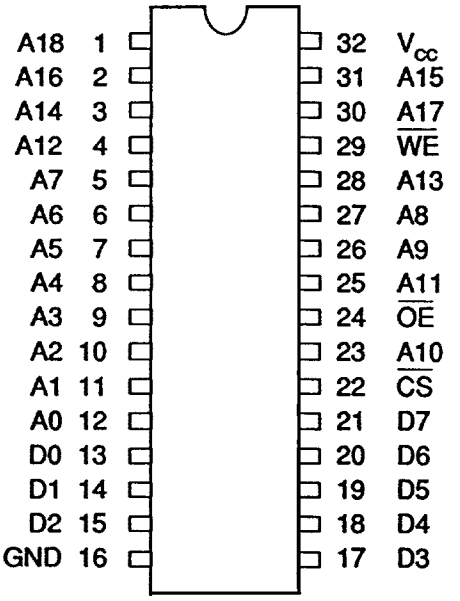
Features

Access Times of 100/120/150 ns
JEDEC Standard 32 pin DIL footprint
Operating Power 230 mW (typ.)
Low Power Standby 20 mW (typ.)
40 µW (typ.) - L
Equal Access and Cycle Times
Battery back-up capability
Completely Static Operation
Common data inputs & outputs
Onboard Decoupling Capacitors

Block Diagram



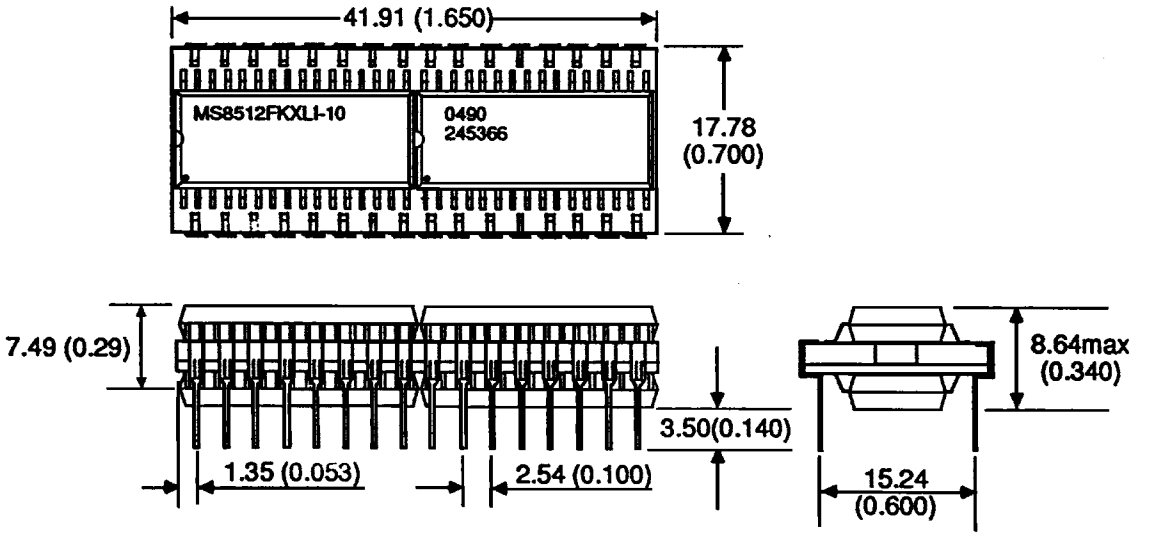
Pin Definition



Pin Functions

A0-A18	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
GND	Ground

Package Details Dimensions in mm (inches).



MOSCS071

Absolute Maximum Ratings

Voltage on any pin relative to V_{SS}	V_T	-0.5V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) V_t can be -3.5V pulse of less than 20ns.

Recommended Operating Conditions

		min	typ	max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	0.6	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (I)

DC Electrical Characteristics

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI1}	$0V \le V_{IN} \le V_{CC}$	-	-	8	µA
(A17, A18, $\overline{CS}$)	I_{LI2}	$0.5V \le V_{IN} \le 2.7V$	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}=V_{IH}$, $V_{I/O}$=Gnd to V_{CC}	-	-	8	µA
Operating Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}$=0mA, I/P's static	-	16	31	mA
Average Current	I_{CC1}	Cycle =1µs, TTL levels	-	46	71	mA
	I_{CC1}	Cycle =1µs, CMOS levels	-	16	30	mA
Standby Current	I_{SB}	TTL Levels	-	4	12	mA
	I_{SB1}	CMOS Levels	-	0.08	8	mA
-L Part	I_{SB2}	CMOS Levels	-	8	500	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

Parameter	*Symbol*	*Test Condition*	*max*	*Unit*
Input Capacitance ($\overline{CS}$, A17, A18)	C_{IN1}	V_{IN} = 0V	6	pF
I/P Capacitance (other)	C_{IN2}	V_{IN} = 0V	32	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	40	pF

Note: Capacitance calculated, not measured.

AC Test Conditions

* Input pulse levels: 0.8V to 2.4V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: 1 TTL gate + 100pF
* V_{CC}=5V±10%

Electrical Characteristics & Recommended AC Operating Conditions

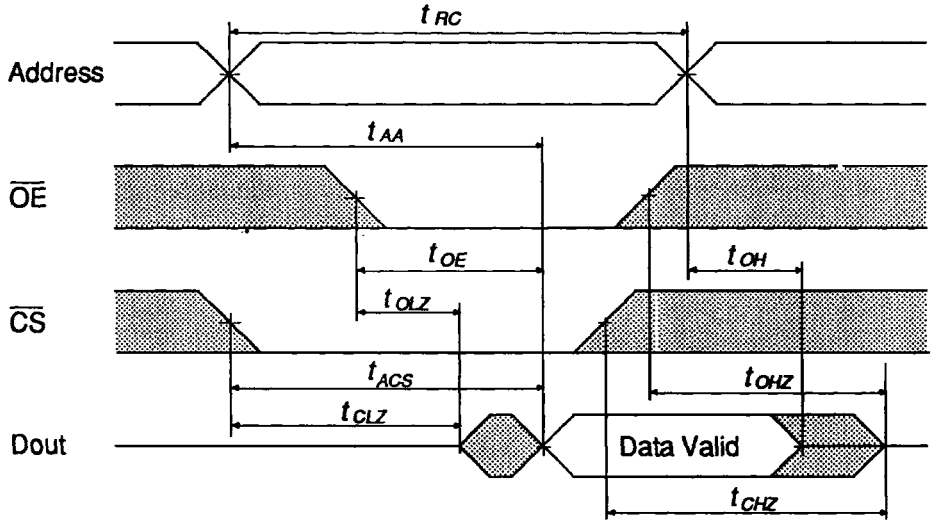
Read Cycle (1,2)

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Read Cycle Time	t_{RC}	100	-	120	-	150	-	ns
Address Access Time	t_{AA}	-	100	-	120	-	150	ns
Chip Select Access Time	t_{ACS}	-	100	-	120	-	150	ns
Output Enable to Output Valid	t_{OE}	-	60	-	70	-	85	ns
Output Hold from Address Change	t_{OH} (2)	10	-	10	-	10	-	ns
Chip Selection to Output in Low Z	t_{CLZ} (2)	10	-	10	-	10	-	ns
Output Enable to Output in Low Z	t_{OLZ} (2)	5	-	5	-	5	-	ns
Chip Deselection to O/P in High Z	t_{CHZ} (2)	0	35	0	45	0	55	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	45	0	55	ns

Notes: 1. WE is High for Read Cycle.

2. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

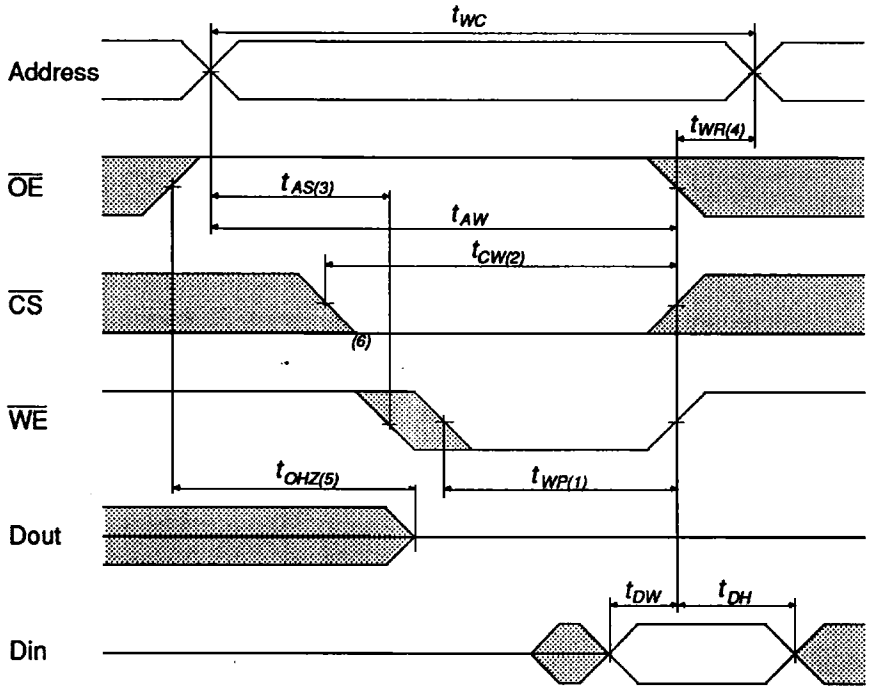
Read Cycle Timing Waveform (1,2)



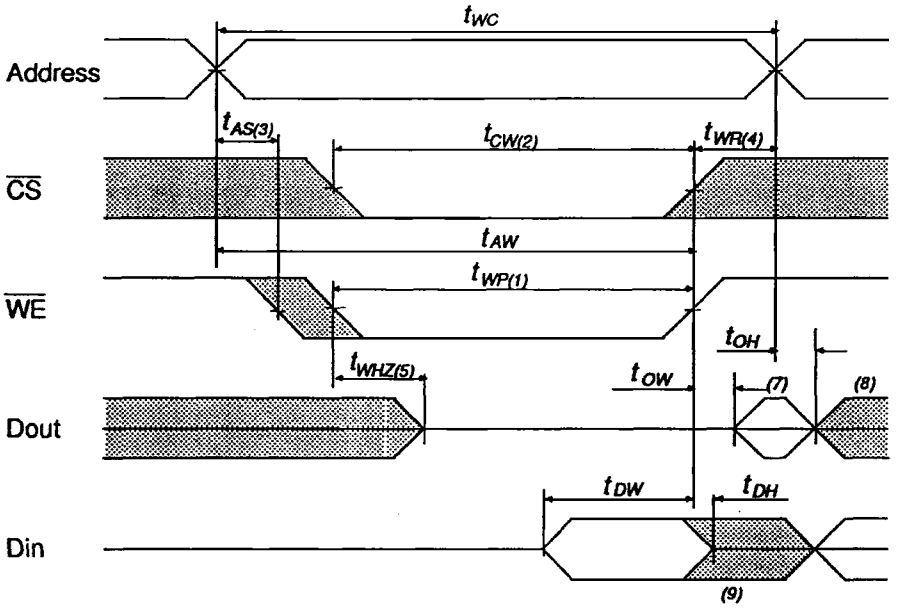
Write Cycle

Parameter	Symbol	-10 min	-10 max	-12 min	-12 max	-15 min	-15 max	Unit
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns
Chip Selection to End of Write	t_{CW}	90	-	100	-	110	-	ns
Address Valid to End of Write	t_{AW}	90	-	100	-	110	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	75	-	85	-	95	-	ns
Write Recovery Time	t_{WR} (10)	5	-	10	-	15	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	45	ns
Data to Write Time Overlap	t_{DW}	40	-	45	-	50	-	ns
Data Hold from Write Time	t_{DH} (10)	0	-	0	-	0	-	ns
Output active from end of write	t_{OW}	5	-	5	-	5	-	ns

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform



Notes:

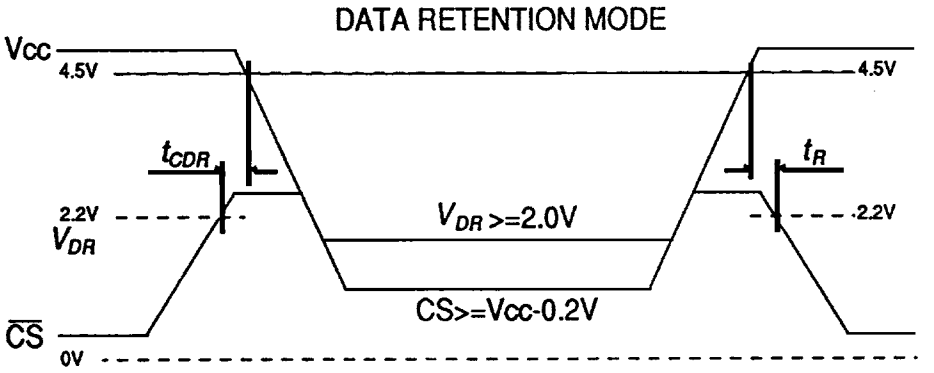
1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{CW} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
3. T_{AS} is measured from the address valid to the beginning of write.
4. T_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of write.
5. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
6. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, outputs remain in a high impedance state.
7. Dout is in the same phase as written data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state, and inputs out of phase must not be applied to I/O pins.
10. This parameter is sampled and not 100% tested.

Low V_{cc} Data Retention Characteristics - L Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current		V_{CC}=3.0V, $\overline{CS} \geq V_{CC}$-0.2V				
	I_{CCDR1}	$T_{OP}=T_A$	-	5	280 (1)	µA
	I_{CCDR2}	$T_{OP}=T_{AI}$		TBA		µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Notes : (1) 110 µA max at T_A= 0 to 40°C

Data Retention Waveform



Ordering Information

MS8512FKXLI-10

Speed	10	= 100 ns
	12	= 120 ns
	15	= 150 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Package	FK	= Plastic 32 pin DIL
Organization	8512	= 512K x 8

The policy of the company is one of continuous development and while the information presented in this data sheet is believed to be accurate, no liability is assumed for any data contained within. The company reserves the right to make changes without notice at any time.

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