Description

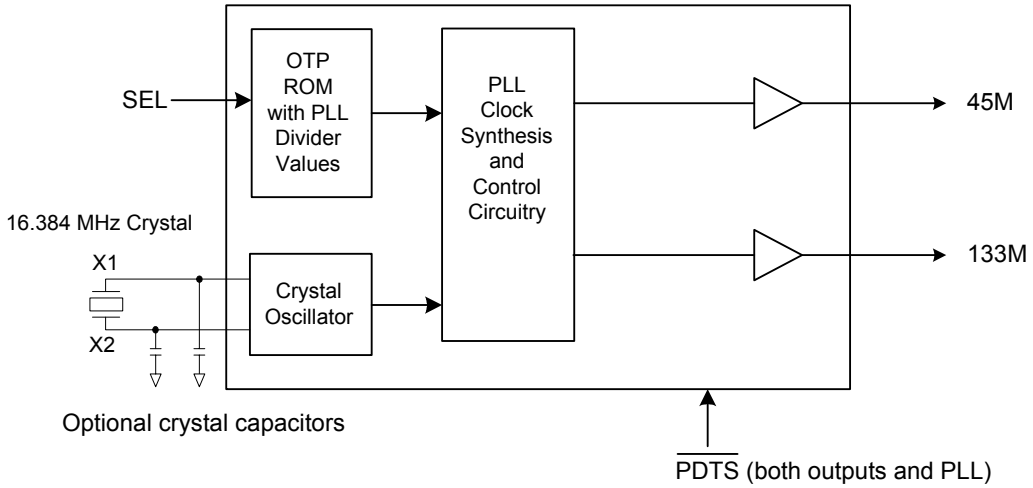
The ICS332-49 is a low-cost frequency generator that is factory programmable. Using analog/digital Phase-Locked-Loop (PLL) techniques, the device accepts a 16.384 MHz clock input to produce output clocks of 45 MHz and 133 MHz. In one selection the 45 MHz clock has center spread spectrum of ±1.0%.

The device also has a power down feature that tri-states the clock outputs and turns off the PLLs when the $\overline{\text{PDTS}}$ pin is taken low.

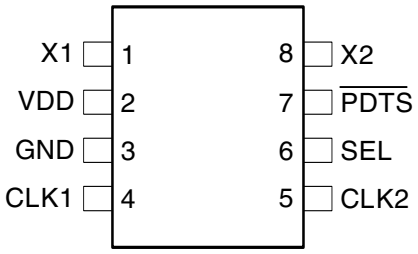
Features

- 8 pin SOIC package – Pb-free, RoHS compliant
- Input clock frequency of 16.384 MHz
- Two output clocks of 45 MHz and 133 MHz
- Spread spectrum enabled at ±1.0% (center)
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low power CMOS process

Block Diagram



Pin Assignment



Output Clock Selection Table

SEL	CLK1 (MHz)	CLK2 (MHz)	Spread on CLK1
0	45	133	-
1	45	133	± 1.0%

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1	XI	Connect this pin to a 16.384 MHz crystal input.
2	VDD	Power	Connect to +3.3 V.
3	GND	Power	Connect to ground.
4	CLK1	Output	45 MHz clock output with selectable ±1.0% spread spectrum. Weak internal pull-down when tri-state.
5	CLK2	Output	133 MHz clock output. Weak internal pull-down when tri-state.
6	SEL	Input	Select pin for frequency selection on CLK1 and CLK2. Internal pull-up.
7	PDTS	Input	Powers down entire chip. Tri-states CLK outputs when low. Internal pull-up.
8	X2	XO	Connect this pin to a 16.384 MHz crystal input.

External Components

Series Termination Resistor

Clock output traces over one inch should use series termination. To series terminate a 50Ω trace (a commonly used trace impedance), place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Decoupling Capacitor

As with any high-performance mixed-signal IC, the ICS332-49 must be isolated from system power supply noise to perform optimally.

A decoupling capacitor of 0.01µF must be connected between VDD and the PCB ground plane.

Crystal Load Capacitors

The device crystal connections should include pads for small capacitors from X1 to ground and from X2 to ground. These capacitors are used to adjust the stray capacitance of the board to match the nominally required crystal load capacitance. Because load capacitance can only be increased in this trimming process, it is important to keep stray capacitance to a minimum by using very short PCB traces (and no vias) between the crystal and device. Crystal capacitors

must be connected from each of the pins X1 and X2 to ground.

The value (in pF) of these crystal caps should equal (C_L -6 pF)*2. In this equation, C_L= crystal load capacitance in pF. Example: For a crystal with a 16 pF load capacitance, each crystal capacitor would be 20 pF [(16-6) x 2 = 20].

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the ICS332-49. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS332-49. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.15	+3.3	+3.45	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.15	3.3	3.45	V
Supply Current	IDD	No load, $\overline{PDTS}$=1		35		mA
		No load, $\overline{PDTS}$=0		21		µA
Input High Voltage, $\overline{PDTS}$	V_{IH}		VDD-0.5			V
Input Low Voltage, $\overline{PDTS}$	V_{IL}				0.4	V
Input High Voltage, SEL	V_{IH}		2			V
Input Low Voltage, SEL	V_{IL}				0.4	V
Input High Voltage, ICLK	V_{IH}		VDD/2+1			V
Input Low Voltage, ICLK	V_{IL}				VDD/2-1	V
Output High Voltage (CMOS High)	V_{OH}	I_{OH} = -8 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.4	V
Short Circuit Current	I_{OS}			±70		mA
Internal Pull-up Resistor	R_{PU}			360		kΩ
Internal Pull-down Resistor	R_{PD}			510		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}			16.384		MHz
Output Rise Time	t_{OR}	0.8 to 2.0 V, Note 1		1.3		ns
Output Fall Time	t_{OF}	2.0 to 0.8 V, Note 1		0.9		ns
Duty Cycle			40	50	60	%
Cycle Jitter (short term jitter)	t_{ja}	Peak to peak, 52M no spread and 120M CLKs		±150		ps
Output Frequency Synthesis Error		45M clock		-2		ppm
Output Frequency Synthesis Error		133M clock		-4		ppm
Output Enable Time	t_{OE}	PDTS high to output on		250		µs
Output Disable Time	t_{OD}	PDTS low to tri-state		200		µs

Notes:

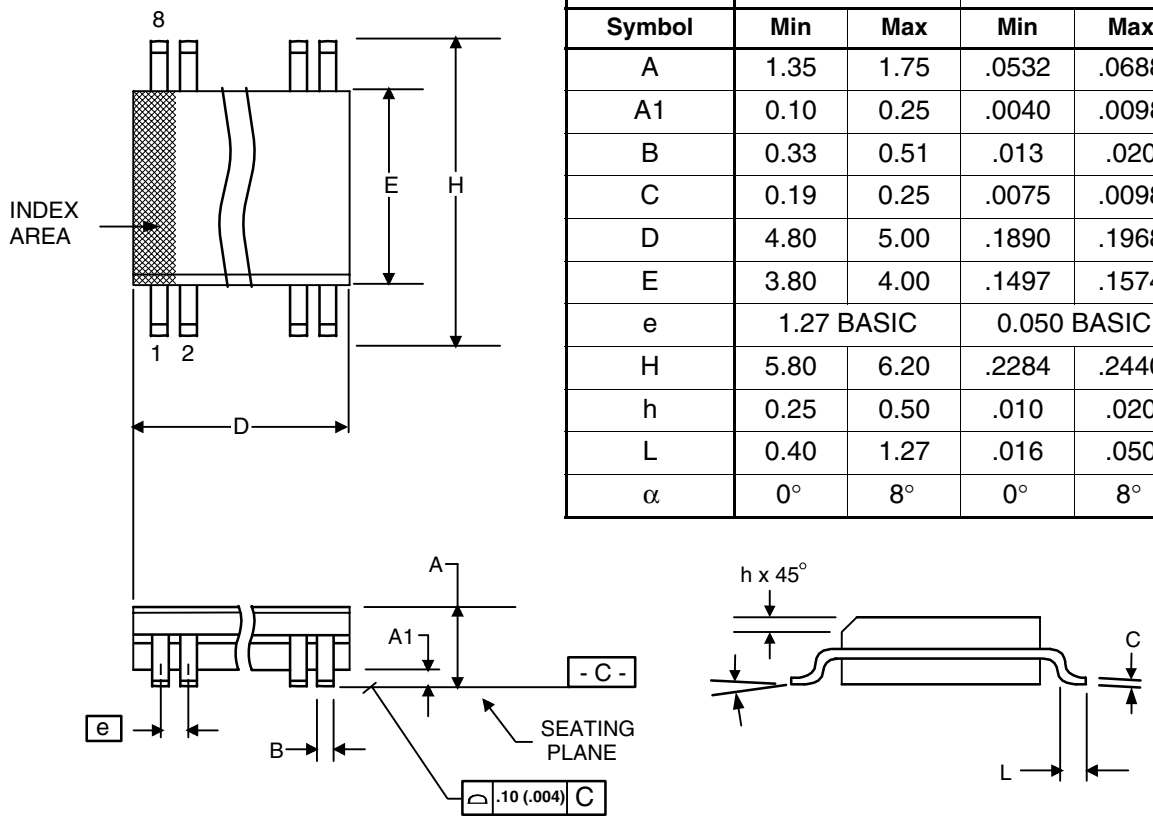
1. Measured with a 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		150		°C/W
	θ_{JA}	1 m/s air flow		140		°C/W
	θ_{JA}	3 m/s air flow		120		°C/W
Thermal Resistance Junction to Case	θ_{JC}			40		°C/W

Package Outline and Package Dimensions (8-pin SOIC, 150 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	4.80	5.00	.1890	.1968
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
332M-49LF	332M49L	Tubes	8-pin SOIC	0 to +70° C
332M-49LFT	332M49L	Tape and Reel	8-pin SOIC	0 to +70° C

"LF" denotes Pb (lead) free package.