REVISION HISTORY

Revision	Description	Issue Date
Rev. 0.1	Initial Issue	October.06.2005
Rev. 0.2	Edit package	October.21.2005
Rev. 0.3	Edit A0, A1, A2 address pins	December.06.2005
Rev. 0.4	Integral 2K, 4K, 8K, 16K datasheet	December.12.2005

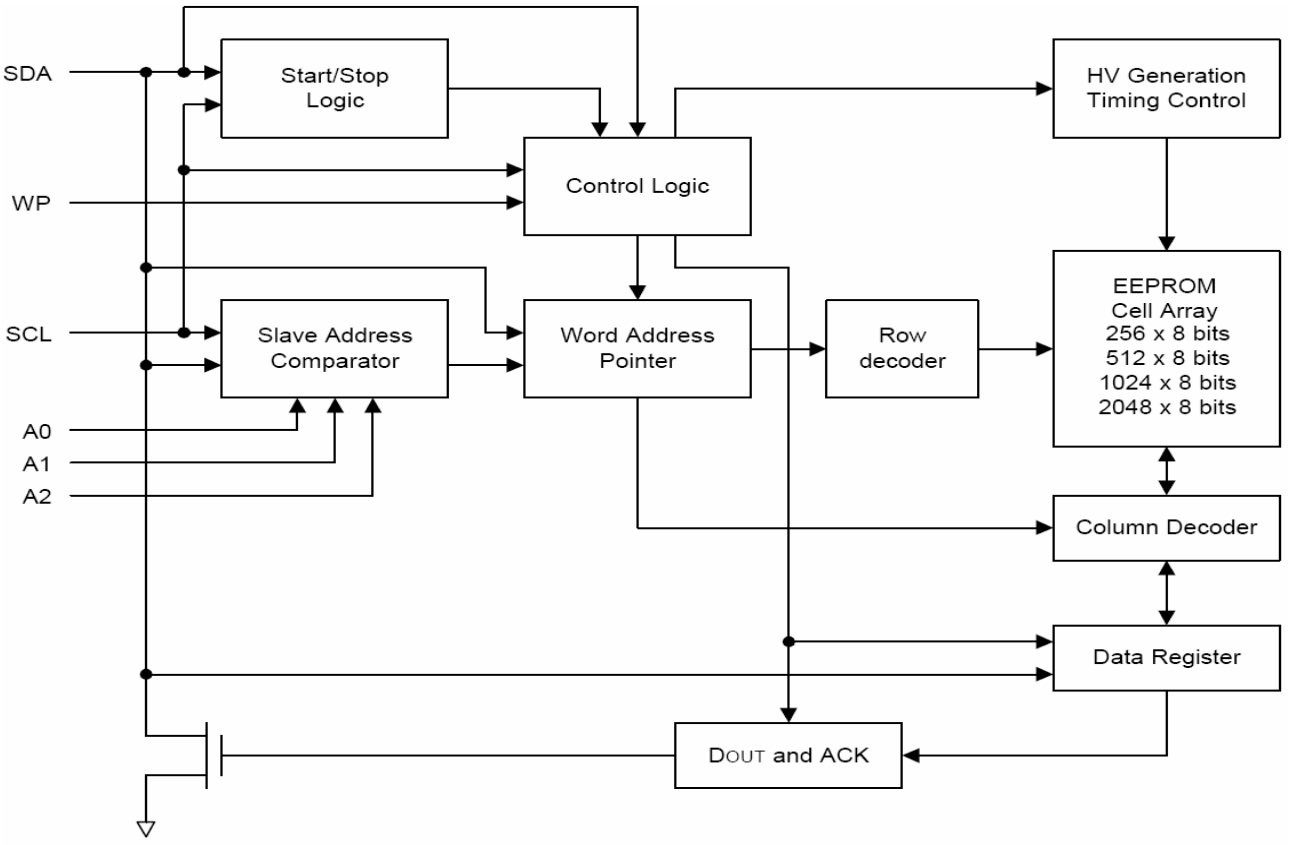
FEATURES

- 2-wire serial interface
- Automatic word address increment
- Operating voltage:1.8V~5.5V
- Operating current
  Maximum write current: <3mA at 5.5V
  Maximum read current: <0.5mA at 5.5V
  Maximum stand-by current: <5uA at 5.5V
- 16-byte page buffer
- Hardware controlled write protection
- EEPROM programming voltage generated on chip
- 1,000,000 erase/write cycle
- 100 years data retention
- Operating temperature range
  0℃ to +70℃ (commercial)
- 8-pin DIP，SOP，TSSOP package
- **Lead free and green package available**

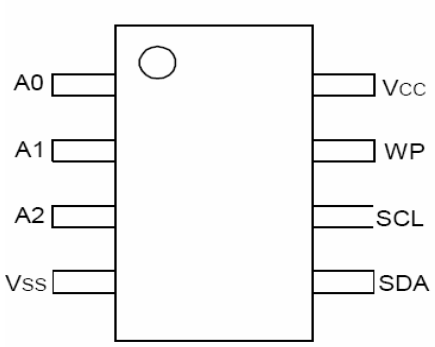
GENERAL DESCRIPTION

The LY24C02/04/08/16 is a 2,048 / 4,096 / 8192 / 16,384-bit serial read/write non-volatile memory device, supporting the standard 2 wire serial interface. It is fabricated using most advanced CMOS technology. It has been developed for low power and low voltage application (1.8V to 5.5V).The LY24C02/04/08/16 is guaranteed for 1,000,000 erase/write cycles and 100 years data retention.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Note: The LY24C02/04/08/16 is available in 8-pin DIP, SOP, TSSOP package.

PIN DESCRIPTION

SYMBOL	TYPE	DESCRIPTION
A0 – A2	Input	Device Address Inputs
SDA	I/O	Serial Data Inputs/Outputs
SCL	Input	Serial clock Input
WP	Input	Write protect Input
Vcc	---	Power Supply
Vss	---	Ground

ABSOLUTE MAXIMUN RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	Vcc	-0.3 to +6.5	V
Input voltage	Vin	-0.3 to +6.5	V
Output voltage	Vo	-0.3 to +6.5	V
Operating temperature	T_A	0 to 70	℃
Storage Temperature	T_{STG}	-65 to 150	℃

DC ELECTRICAL CHARACTERISTICS

PARAMETER		SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Power Supply		Vcc		1.8	5.5	V
Input Low Voltage		V_{IL}	SCL, SDA, A0, A1, A2	-0.3	0.3 Vcc	V
Input High Voltage		V_{IH}		0.7 Vcc	Vcc+0.3	V
Input Leakage Current		I_{LI}	V_{IN} =0 to V_{CC}	-	10	μA
Output Leakage Current		I_{LO}	V_{OUT} =0 to V_{CC}	-	10	μA
Output Low Voltage		V_{OL}	I_{OL} = 0.15mA,Vcc=1.8V	-	0.2	V
			I_{OL} = 2.1mA, Vcc=2.5V	-	0.4	V
Power Supply Current	Write	I_{CCW}	Minimum cycle= 400kHz	-	3	mA
	Read	I_{CCR}	Minimum cycle= 400kHz	-	0.5	
Standby Power Supply Current		Isb	Vcc=SDA=SCL=5.5V All other inputs =0V	-	5	uA

Notes:
1. T_A=-25℃ to 70℃(C), -40℃ to +85℃(I), V_{CC}=1.8V to 5.5V

D.C. Electrical Characteristics (Continued)

PARAMETER	SYMBOL	Conditions	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	25℃, 1MHz, Vcc=5V,V_{IN}=0V A0,A1,A2 SCL and WP pin	-	10	pF
Input/Output Capacitance	$C_{I/O}$	25℃, 1MHz, Vcc=5V,$V_{I/O}$=0V SDA pin	-	10	pF

AC ELECTRICAL CHARACTERISTICS

PARAMETER	SYM.	Conditions	Vcc = 1.8 to 5.5V (Standard Mode)		Vcc = 2.5 to 5.5V (Fast Mode)		UNIT
			MIN.	MAX.	MIN.	MAX.	
External clock frequency	f_{CLK}	-	0	100	0	400	kHz
Clock high time	t_{HIGH}	-	4	-	0.6	-	us
Clock low time	t_{LOW}	-	4.7	-	1.3	-	us
Rising time	t_R	SDA, SCL	-	1	-	0.3	us
Falling time	t_F	SDA, SCL	-	0.3	-	0.3	us
Start condition hold time	$t_{HD:STA}$	-	4	-	0.6	-	us
Start condition setup time	$t_{SU:STA}$	-	4.7	-	0.6	-	us
Data input hold time	$t_{HD:DAT}$	-	0	-	0	-	us
Data input setup time	$t_{SU:DAT}$	-	0.25	-	0.1	-	us
Stop condition setup time	$t_{SU:STO}$	-	4	-	0.6	-	us
Bus free time	t_{BUF}	Before new transmission	4.7	-	1.3	-	us
Data output valid from clock low(note)	t_{AA}	-	0.3	3.5	-	0.9	us
Noise spike width	t_{SP}	-	-	100	-	50	ns
Write cycle time	t_{WR}	-	-	5	-	5	ms

Notes:

1. Upon customers request up to 400 kHz (Max.)in standard mode and 1 MHz in fast mode are available.
2. When acting as a transmitter, the LY24C02/04/08/16 must provide an internal minimum delay time to bridge the undefined (minimum 300 ns)
   Of the falling edge of SCL. This is required to avoid unintended generation of a start or stop condition.

FUNCTION DESCRIPTION

I²C-BUS INTERFACE

The LY24C02/04/08/16 supports the I²C-bus serial interface data transmission protocol.
The 2-wire bus consists of a serial data line (SDA) and a serial clock line (SCL). The SDA and the SCL lines must be connected to Vcc by a pull-up resistor that is located somewhere on the bus.
Any device that puts data onto the bus is defined as the “transmitter” and any device that gets data from the bus is the “receiver.” The bus is controlled by a master device which generates the serial clock and start/stop conditions, controlling bus access. The A2, A1 and A0 pins are device address inputs that are hard wired for the LY24C02/04/08/16. As many as eight for 2K (four for 4K,two for 8K, one for 16K)devices may be addressed on a single bus system.

A0, A1, A2

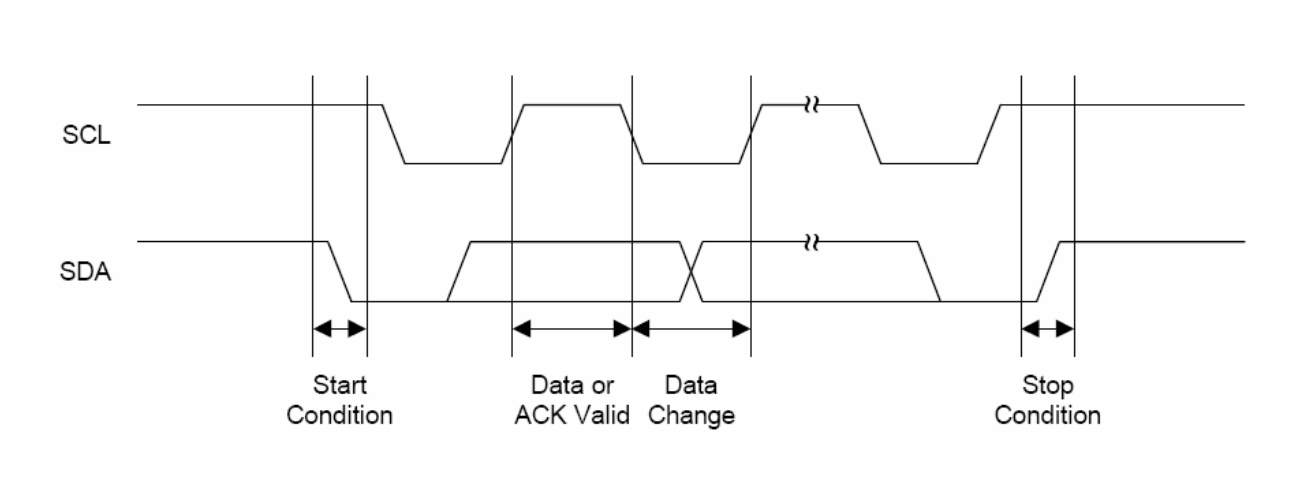
The A0, A1 and A2 pins are device address inputs that are hard wired for the LY24C02. As many as eight for 2K devices may be addressed on a single bus system.
The LY24C04 uses A1 and A2 pins for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is not connected in the LY24C04.
The LY24C08 only use the A2 input for hard wire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects in the LY24C08.
The LY24C16 does not use the A0, A1, A2 device address pins. so the A0, A1, A2 pins have no connection.

I²C-BUS PROTOCOLS

Here are several rules for I²C-bus transfers:
— A new data transfer can be initiated only when the bus is currently not busy.
— MSB is always transferred first in transmitting data.
— During a data transfer, the data line (SDA) must remain stable whenever the clock line (SCL) is high.

The I2C-bus interface supports the following communication protocols:

- Bus not busy: The SDA and the SCL lines remain High level when the bus is not active.
- Start condition: Start condition is initiated by a High-to-Low transition of the SDA line while SCL remains High level. All bus commands must be preceded by a start condition.
- Stop condition: A stop condition is initiated by a Low-to-High transition of the SDA line while SCL remains High level. All bus operations must be completed by a stop condition

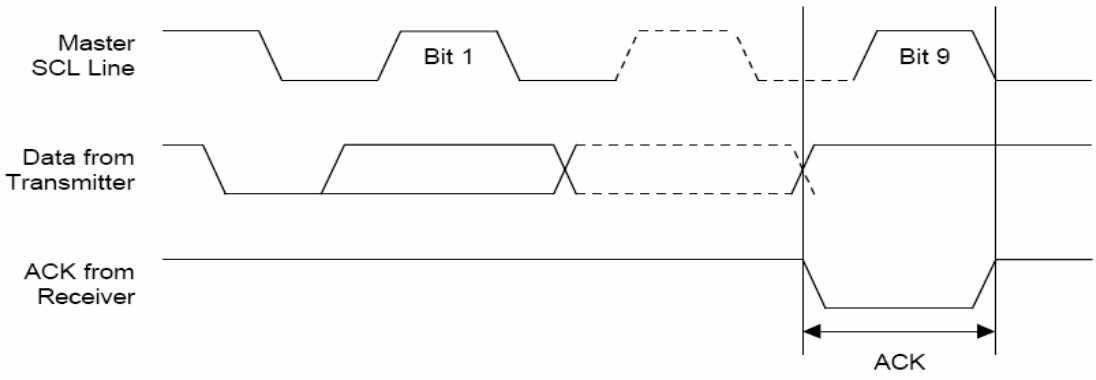


Note: Data transmission sequence

- Data valid: Following a start condition, the data becomes valid if the data line remains stable for the duration of the High period of SCL. New data must be put onto the bus while SCL is Low. Bus timing is one clock pulse per data bit. The number of data bytes to be transferred is determined by the master device. The total number of bytes that can be transferred in one operation is theoretically unlimited.

- ACK (Acknowledge): An ACK signal indicates that a data transfer is completed successfully. The transmitter (the master or the slave) releases the bus after transmitting eight bits. During the 9th clock, which the master generates, the receiver pulls the SDA line low to acknowledge that it successfully received the eight bits of data (see Figure 3-8). But the slave does not send an ACK if an internal write cycle is still in progress.

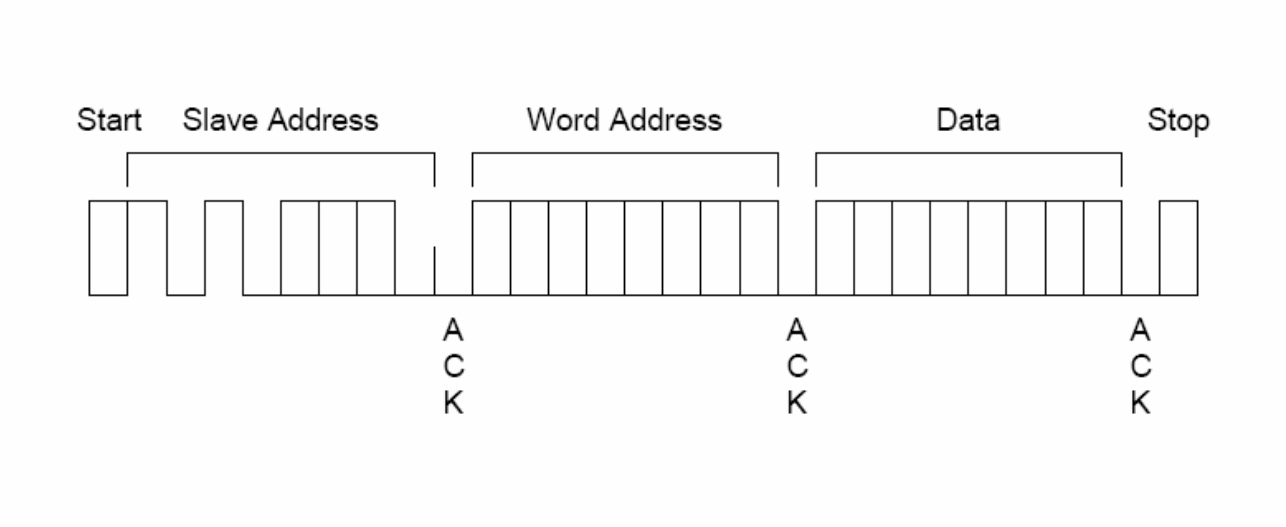
In data read operations, the slave releases the SDA line after transmitting 8 bits of data and then monitors the line for an ACK signal during the 9th clock period. If an ACK is detected, the slave will continue to transmit data. If an ACK is not detected, the slave terminates data transmission and waits for a stop condition to be issued by the master before returning to its stand-by mode.



Note: Acknowledge response from receiver

BYTE WRITE OPERATION

In a complete byte write operation, the master transmits the slave address, word address, and one data byte to the LY24C02/04/08/16 slave device



Note: Byte write operation

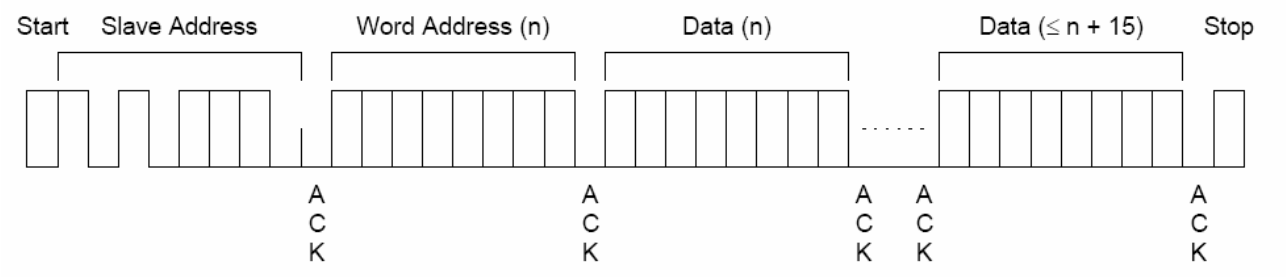
Following the Start condition, the master sends the device identifier (4 bits), the device address (3 bits), and an R/W bit set to “0” onto the bus. Then the addressed LY24C02/04/08/16 generates an ACK and waits for the next byte. The next byte to be transmitted by the master is the word address. This 8-bit address is written into the word address pointer of the LY24C02/04/08/16

When the LY24C02/04/08/16 receives the word address, it responds by issuing an ACK and then waits for the next 8-bit data. When it receives the data byte, the LY24C02/04/08/16 again responds with an ACK. The master terminates the transfer by generating a Stop condition, at which time the LY24C02/04/08/16 begins the internal write cycle.

While the internal write cycle is in progress, all LY24C02/04/08/16 inputs are disabled and the LY24C02/04/08/16 does not respond to additional requests from the master.

PAGE WRITE OPERATION

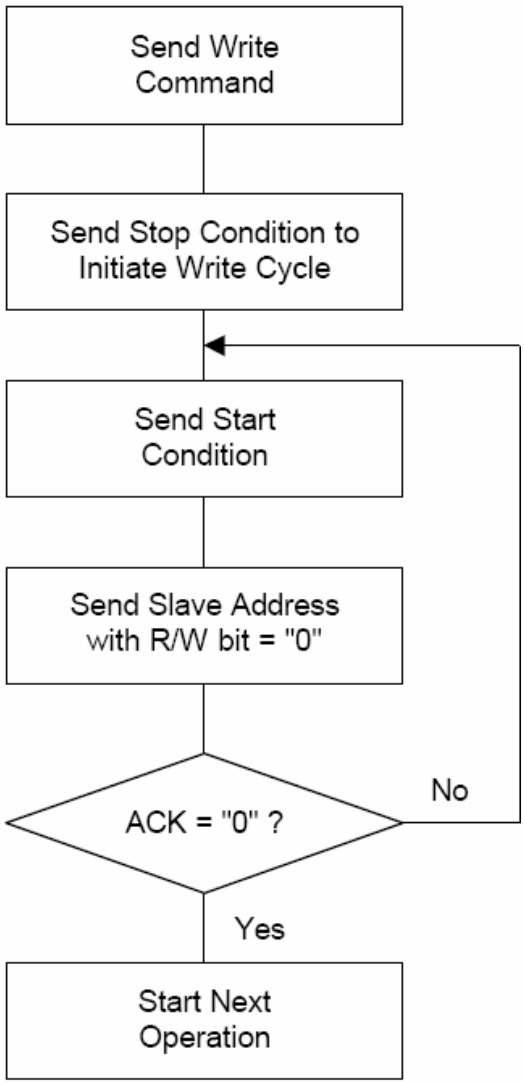
The LY24C02/04/08/16 can also perform 16-byte page write operation. A page write operation is initiated in the same way as a byte write operation. However, instead of finishing the write operation after the first data byte is transferred, the master can transmit up to 15 additional bytes. The LY24C02/04/08/16 responds with an ACK each time it receives a complete byte of data.



Note: Page write operation

The LY24C02/04/08/16 automatically increments the word address pointer each time it receives a complete data byte. When one byte has been received, the internal word address pointer increments to the next address and the next data byte can be received.
If the master transmits more than 16 bytes before it generates a stop condition to end the page write operation, the LY24C02/04/08/16 word address pointer value “rolls over” and the previously received data is overwritten.
If the master transmits less than 16 bytes and generates a stop condition, the LY24C02/04/08/16 writes the received data to the corresponding EEPROM address.
During a page write operation, all inputs are disabled and there is no response to additional requests from the master until the internal write cycle is completed.

POLLING FOR AN ACK SIGNAL
When the master issues a stop condition to initiate a write cycle, the LY24C02/04/08/16 starts an internal write cycle. The master can then immediately begin polling for an ACK from the slave device.
To poll for an ACK signal in a write operation, the master issues a start condition followed by the slave address. As long as the LY24C02/04/08/16 remains busy with the write operation, no ACK is returned. When the LY24C02/04/08/16 completes the write operation, it returns an ACK and the master can then proceed with the next read or write operation.



Note: Master polling for an ACK signal from a slave device

HARDWARE-BASED WRITE PROTECTION

You can also write-protect the entire memory area of the LY24C02/04/08/16. This method of write protection is controlled by the state of the Write Protect (WP) pin.

When the WP pin is connected to VCC, any attempt to write a value to the memory is ignored.The LY24C02/04/08/16 will acknowledge slave and word address, but it will not generate an acknowledge after receiving the first byte of the data. Thus the write cycle will not be started when the stop condition is generated.

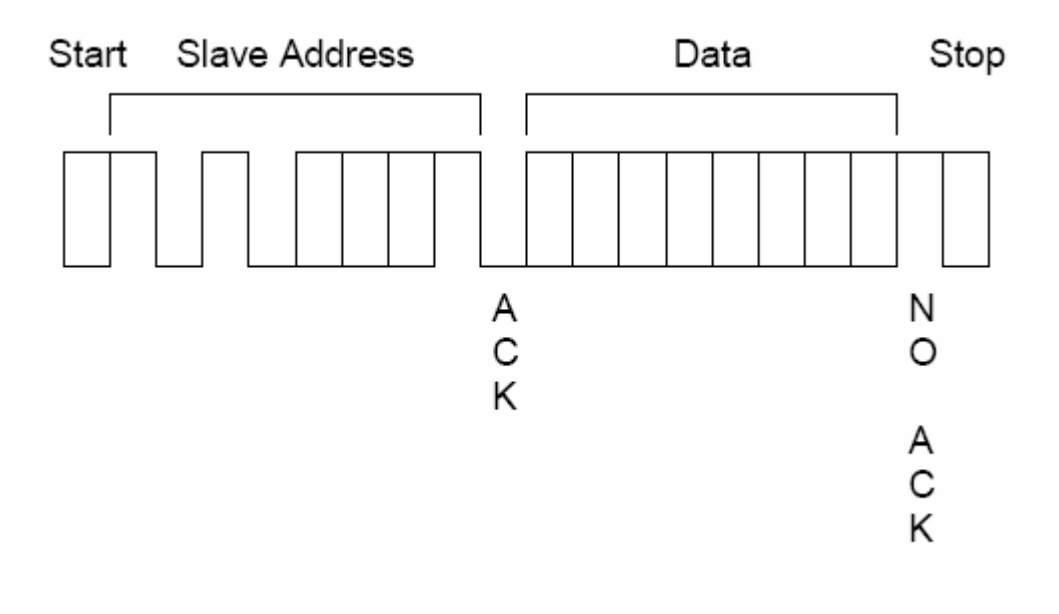
By connecting the WP pin to VSS, the write function is allowed for the entire memory.

These write protection features effectively change the EEPROM to a ROM in order to prevent data from being overwritten. Whenever the write function is disabled, a slave address and a word address are acknowledged on the bus, but data bytes are not acknowledged.

CURRENT ADDRESS BYTE READ OPERATION

The internal word address pointer maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either read or write) was to the address “n”, the next read operation would access data at address “n+1”.

When the LY24C02/04/08/16 receives a slave address with the R/W bit set to “1”, it issues an ACK and sends the eight bits of data. The master does not acknowledge the transfer but it does generate a Stop condition. In this way, the LY24C02/04/08/16 effectively stops the transmission.

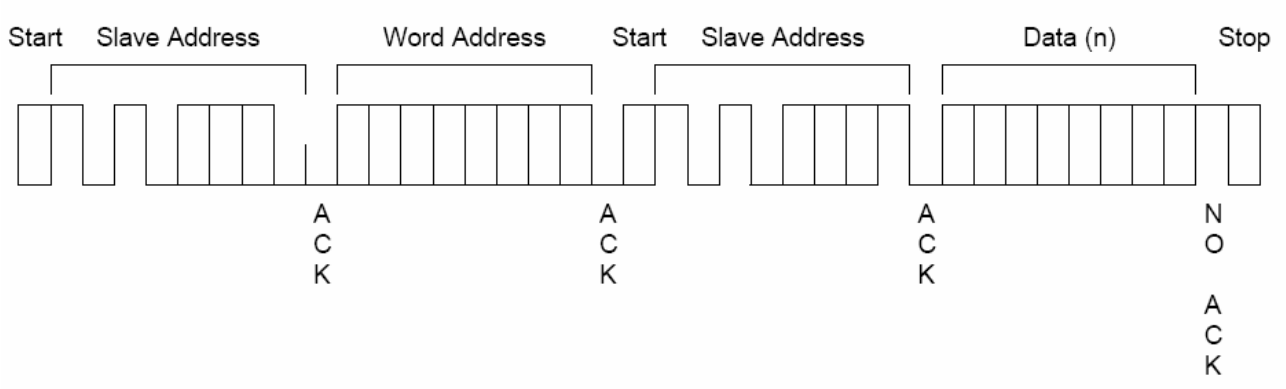


Note: Current address byte read operation

RANDOM ADDRESS BYTE READ OPERATION

Using random read operations, the master can access any memory location at any time. Before it issues the slave address with the R/W bit set to “1”, the master must first perform a “dummy” write operation. This operation is performed in the following steps:

1. The master first issues a Start condition, the slave address, and the word address to be read. (This step sets the internal word address pointer of the LY24C02/04/08/16 to the desired address.)
2. When the master receives an ACK for the word address, it immediately re-issues a start condition followed by another slave address, with the R/W bit set to “1”.
3. TheLY24C02/04/08/16 then sends an ACK and the 8-bit data stored at the desired address.
4. At this point, the master does not acknowledge the transmission, but generates a stop condition instead.
5. In response, the LY24C02/04/08/16 stops transmitting data and reverts to its stand-by mode.



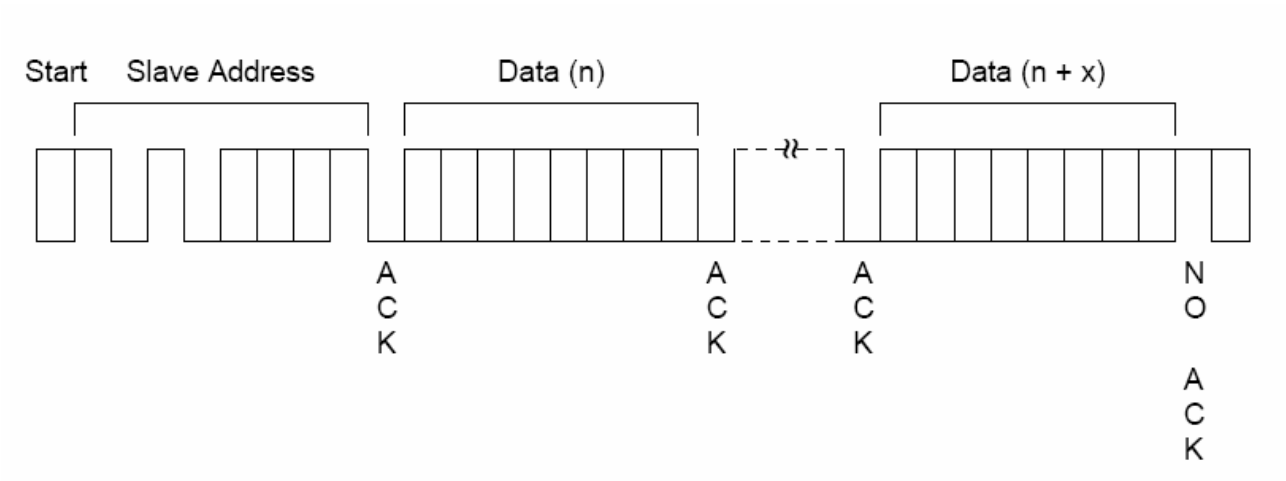
Note: Random address byte read operation

SEQUENTIAL READ OPERATION

Sequential read operations can be performed in two ways: as a series of current address reads or as random address reads. The first data is sent in the same way as the previous read mode used on the bus. The next time,however, the master responds with an ACK, indicating that it requires additional data.

The LY24C02/04/08/16 continues to output data for each ACK it receives. To stop the sequential read operation, the master does not respond with an ACK, but instead issues a Stop condition.

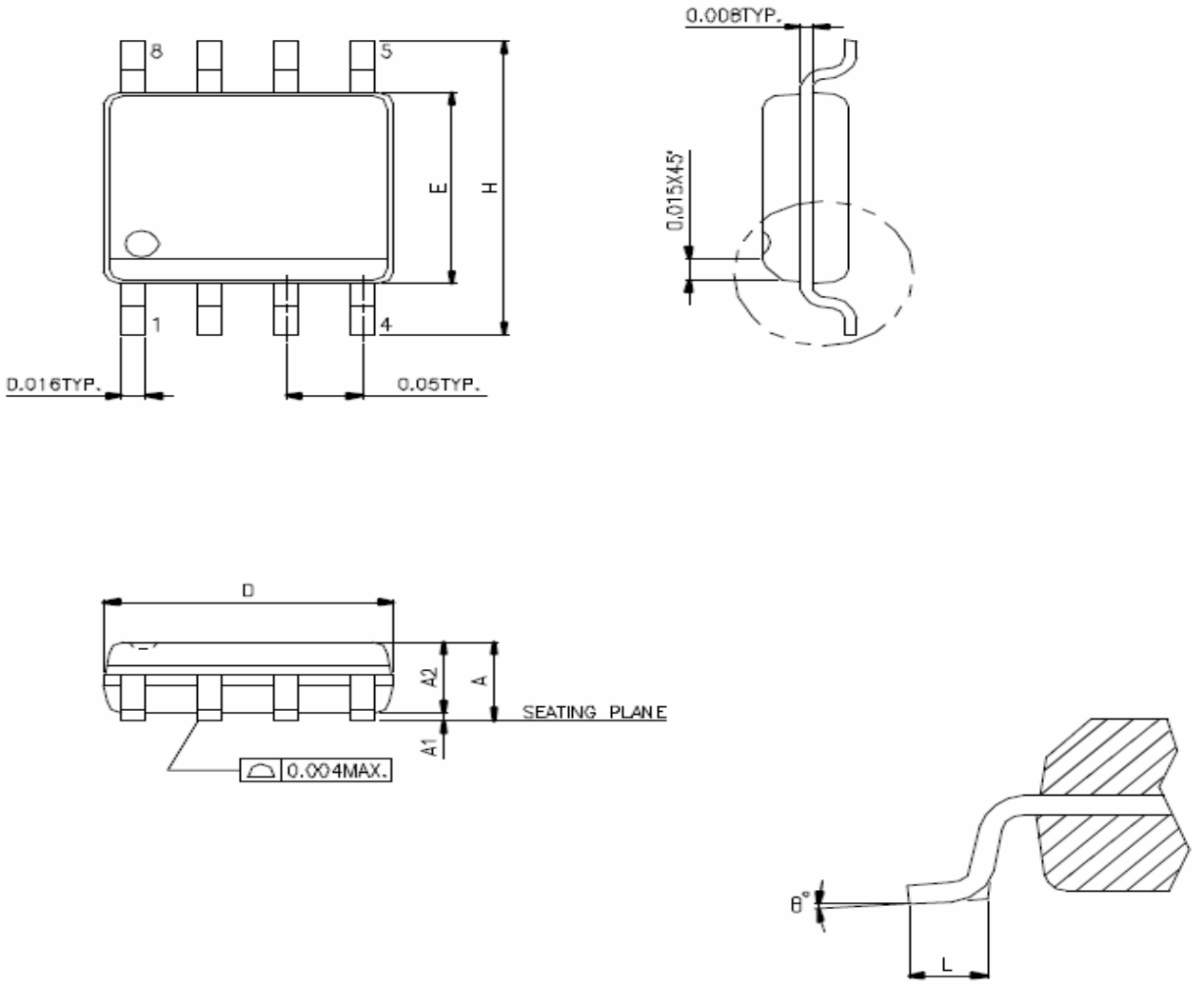
Using this method, data is output sequentially with the data from address “n” followed by the data from “n+1”. The word address pointer for read operations increments all word addresses, allowing the entire EEPROM to be read sequentially in a single operation. After the entire EEPROM is read, the word address pointer “rolls over” and the LY24C02/04/08/16 continues to transmit data for each ACK it receives from the master.



Note: Sequential read operation

PACKAGE OUTLINE DIMENSION

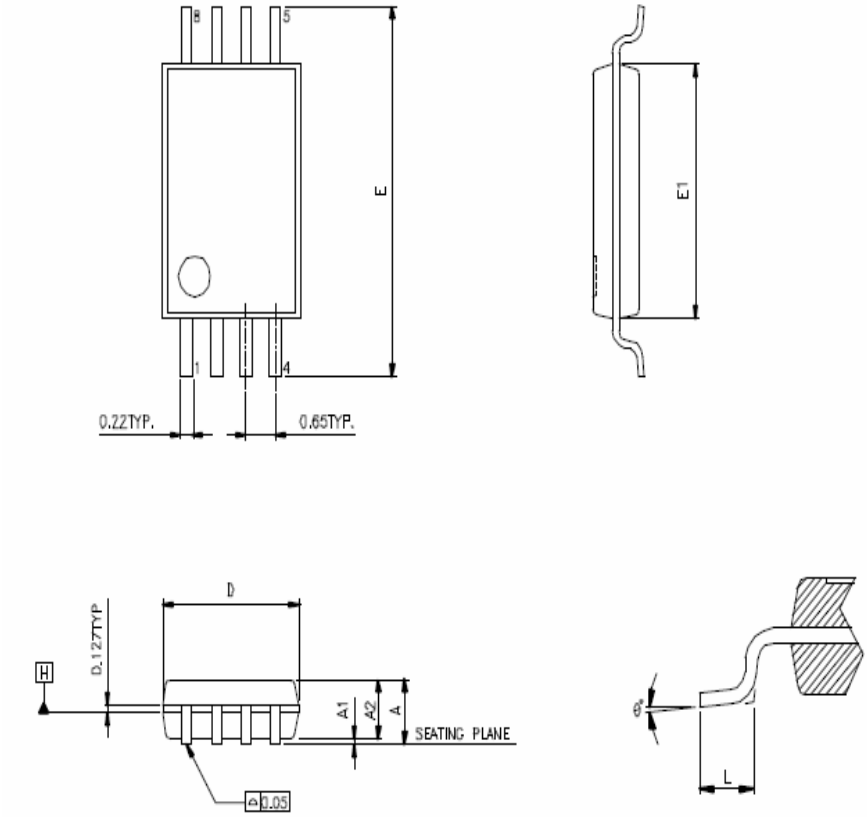
8-pin 150mil SOP Package Outline Dimension



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
A2	–	0.059
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

8-pin TSSOP Package Outline Dimension

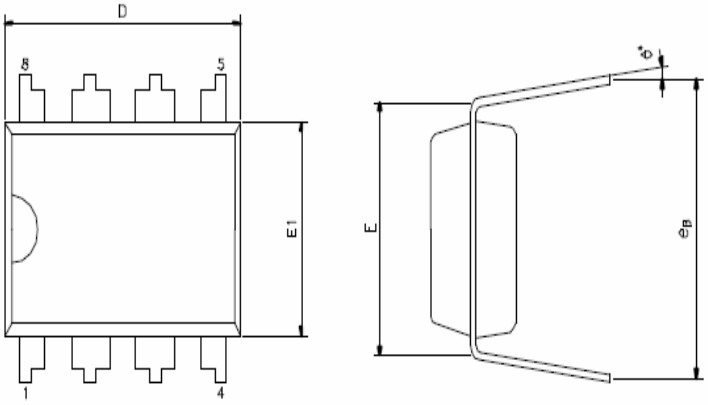


SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.96	1.01	1.06
D	2.90	3.00	3.10
E		6.40 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ°	0	–	8

UNIT : MM

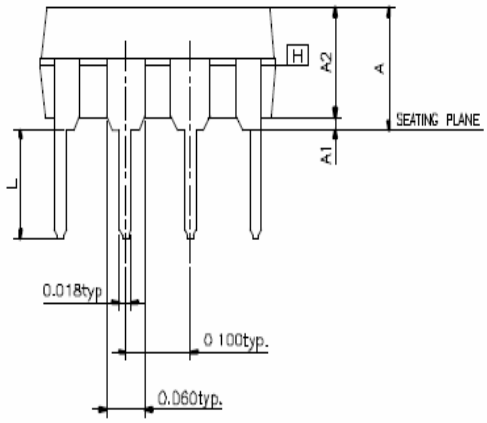
NOTES:
1. JEDEC OUTLINE : MO-153 AA
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3. DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4. DIMENSION '0.22' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE '0.22' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM
5. DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

8-pin 300mil PDIP Package Outline Dimension



SYMBOLS	MIN.	NOR.	MAX.
A	–	–	0.210
A1	0.015	–	–
A2	0.125	0.130	0.135
D	0.355	0.365	0.400
E		0.300 BSC.	
E1	0.245	0.250	0.255
L	0.115	0.130	0.150
e_B	0.335	0.355	0.375
θ°	0	7	15

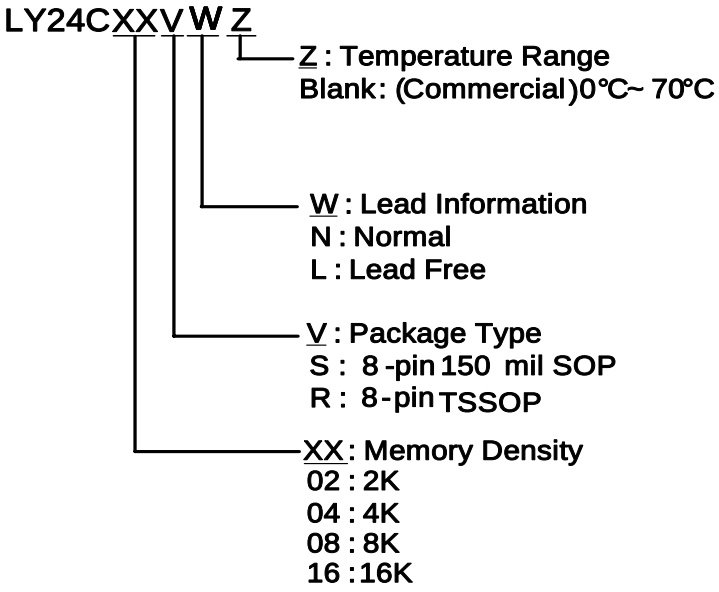
UNIT : INCH



NOTES:

1. JEDEC OUTLINE : MS-001 BA
2. "D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
3. eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
4. POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
5. DISTANCE BETWEEN LEADS INCLUDING DAM BAR PROTRUSIONS TO BE .005 INCH MININUM.
6. DATUM PLANE [H] COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.

Ordering information



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