LT-1001 Series Precision Operational Amplifiers

Features

- Ultra-low V_{OS} — 15 μV max
- Ultra-low V_{OS} drift — 0.6 μV/°C max
- Low input bias current — 2 nA max
- High CMRR — 114 dB min
- High PSRR — 110 dB min
- Low noise — 0.3 μV_{p-p} (0.1 to 10 Hz)
- Low power dissipation — 75 mW max
- High gain linearity
- LCC, SO-8, DIP and can packages

Description

Designed for low level signal conditioning, instrumentation, and data conversion applications, the LT-1001 is a precision amplifier combining excellent dc input specifications with low input voltage noise. Advanced circuit design, wafer processing, and test methods all contribute to these well-balanced, mutually supporting input characteristics.

The circuit design uses special low-noise transistor geometries and careful thermal layout to achieve exceptionally low noise and linear gain characteristics. A patented, proprietary test method which includes digital V_{OS} nulling after packaging as well as at wafer test tightens the distribution of this parameter such that the highest grade, the LT-1001AM, is specified at ±15 μV maximum. This low V_{OS}, along with extra-low power dissipation (which reduces warm-up drift), set the LT-1001 apart from similar precision op amp types.

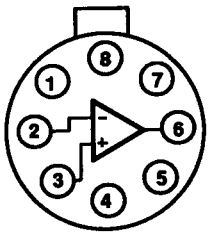
Ordering Information

Part Number	Package	Operating Temperature Range
LT-1001ACN	N	0°C to +70°C
LT-1001CN	N	0°C to +70°C
LT-1001ACM	M	0°C to +70°C
LT-1001CM	M	0°C to +70°C
LT-1001MT	T	-55°C to +125°C
LT-1001AMT/883B	T	-55°C to +125°C
LT-1001MD	D	-55°C to +125°C
LT-1001AMD/883B	D	-55°C to +125°C
LT-1001ML	L	-55°C to +125°C
LT-1001AML/883B	L	-55°C to +125°C

Notes:
/883B suffix denotes Mil-Std-883, Level B processing
N = 8-lead plastic DIP
D = 8 lead ceramic DIP
T = 8-lead metal can (TO-99)
L = 20-pad leadless chip carrier
M = 8-lead plastic SOIC
Contact a Raytheon sales office or representative for ordering information on special package/temperature range combinations.

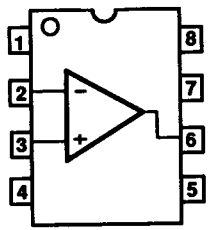
Connection Information

8-Lead TO-99 Metal Can
(Top View)



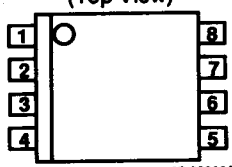
65-03205A

8-Lead Dual In-Line Package
(Top View)



65-03206A

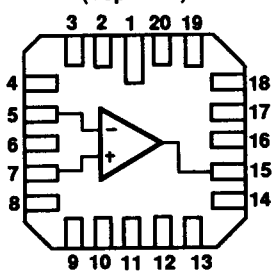
8-Lead Plastic Dual In-Line SO-8
(Top View)



65-02666A

Pin	Function
1	V_{OS} Trim
2	-Input
3	+Input
4	$-V_S$
5	NC
6	Output
7	$+V_S$
8	V_{OS} Trim

20-Pad LCC
(Top View)



65-02657A

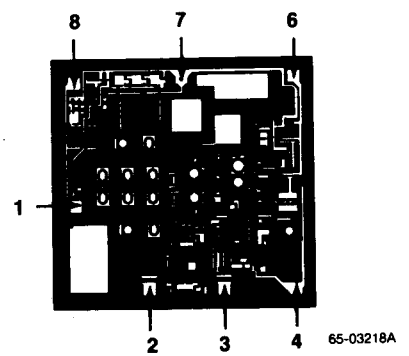
Pin	Function
2	V_{OS} Trim
5	-Input
7	+Input
10	$-V_S$
15	Output
17	$+V_S$
20	V_{OS} Trim

Absolute Maximum Ratings

Supply Voltage ..... ±22V
Input Voltage* ..... ±22V
Differential Input Voltage 30V
Internal Power Dissipation** ..... 500 mW
Output Short Circuit Duration ..... Indefinite
Storage Temperature
Range ..... -65°C to +150°C
Operating Temperature Range
M Suffix ..... -55°C to +125°C
C Suffix ..... 0°C to +70°C
Lead Soldering Temperature
(SO-8; 10 sec) ..... +260°C
Lead Soldering Temperature
(DIP, LCC, TO-99; 60 sec) ..... +300°C

*For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
**Observe package thermal characteristics.

Mask Pattern



65-03218A

Die Size: 75 x 78 mils
Min. Pad Dimensions: 4 x 4 mils

Thermal Characteristics

	20-Pad LCC	8-Lead Ceramic DIP	8-Lead TO-99 Metal Can	8-Lead Small Outline	8-Lead Plastic DIP
Max. Junction Temp.	175°C	175°C	175°C	125°C	125°C
Max. P_D T_A <50°C	925 mW	833 mW	658 mW	300 mW	468 mW
Therm. Res θ_{JC}	37°C/W	45°C/W	50°C/W	–	–
Therm. Res.θ_{JA}	105°C/W	150°C/W	190°C/W	240°C/W	160°C/W
For T_A >50°C Derate at	7.0 mW/°C	8.33 mW/°C	5.26 mW/°C	4.17 mW/°C	6.25 mW/°C

Electrical Characteristics (V_S = ±15V and T_A = +25°C unless otherwise noted)

Parameters	Test Conditions	LT-1001A			LT-1001M/C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]	LT-1001AM/883B		7.0	15		18	60	μV
	LT-1001AC		10	25				
Long Term Input Offset Voltage Stability[3,4]			0.2	1.0		0.2	1.5	μV/Mo
Input Offset Current			0.3	2.0		0.4	3.8	nA
Input Bias Current			±0.5	±2.0		±1.0	±4.0	nA
Input Noise Voltage[2]	0.1 Hz to 10 Hz		0.35	0.6		0.35	0.6	μV_{p-p}
Input Noise Voltage Density[2,5]	f_O = 10 Hz		10.3	18		10.3	18	$\frac{nV}{\sqrt{Hz}}$
	f_O = 100 Hz		10	13		10	13	
	f_O = 1000 Hz		9.6	11		9.6	11	
Input Noise Current[2]	0.1 Hz to 10 Hz		14	30		14	30	pA_{p-p}
Input Noise Current Density[5]	f_O = 10 Hz		0.32	0.8		0.32	0.8	$\frac{pA}{\sqrt{Hz}}$
	f_O = 100 Hz		0.14	0.23		0.14	0.23	
	f_O = 1000 Hz		0.12	0.17		0.12	0.17	
Input Resistance (Diff. Mode)[3]		30	100		15	80		MΩ
Input Resistance (Com. Mode)			200			200		GΩ
Input Voltage Range		±13	±14		±13	±14		V
Common Mode Rejection Ratio	V_{CM} = ±13V	114	126		110	126		dB
Power Supply Rejection Ratio	V_S = ±3V to ±18V	110	123		106	123		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±12V	450	2000		400	2000		V/mV
	$R_L \geq 1$ kΩ, V_O = ±10V	300	1000		250	1000		
Output Voltage Swing	$R_L \geq 2$ kΩ	±13	±14		±13	±14		V
	$R_L \geq 1$ kΩ	±12	±13.5		±12	±13.5		
Slew Rate	$R_L \geq 2$ kΩ	0.1	0.3		0.1	0.3		V/μS
Unity Gain Bandwidth	A_{VCL} = +1.0	0.4	0.8		0.4	0.8		MHz
Open Loop Output Resistance	V_O = 0, I_O = 0		60			60		Ω
Power Consumption	V_S = ±15V, R_L = ∞		50	75		50	80	mW
	V_S = ±3V, R_L = ∞		4.0	6.0		4.0	8.0	
Offset Adjustment Range	R_P = 20 kΩ		±4.0			±4.0		mV

Notes:

1. Input Offset Voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. LT1001AM/883B and LT-1001AC grades in hermetic packages are measured after the device is fully warmed up.
2. This parameter is tested on a sample basis only.
3. This parameter is guaranteed by design.
4. Long Term Input Offset Voltage Stability refers to the average trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically 2.5 μV.
5. 10 Hz input noise voltage density is sample tested on every lot. Devices 100% tested at 10 Hz are available on request.

Electrical Characteristics (V_S = ±15V and -55°C ≤ T_A ≤ +125°C unless otherwise noted)

Parameters	Test Conditions	LT-1001AM/883B			LT-1001M			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			25	60		45	160	µV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.0	µV/°C
With External Trim[3]	R_P = 20 kΩ		0.2	0.6		0.3	1.0	
Input Offset Current			0.8	4.0		1.2	7.6	nA
Average Input Offset Current Drift[2]			5.0	25		8.0	50	pA/°C
Input Bias Current			±1.0	±4.0		±1.5	±8.0	nA
Average Input Bias Current Drift[2]			8.0	25		13	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	123		106	123		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	104	117		100	117		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	300	600		200	600		V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±12.5	±13		±12	±13		V
Power Consumption	R_L = ∞		60	90		60	100	mW

See notes on page 3.

Electrical Characteristics (V_S = ±15V and 0°C ≤ T_A ≤ +70°C unless otherwise noted)

Parameters	Test Conditions	LT-1001AC			LT-1001C			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage[1]			20	60		30	110	µV
Average Input Offset Voltage Drift Without External Trim[2]			0.2	0.6		0.3	1.0	µV/°C
With External Trim[3]	R_P = 20 kΩ		0.2	0.6		0.3	1.0	
Input Offset Current			0.5	3.5		1.6	8.0	nA
Average Input Offset Current Drift[2]			8.0	35		12	50	pA/°C
Input Bias Current			±0.7	±3.5		±1.0	±5.5	nA
Average Input Bias Current Drift[2]			13	35		18	50	pA/°C
Input Voltage Range		±13	±13.5		±13	±13.5		V
Common Mode Rejection Ratio	V_{CM} = ±13V	110	123		106	120		dB
Power Supply Rejection Ratio	V_S = ±3.0V to ±18V	106	120		103	120		dB
Large Signal Voltage Gain	$R_L \geq 2$ kΩ, V_O = ±10V	300	600		250	600		V/mV
Output Voltage Swing	$R_L \geq 2$ kΩ	±12.5	±13.5		±12.5	±13.5		V
Power Consumption	R_L = ∞		60	85		60	90	mW

See notes on page 3.

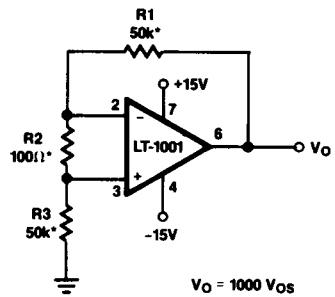
Applications Information

The LT-1001 series units may be inserted directly into OP-07, OP-05, 725, 108A or 101A sockets with or without removal of external frequency compensation or nulling components. The LT-1001 can also be used in 741 applications provided that the nulling circuitry is removed.

Unless proper care is exercised, thermocouple effects caused by temperature gradients across dissimilar metals at the contacts to the input terminals, can exceed the inherent drift of the amplifier. Air currents over device leads should be minimized, package leads should be short, and the two input leads should be as close together as possible and maintained at the same temperature.

Input bias currents may flow either into or out of the input terminals, depending on the value of I_{OS}.

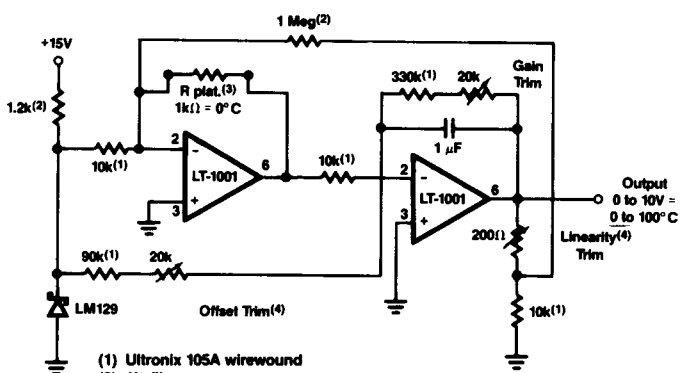
Typical Applications



65-03787A

*Resistors must have low thermoelectric potential.

Test Circuit for Offset Voltage and Its Drift With Temperature



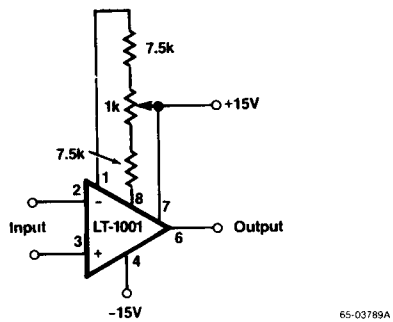
(1) Ultronix 105A wirewound
(2) 1% film
(3) Platinum RTD 118MF (Rosemount, Inc.)
(4) Trim sequence:
trim offset (0°C = 1000.0Ω),
trim linearity (35°C = 1138.7Ω),
trim gain (100°C = 1392.6Ω).
Repeat until all three points are fixed with ±0.025°C.

65-03788A

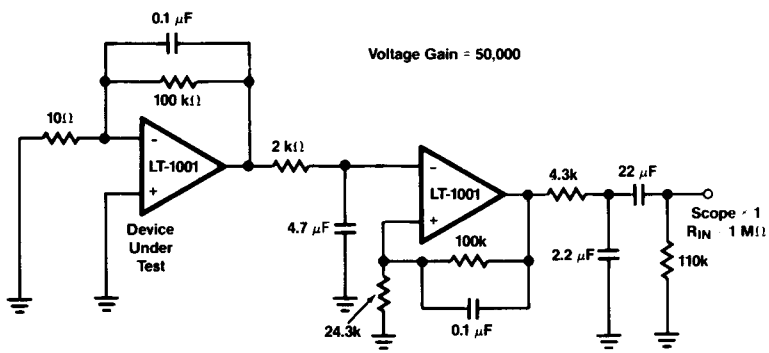
Linearized Platinum Resistance Thermometer With ±0.025°C Accuracy Over 0 to 100°C

Offset Voltage Adjustment

The input offset voltage of the LT-1001, and its drift with temperature, are permanently trimmed at wafer test to a low level. However, if further adjustment of V_{OS} is necessary, nulling with a 10k or 20k potentiometer will not degrade drift with temperature. Trimming to a value other than zero creates a drift of (V_{OS}/300) μV/°C, e.g., if V_{OS} is adjusted to 300 μV, the change in drift will be 1 μV/°C. The adjustment range with a 10k or 20k pot is approximately 4.0 mV. If less adjustment range is needed, the sensitivity and resolution of the nulling can be improved by using a smaller pot in conjunction with fixed resistors. The example below has an approximate null range of ±100 μV.



Improved Sensitivity Adjustment

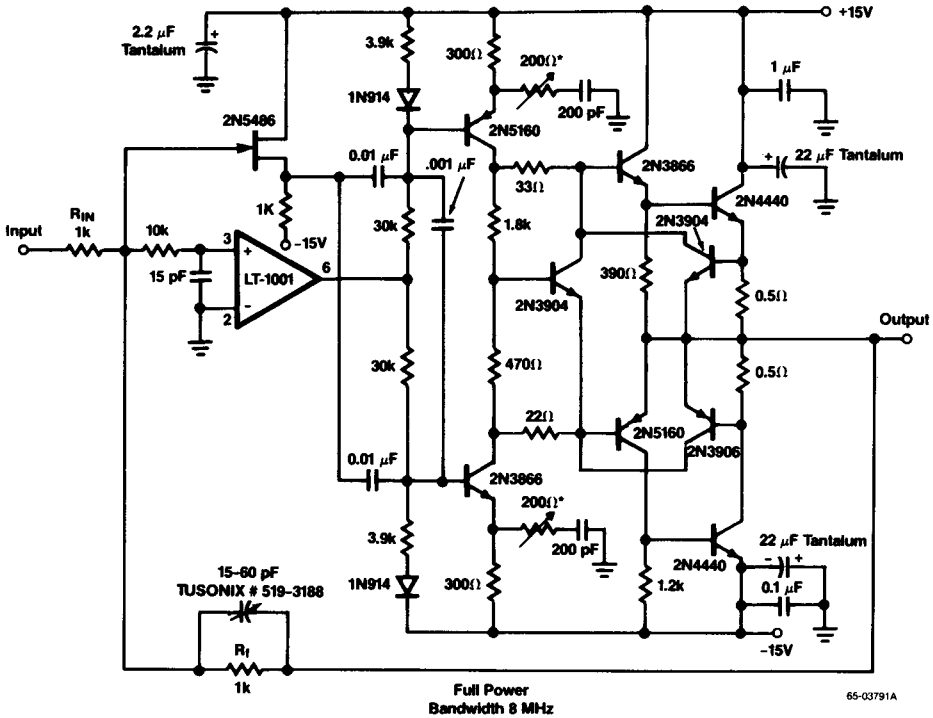


(1) Peak-to-peak noise is measured in a 10-second interval
(2) The device under test should be warmed up for 3 minutes and shielded from air currents.

65-03790A

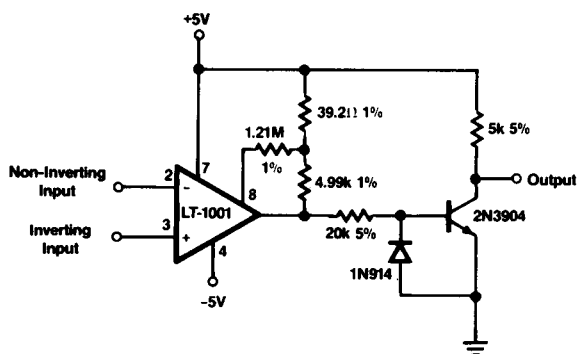
0.1 Hz to 10 Hz Noise Test Circuit

Typical Applications (Continued)



*Adjust for best squarewave at output.

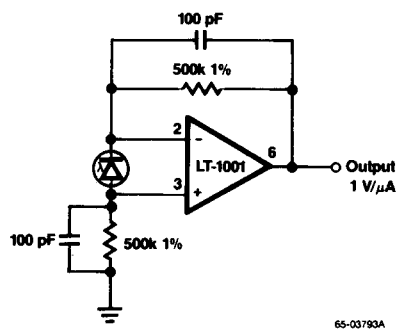
DC Stabilized — 1000 V/μS Op Amp



Positive feedback to one of the nulling terminals creates 5μ to 20 μV of hysteresis. Input offset voltage is typically changed by less than 5 μV due to the feedback.

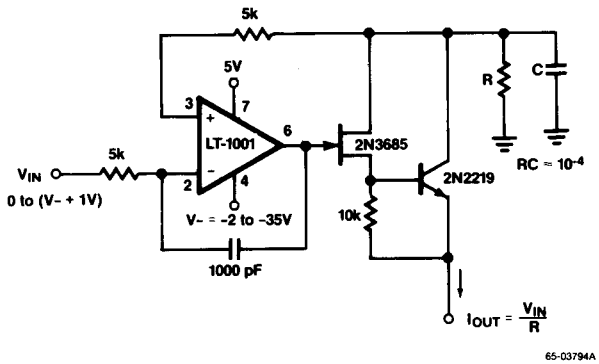
65-03792A

Microvolt Comparator With TTL Output

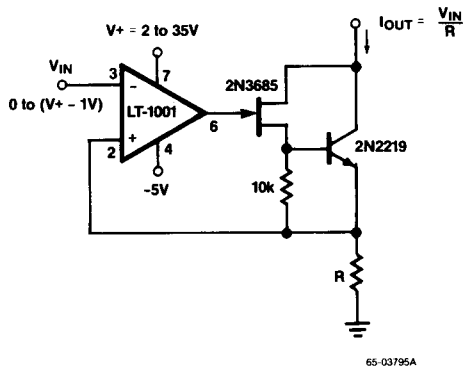


Photodiode Amplifier

Typical Applications (Continued)



Precision Current Source



Precision Current Sink

Schematic Diagram